Intel® Quartus® Prime Pro Edition
User Guide

Getting Started

Updated for Intel® Quartus® Prime Design Suite: 18.1
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1. Introduction to Intel® Quartus® Prime Pro Edition

This user guide describes basic concepts and operation of the Intel® Quartus® Prime Pro Edition design software, including GUI and project structure basics, initial design planning, use of Intel FPGA IP, and migration to Intel Quartus Prime Pro Edition. This software provides a complete design environment for the most advanced Intel Stratix® 10, Intel Arria® 10, and Intel Cyclone® 10 FPGA and SoC designs.

The Intel Quartus Prime software GUI supports easy design entry, fast design processing, straightforward device programming, and integration with other industry-standard EDA tools. The user interface makes it easy for you to focus on your design—not on the design tool. The modular Compiler streamlines the FPGA development process, and ensures the highest performance for the least effort.

Figure 1. Intel Quartus Prime Pro Edition Software GUI
The Intel Quartus Prime Pro Edition software expands on the capabilities of the Intel Quartus Prime Standard Edition, and provides unique features that support the latest Intel FPGAs. Select the Intel Quartus Prime software edition that provides the device support and features you require, as Selecting an Intel Quartus Prime Software Edition on page 6 describes.

The Intel Quartus Prime Pro Edition software offers flexible design methodologies, advanced synthesis, and supports the latest Intel FPGA architectures and hierarchical design flows. The Compiler provides powerful and customizable design processing to achieve the best possible design implementation in silicon. The following features are unique to the Intel Quartus Prime Pro Edition:

- Hyper-Aware Design Flow—use Hyper-Retiming and Fast Forward compilation to reach the highest performance in Intel Stratix 10 devices.
- Hierarchical project structure—preserve individual post-synthesis, post-placement, and post-place and route results for each design instance. Allows optimization without impacting other partition placement or routing.
- Incremental Fitter Optimizations—run and optimize Fitter stages incrementally. Each Fitter stage generates detailed reports.
- Faster, more accurate I/O placement—plan interface I/O in Interface Planner.
- Partial Reconfiguration—reconfigure a portion of the FPGA, while the remaining FPGA continues to function.
- Block-Based Design Flows—preserve and reuse design blocks at various stages of compilation.

1.1. Selecting an Intel Quartus Prime Software Edition

Depending on your device support and software feature requirements, you can choose either the Intel Quartus Prime Pro Edition or Intel Quartus Prime Standard Edition software for your design. Consider the requirements and timeline of your project in determining whether to select the Intel Quartus Prime Standard Edition or Intel Quartus Prime Pro Edition software:
Select the Intel Quartus Prime Pro Edition if you are beginning a new Intel Arria 10, Intel Cyclone 10 GX, or Intel Stratix 10 design, or to take advantage of the unique features of Intel Quartus Prime Pro Edition.

Figure 2. Intel Quartus Prime Feature Support Matrix

<table>
<thead>
<tr>
<th>Software Features</th>
<th>Intel Quartus Prime Standard Edition</th>
<th>Intel Quartus Prime Pro Edition</th>
</tr>
</thead>
<tbody>
<tr>
<td>New Hybrid Placer &amp; Global Router</td>
<td>✔</td>
<td>✔</td>
</tr>
<tr>
<td>New Timing Analyzer</td>
<td>✔</td>
<td>✔</td>
</tr>
<tr>
<td>New Physical Synthesis</td>
<td>✔</td>
<td>✔</td>
</tr>
<tr>
<td>Platform Designer (formerly Qsys)</td>
<td>✔</td>
<td>✔</td>
</tr>
<tr>
<td>Intel Stratix® 10, Intel Cyclone® 10 GX</td>
<td></td>
<td>✔</td>
</tr>
<tr>
<td>New Synthesis Engine</td>
<td></td>
<td>✔</td>
</tr>
<tr>
<td>Partial Reconfiguration</td>
<td></td>
<td>✔</td>
</tr>
<tr>
<td>Block-Based (Hierarchical) Design Flows</td>
<td></td>
<td>✔</td>
</tr>
<tr>
<td>OpenCL support</td>
<td></td>
<td>✔</td>
</tr>
<tr>
<td>Incremental Fitter Optimization</td>
<td></td>
<td>✔</td>
</tr>
<tr>
<td>Interface Planner (formerly BluePrint)</td>
<td></td>
<td>✔</td>
</tr>
</tbody>
</table>

Select the Intel Quartus Prime Standard Edition software if your design must target Arria V, Arria, Intel Cyclone 10 LP, Cyclone IV, Cyclone V, or MAX® series devices, and you do not want to migrate your design to a device that Intel Quartus Prime Pro Edition supports.

Intel Quartus Prime Pro Edition software does not support the following Intel Quartus Prime Standard Edition features:

- I/O Timing Analysis
- NativeLink third party tool integration (other third-party tool integration available)
- Video and Image Processing Suite IP Cores
- Talkback features
- Various register merging and duplication settings
- Saving a node-level netlist as .vqm
- Compare project revisions
Note: Intel replaces the following Altera tool names in the Intel Quartus Prime software:

<table>
<thead>
<tr>
<th>Altera Name</th>
<th>Intel Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>Qsys</td>
<td>Platform Designer</td>
</tr>
<tr>
<td>BluePrint</td>
<td>Interface Planner</td>
</tr>
<tr>
<td>TimeQuest</td>
<td>Timing Analyzer</td>
</tr>
<tr>
<td>EyeQ</td>
<td>Eye Viewer</td>
</tr>
<tr>
<td>JNEye</td>
<td>Advanced Link Analyzer</td>
</tr>
</tbody>
</table>

Related Information
Migrating to Intel Quartus Prime Pro Edition on page 91

1.2. Introduction to Intel Quartus Prime Pro Edition Revision History

<table>
<thead>
<tr>
<th>Document Version</th>
<th>Intel Quartus Prime Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>2018.09.24</td>
<td>18.1.0</td>
<td>• Added screenshot of Intel Quartus Prime Pro Edition GUI.</td>
</tr>
<tr>
<td>2018.05.07</td>
<td>18.0</td>
<td>Initial release as separate chapter of Getting Started User Guide.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Separated Migrating to Intel Quartus Prime Pro Edition as independent chapter in user guide.</td>
</tr>
<tr>
<td>2017.11.06</td>
<td>17.1.0</td>
<td>• Described Intel Quartus Prime tool name updates for Platform Designer (Qsys), Interface Planner (BluePrint), Timing Analyzer (TimeQuest), Eye Viewer (EyeQ), and Advanced Link Analyzer (Advanced Link Analyzer).</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added Verilog HDL Macro example.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Updated for latest Intel branding conventions.</td>
</tr>
<tr>
<td>2017.05.08</td>
<td>17.0.0</td>
<td>• Removed statement about limitations for safe state machines. The Compiler supports safe state machines. State machine inference is enabled by default.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added reference to Block-Based Design Flows.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Removed procedure on manual dynamic synthesis report generation. The Compiler automatically generates dynamic synthesis reports when enabled.</td>
</tr>
<tr>
<td>2016.10.31</td>
<td>16.1.0</td>
<td>• Implemented Intel rebranding.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added reference to Partial Reconfiguration support.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added to list of Intel Quartus Prime Standard Edition features unsupported by Intel Quartus Prime Pro Edition.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added topic on Safe State Machine encoding.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Described unsupported Intel Quartus Prime Standard Edition physical synthesis options.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Removed deprecated Per-Stage Compilation (Beta) Compilation Flow.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Changed title from &quot;Remove Filling Vectors&quot; to &quot;Remove Unsized Constant&quot;.</td>
</tr>
<tr>
<td>2016.05.03</td>
<td>16.0.0</td>
<td>• Removed software beta status and revised feature set.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added topic on Safe State Machine encoding.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added Generating Dynamic Synthesis Reports.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Corrected statement about Verilog Compilation Unit.</td>
</tr>
</tbody>
</table>

continued...
### Changes

- Corrected typo in Modify Entity Name Assignments.
- Added description of Fitter Plan, Place and Route stages, reporting, and optimization.
- Added [Per-Stage Compilation (Beta)](https://www.intel.com) Compilation Flow.
- Added Platform Designer information.
- Added OpenCL and Signal Tap with routing preservation as unique Pro Edition features.
- Clarified limitations for multiple Logic Lock instances in the same region.

<table>
<thead>
<tr>
<th>Document Version</th>
<th>Intel Quartus Prime Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>2015.11.02</td>
<td>15.1.0</td>
<td>First version of document.</td>
</tr>
</tbody>
</table>

### Related Information

#### Documentation Archive

For previous versions of the *Intel Quartus Prime Handbook*, search the documentation archives.
2. Managing Intel Quartus Prime Projects

The Intel Quartus Prime software organizes and manages the elements of your design within a project. The project encapsulates information about your design files, hierarchy, libraries, constraints, and project settings. This chapter describes the basics of working with Intel Quartus Prime software projects, including initial project setup, viewing project information, adding design files and constraints, and exporting compilation results.

Click **File > New Project Wizard** to quickly setup and open a new project.

**Figure 3. New Project Wizard**

After you create or open a project, the GUI displays integrated information and controls for the open project.
2.1. Viewing Basic Project Information

You can view basic information about your project in the Tasks pane, Project Navigator, Compilation Dashboard, Report panel, and Messages window.

**Project Tasks Pane**

The Tasks pane (View ➤ Tasks) provides one-click launch of common project tasks, such as creating design files, specifying project settings, running compilation, debug and timing closure, and device programming.

![Project Tasks Pane](image)

**Figure 4. Project Tasks Pane**

**The Project Navigator**

The Project Navigator (View ➤ Project Navigator) displays information about the elements of your project, such as the design files, IP components, and your project hierarchy (after elaboration). You can right-click items in the Project Navigator to locate or perform actions on the elements of your project. The Project Navigator organizes information on the Files, Hierarchy, Design Units, and IP Components tabs.
Table 2. Project Navigator Tabs

<table>
<thead>
<tr>
<th>Project Navigator Tab</th>
<th>Description</th>
</tr>
</thead>
</table>
| Files                 | Lists all design files in the current project. Right-click design files in this tab to run these commands:  
  • **Open** the file  
  • **Remove** the file from project  
  • View file **Properties** |
| Hierarchy             | Provides a visual representation of the project hierarchy, specific resource usage information, and device and device family information. Right-click items in the hierarchy to **Locate**, **Set as Top-Level Entity**, or define Logic Lock regions or design partitions. |
| Design Units          | Displays the design units in the project. Right-click a design unit to **Locate in Design File**. |
| IP Components         | Displays the design files that make up the IP instantiated in the project, including Intel FPGA IP, Platform Designer components, and third-party IP. Click **Launch IP Upgrade Tool** from this tab to upgrade outdated IP components. Right-click any IP component to **Edit in Parameter Editor**. |

Figure 5. Project Navigator Hierarchy, Files, Design Units, and IP Components Tabs

2.1.1. Using the Compilation Dashboard

The Compilation Dashboard provides immediate access to settings, controls, and reporting for each stage of the compilation flow.
The Compilation Dashboard appears by default when you open a project, or you can click **Compilation Dashboard** in the Tasks window to re-open it.

- Click the pencil icon to edit settings for that stage of the compilation flow.
- Click **Compile Design** to run all modules of the Compiler in sequence, or click any individual Compiler module to run compilation through that stage.
- Click the report icon to view reports for that compilation stage.

**Figure 6. Compilation Dashboard**

As the Compiler progresses through the flow, the dashboard updates the status of each module, and enables icons that you can click for reports and analysis.

### 2.1.2. Viewing Project Reports

The Compilation Report panel updates dynamically to display detailed reports during project processing.

To access Compilation Reports, click **(Processing ➤ Compilation Report)**:

Analyze the detailed information in these reports to determine correct implementation. Right-click report data to locate and edit the source in project files.
2.1.3. Viewing Project Messages

The Messages window (View ➤ Messages) displays information, warning, and error messages about Intel Quartus Prime processes. Right-click messages to locate the source or get message help.

- **Processing** tab—displays messages from the most recent process
- **System** tab—displays messages unrelated to design processing
- **Search**—locates specific messages

Messages are written to stdout when you use command-line executables.
To suppress display of unimportant messages, right-click one or more messages and click on of the following:

- **Suppress Message**—suppresses all messages matching exact text
- **Suppress Messages with Matching ID**—suppresses all messages matching the message ID number, ignoring variables
- **Suppress Messages with Matching Keyword**—suppresses all messages matching keyword or hierarchy

You cannot suppress error or Intel legal agreement messages.
Suppressing a message also suppresses any submessages.
Message suppression is project revision-specific. Derivative project revisions inherit any suppression.
You cannot edit messages or suppression rules during compilation.
2.2. Intel Quartus Prime Project Contents

The Intel Quartus Prime software organizes your design work within a project. You can create and compare multiple revisions of your project, to experiment with settings that achieve your design goals. When you create a new project in the GUI, the Intel Quartus Prime software automatically creates an Intel Quartus Prime Project File (.qpf) for that project. The .qpf references the Intel Quartus Prime Settings File (.qsf). The .qsf lists the project's design, constraint, and IP files, and stores project-wide and entity-specific settings that you specify in the GUI. You do not need to edit the text-based .qpf or .qsf files directly. The Intel Quartus Prime software creates and updates these files automatically as you make changes in the GUI.

Table 3. Intel Quartus Prime Project Files

<table>
<thead>
<tr>
<th>File Type</th>
<th>Contains</th>
<th>To Edit</th>
<th>Format</th>
</tr>
</thead>
<tbody>
<tr>
<td>Project file</td>
<td>Project and revision name</td>
<td>File ➤ New Project Wizard</td>
<td>Intel Quartus Prime Project File (.qpf)</td>
</tr>
<tr>
<td>Settings file</td>
<td>Lists design files, entity settings, target device, synthesis directives, placement constraints</td>
<td>Assignments ➤ Settings</td>
<td>Intel Quartus Prime Settings File (.qsf)</td>
</tr>
<tr>
<td>Quartus database</td>
<td>Project compilation results</td>
<td>Project ➤ Export Design</td>
<td>Quartus Database File (.qdb)</td>
</tr>
<tr>
<td>Partition database</td>
<td>Partition compilation results</td>
<td>Project ➤ Export Design Partition</td>
<td>Partition Database File (.qdb)</td>
</tr>
<tr>
<td>Timing constraints</td>
<td>Clock properties, exceptions, setup/hold</td>
<td>Tools ➤ Timing Analyzer</td>
<td>Synopsys Design Constraints File (.sdc)</td>
</tr>
<tr>
<td>Logic design files</td>
<td>RTL and other design source files</td>
<td>File ➤ New</td>
<td>All supported HDL files</td>
</tr>
<tr>
<td>Programming files</td>
<td>Device programming image and information</td>
<td>Tools ➤ Programmer</td>
<td>SRAM Object File (.sof)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Programmer Object File (.pof)</td>
</tr>
<tr>
<td>IP core files</td>
<td>IP core variation parameterization</td>
<td>Tools ➤ IP Catalog</td>
<td>Intel Quartus Prime IP File (.ip)</td>
</tr>
<tr>
<td>Platform Designer system files</td>
<td>System definition</td>
<td>Tools ➤ Platform Designer</td>
<td>Platform Designer System File (.qsys)</td>
</tr>
<tr>
<td>EDA tool files</td>
<td>Scripts for third-party EDA tools</td>
<td>Assignments ➤ Settings ➤ EDA Tool Settings</td>
<td>Verilog Output File (.vo)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>VHDL Output File (.vho)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Verilog Quartus Mapping File (.vqm)</td>
</tr>
<tr>
<td>Archive files</td>
<td>Complete project as single compressed file</td>
<td>Project ➤ Archive Project</td>
<td>Intel Quartus Prime Archive File (.qar)</td>
</tr>
</tbody>
</table>

2.2.1. Project File Best Practices

The Intel Quartus Prime software provides various options for specifying project settings and constraints. The following best practices help ensure automated management and portability of your project files.
Avoid manually editing Intel Quartus Prime data files, such as the Intel Quartus Prime Project File (.qpf), Intel Quartus Prime Settings File (.qsf), Quartus IP File (.ip), or Platform Designer System File (.qsys). Syntax errors in these files cause errors during compilation. For example, the software may ignore improperly formatted settings and assignments.

Do not compile multiple projects into the same directory. Instead, use a separate directory for each project.

By default, the Intel Quartus Prime software saves all project output files, such as Text-Format Report Files (.rpt), in the project directory. If you want to change the location of output files, instead of manually moving project output files, click Assignments ➤ Settings ➤ Compilation Process Settings, and specify the Save project output files in specified directory option.

2.3. Managing Project Settings

The New Project Wizard guides you to make initial project settings when you setup a new project. You can modify these and other global project settings in the Settings and Device dialog boxes, respectively. The .qsf stores the settings for each project revision. The optimization of these project settings helps the Compiler to generate programming files that meet or exceed your specifications.

Global Project Settings

To access global project settings, click Assignments ➤ Settings, or click Settings on the Tasks pane.

Figure 10. Settings Dialog Box for Global Project Settings

The Settings dialog box provides access to settings that control project design files, synthesis, Fitter, and timing constraints, operating conditions, EDA tool file generation, programming file generation, and other project-level settings.
Additionally, the Assignment Editor (Assignments ➤ Assignment Editor) provides a spreadsheet-like interface for specifying instance-specific settings and constraints.

Figure 11. Assignment Editor

![Assignment Editor](image)

### 2.3.1. Specifying the Target Device or Board

Specify the target Intel device or board for your project in the **Device** dialog box. Click the **Device and Pin Options** button in the dialog to specify preferences for the device configuration scheme, programming file generation, I/O timing, voltage, and other options.

1. Open a project in the Intel Quartus Prime software.
2. Click **Assignments ➤ Device**.

Figure 12. Device Dialog Box

![Device Dialog Box](image)

3. Specify either a target Intel FPGA board or device for your project. When you specify a board, the Intel Quartus Prime software generates the appropriate pin assignments script for that board automatically.
To specify an Intel FPGA board or development kit for your project:

a. Click the **Board** tab.
b. Select the target device **Family** and a supported **Development Kit**. Click **Yes** if prompted to remove existing **Location** and **I/O Standard** pin assignments. The Intel Quartus Prime software creates the kit's baseline design and stores the design in `<current_project_dir>/devkits/<design_name>`. To retain all your existing pin assignments, click **No**.
c. Select the desired development kit and click **OK**.

To specify a device family for your project:

a. On the **Device** tab, select the **Family** and **Device** name. The list of **Available devices** reflects your selections.
b. To further refine your selection, specify options for the **Package**, **Pin count**, **Core speed grade**, **Name filter**, and **Show advanced devices** filters.
c. From the **Available devices**, select your target device **Name** and click **OK**.

### 2.3.2. Optimizing Project Settings

Optimize project settings to meet your design goals. The Intel Quartus Prime Design Space Explorer II iteratively compiles your project with various setting combinations to find the optimal settings for your goals. Alternatively, you can create a project revision or project copy to manually compare various project settings and design combinations.

The Intel Quartus Prime software includes several advisors to help you optimize your design and reduce compilation time. The advisors listed in the **Tools ➤ Advisors** menu can provide recommendations based on your project settings and design constraints.

#### 2.3.2.1. Optimize Settings with Design Space Explorer II

Use Design Space Explorer II (**Tools ➤ Launch Design Space Explorer II**) to find optimal project settings for resource, performance, or power optimization goals. Design Space Explorer II (DSE II) processes your design using various setting and constraint combinations, and reports the best settings for your design.

DSE II attempts multiple seeds to identify one meeting your requirements. DSE II can run different compilations on multiple computers in parallel to streamline timing closure.
You can save multiple, named project revisions within your Intel Quartus Prime project (Project > Revisions). Each project revision captures a unique set of project settings and constraints, while using the same set of logic design files.

Use revisions to experiment with different settings while preserving the original. Optimize different revisions for separate applications:

- Create a unique revision to optimize a design for different criteria, such as by area in one revision and by $f_{\text{MAX}}$ in another revision.
- When you create a new revision the default Intel Quartus Prime settings initially apply.
- Create a revision of a revision to experiment with settings and constraints. The child revision includes all the assignments and settings of the parent revision.

You create, delete, and edit revisions in the Revisions dialog box. Each time you create a new project revision, the Intel Quartus Prime software creates a new .qsf using the revision name.

To compare each revision’s synthesis, fitting, and timing analysis results side-by-side, click Project > Revisions and then click Compare. In addition to viewing the compilation Results of each revision, you can also compare the Assignments for each revision. This comparison reveals how different optimization options affect your design.
2.3.2.3. Back-Annotating Compiler Assignments

The Compiler maps the elements of your design to specific device resources during fitting. After compilation, you can back-annotate (copy) the Compiler's device and resource assignments to the project .qsf if you want to preserve that same implementation in subsequent compilations.

Click Assignments ➤ Back-Annotate Assignments to copy the device resource assignments from the last compilation to the .qsf for use in the next compilation. Select the back-annotation type in the Back-annotation type list.

2.4. Managing Logic Design Files

The Intel Quartus Prime software helps you create and manage the logic design files in your project. Logic design files contain the logic that implements your design. When you add a logic design file to the project, the Compiler automatically includes that file in the next compilation. The Compiler synthesizes your logic design files to generate programming files for your target device.

The Intel Quartus Prime software includes full-featured schematic and text editors, as well as HDL templates to accelerate your design work. The Intel Quartus Prime software supports VHDL Design Files (.vhd), Verilog HDL Design Files (.v),
SystemVerilog (.sv) and schematic Block Design Files (.bdf). In addition, you can combine your logic design files with Intel and third-party IP core design files, including combining components into a Platform Designer system (.qsys).

The New Project Wizard prompts you to identify logic design files. Add or remove project files by clicking **Project > Add/Remove Files in Project**. View the project’s logic design files in the Project Navigator.

**Figure 15. Design and IP Files in Project Navigator**

Right-click files in the Project Navigator to:

- **Open** and edit the file
- **Remove File from Project**
- **Set as Top-Level Entity** for the project revision
- **Create a Symbol File for Current File** for display in schematic editors
- **Edit file Properties**

### 2.4.1. Including Design Libraries

Include design files libraries in your project. Specify libraries for a single project, or for all Intel Quartus Prime projects. The .qsf stores project library information.

The quartus2.ini file stores global library information.

1. Click **Assignment > Settings**.
2. Click **Libraries** and specify the **Project Library name** or **Global Library name**. Alternatively, you can specify project libraries with SEARCH_PATH in the .qsf, and global libraries in the quartus2.ini file.

**Related Information**

- Design Library Migration Guidelines on page 35

### 2.4.2. Creating a Project Copy

Click **Project > Copy Project** to create a separate copy of your project, rather than just a revision within the same project.
The project copy includes separate copies of all design files, any .qsf files, and project revisions. You can use this technique to optimize project copies for different applications that require design file differences. For example, you can optimize one project to interface with a 32-bit data bus, and optimize a project copy to interface with a 64-bit data bus.

2.5. Managing Timing Constraints

Apply appropriate timing constraints to correctly optimize fitting and analyze timing for your design. The Fitter optimizes the placement of logic in the device to meet your specified timing and routing constraints.

Specify timing constraints in the Timing Analyzer (Tools > Timing Analyzer), or in an .sdc file. Specify constraints for clock characteristics, timing exceptions, and external signal setup and hold times before running analysis. The Timing Analyzer reports detailed information about the performance of your design compared with constraints in the Compilation Report panel.

Save the constraints you specify in the GUI in an industry-standard Synopsys Design Constraints File (.sdc). You can subsequently edit the text-based .sdc file directly. If you refer to multiple .sdc files in a parent .sdc file, the Timing Analyzer reads the .sdc files in the order you list.

Figure 16. Timing Analyzer
2.6. Integrating Other EDA Tools

Optionally integrate supported EDA design entry, synthesis, simulation, physical synthesis, and formal verification tools into the Intel Quartus Prime design flow. The Intel Quartus Prime software supports netlist files from other EDA design entry and synthesis tools. The Intel Quartus Prime software optionally generates various files for use in other EDA tools.

The Intel Quartus Prime software manages EDA tool files and provides the following integration capabilities:

- Compile all RTL and gate-level simulation model libraries for your device, simulator, and design language automatically (Tools > Launch Simulation Library Compiler).
- Include files generated by other EDA design entry or synthesis tools in your project as synthesized design files (Project > Add/Remove File from Project).
- Automatically generate optional files for board-level verification (Assignments > Settings > EDA Tool Settings).

Figure 17. EDA Tool Settings

2.7. Exporting Compilation Results

When you run compilation, the Compiler preserves a database of results in a Quartus Database File (.qdb). The .qdb contains the data to reproduce similar results in another project, or in a later software version. You can export your project’s compilation results database for import to another project or migration to a later Intel Quartus Prime software version.
You can export the .qdb for your entire project or for a design partition that you define in your project. When migrating the database for an entire project, you can export the compilation database in a version-compatible format to ensure compatibility for import to a later software version. Although you cannot directly read the contents of the .qdb file after export, you can view attributes of the database file in the Quartus Database File Viewer.

Table 4. Exporting Compilation Results

<table>
<thead>
<tr>
<th>To Export Compilation Results For</th>
<th>Method</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Complete Design</td>
<td>Click Project ➤ Export Design</td>
<td>Saves compilation results for the entire project in a version-compatible Quartus database file (.qdb) that you can import to another project or migrate to a later version of the Intel Quartus Prime software. You can export the results for the synthesized or final compilation snapshot.</td>
</tr>
<tr>
<td>Design Partition</td>
<td>Click Project ➤ Export Design Partition</td>
<td>Saves compilation results for a design partition as a Partition Database File (.qdb) that you can import to another project using the same version of the Intel Quartus Prime software. You can export the results for the synthesized or final compilation snapshot.</td>
</tr>
</tbody>
</table>

2.7.1. Exporting a Version-Compatible Compilation Database

To export a project compilation database to a format that ensures version-compatibility with a later version of the Intel Quartus Prime software:

1. In the Intel Quartus Prime software, open the project that you want to export.
2. Generate synthesis or final compilation results by running one of the following commands:
   - Click Processing ➤ Start ➤ Start Analysis & Synthesis to generate synthesized compilation results.
   - Click Processing ➤ Start Compilation to generate final compilation results.
3. Click Project ➤ Export Design. Select the synthesized or final Snapshot.

Figure 18. Export Design Dialog Box

4. Specify a name for the Quartus Database File to contain the exported results, and click OK.
5. To include the exported design's settings and constraint files, copy the .qsf and .sdc files to the import project directory.
2.7.2. Importing a Version-Compatible Compilation Database

Follow these steps to import a project compilation database into a newer version of the Intel Quartus Prime software:

1. Export a version-compatible compilation database for a complete design, as Exporting a Version-Compatible Compilation Database on page 25 describes.

2. In a newer version of the Intel Quartus Prime software, open the original project. Click Yes if prompted to open a project created with a different software version.

3. Click Project ➤ Import Design and specify the Quartus Database File. To remove previous results, turn on Overwrite existing project’s databases.

Figure 19. Import Design Dialog Box

4. Click OK.

5. When you compile the imported design, run only Compiler stages that occur after the stage that the .qdb preserves, rather than running a full compilation. For example, if you import a version-compatible database that contains the synthesis snapshot, start compilation with the Fitter (Processing ➤ Start ➤ Start Fitter). If you import a version-compatible database that contains the final snapshot, start compilation with Timing Analysis (Signoff) (Processing ➤ Start ➤ Start Timing Analysis (Signoff)).

2.7.3. Creating a Design Partition

A design partition is a logical, named, hierarchical boundary that you can assign to an instance in your design. Defining a design partition allows you to optimize and lock down the compilation results for individual blocks. You can then optionally export the compilation results of a design partition for reuse in another context, such as reuse in another project.
Follow these steps to create and modify design partitions:

1. In the Intel Quartus Prime software, open the project that you want to partition.
2. Generate synthesis or final compilation results by running one of the following commands:
   - Click **Processing ➤ Start ➤ Start Analysis & Synthesis** to generate synthesized compilation results.
   - Click **Processing ➤ Start Compilation** to generate final compilation results.
3. In the Project Navigator, right-click an instance in the **Hierarchy** tab, click **Design Partition ➤ Set as Design Partition**.
4. To view and edit all design partitions in the project, click **Assignments ➤ Design Partitions Window**.
5. Specify the properties of the design partition in the Design Partitions Window. The following settings are available:

Table 5. Design Partition Settings

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Partition Name</td>
<td>Specifies the partition name. Each partition name must be unique and consist of only alphanumeric characters. The Intel Quartus Prime software automatically creates a top-level &quot;root_partition&quot; for each project revision.</td>
</tr>
<tr>
<td>Hierarchy Path</td>
<td>Specifies the hierarchy path of the entity instance that you assign to the partition. You specify this value in the Create New Partition dialog box. The root partition hierarchy path is</td>
</tr>
</tbody>
</table>
| Type                     | Double-click to specify one of the following partition types that control how the Compiler processes and implements the partition:  
- Default—Identifies a standard partition. The Compiler processes the partition using the associated design source files.  
- Reconfigurable—Identifies a reconfigurable partition in a partial reconfiguration flow. Specify the Reconfigurable type to preserve synthesis results, while allowing refit of the partition in the PR flow.  
- Reserved Core—Identifies a partition in a block-based design flow that is reserved for core development by a Consumer reusing the device periphery. |
| Preservation Level       | Specifies one of the following preservation levels for the partition:  
- Not Set—specifies no preservation level. The partition compiles from source files.  
- synthesized—the partition compiles using the synthesized snapshot.  
- final—the partition compiles using the final snapshot. |
| Empty                    | Specifies an empty partition that the Compiler skips. This setting is incompatible with the Reserved Core and Partition Database File settings for the same partition. The Preservation Level must be Not Set. An empty partition cannot have any child partitions. |
| Partition Database File  | Specifies a Partition Database File (.qdb) that the Compiler uses during compilation of the partition. You export the .qdb for the stage of compilation that you want to reuse (synthesized or final). Assign the .qdb to a partition to reuse those results in another context. |
| Entity Re-binding        | PR Flow—specifies the entity that replaces the default persona in each implementation revision.  
- Root Partition Reuse Flow —specifies the entity that replaces the reserved core logic in the consumer project. |
| Color                    | Specifies the color-coding of the partition in the Chip Planner and Design Partition Planner displays. |
| Post Synthesis Export File | Automatically exports post-synthesis compilation results for the partition to the .qdb that you specify, each time Analysis & Synthesis runs. You can automatically export any design partition that does not have a preserved parent partition, including the root_partition. |
| Post Final Export File   | Automatically exports post-final compilation results for the partition to the .qdb that you specify, each time the final stage of the Fitter runs. You can automatically export any design partition that does not have a preserved parent partition, including the root_partition. |
2.7.4. Exporting a Design Partition

The following steps describe export of design partitions that you create in your project.

When you compile a design containing design partitions, the Compiler can preserve a synthesis or final snapshot of results for each partition. You can export the synthesized or final compilation results for individual design partitions with the Export Design Partition dialog box.

If the partition includes any entity-bound .sdc files, you can include those constraints in the .qdb. In addition, you can automate export of one or more partitions in the Design Partitions Window.

Manual Design Partition Export

Follow these steps to manually export a design partition with the Export Design Partition dialog box:

1. Open a project and create one or more design partitions. Creating a Design Partition on page 26 describes this process.
2. Run synthesis (Processing ➤ Start ➤ Start Analysis & Synthesis) or full compilation (Processing ➤ Start Compilation), depending on which compilation results that you want to export.
3. Click Project ➤ Export Design Partition, and specify one or more options in the Export Design Partition dialog box:

Figure 23. Export Design Partition Dialog Box

Export Design Partition

Allows you to export a design partition of a specified snapshot as a Partition Database File (.qdb). You can reuse the file in a design partition of another project.

Partition name:

speed_ch

Partition Database File

File name: speed_ch.qdb

Include entity-bound SDC files for the selected partition

SDC File Entity Assignments

Entity | SDC file
---|---

Snapshot:

synthesized
• Select the **Partition name** and the compilation **Snapshot** for export.
• To include any entity-bound `.sdc` files in the exported `.qdb`, turn on **Include entity-bound SDC files for the selected partition**.

4. Click **OK**. The compilation results for the design partition exports to the file that you specify.

**Automated Design Partition Export**

Follow these steps to automatically export one or more design partitions following each compilation:

1. Open a project containing one or more design partitions. *Creating a Design Partition* on page 26 describes this process.
2. To open the Design Partitions Window, click **Assignments ➤ Design Partitions Window**.
3. To automatically export a partition with synthesis results after each time you run synthesis, specify the a `.qdb` export path and file name for the **Post Synthesis Export File** option for that partition. If you specify only a file name without path, the file exports to the `output_files` directory after compilation.
4. To automatically export a partition with final snapshot results each time you run the Fitter, specify a `.qdb` file name for the **Post Final Export File** option for that partition. If you specify only a file name without path, the file exports to the `output_files` directory after compilation.

**Figure 24. Specifying Export File in Design Partitions Window**

![Design Partitions Window](image)

**.qsf Equivalent Assignment:**

```
set_instance_assignment -name EXPORT_PARTITION_SNAPSHOT_<FINAL|SYNTHESIZED> \
<hpath> -to <file_name>.qdb
```

**Related Information**

• Intel Quartus Prime Pro Edition User Guide: Block-Based Design
• Intel Quartus Prime Pro Edition User Guide: Partial Reconfiguration
2.7.5. Reusing a Design Partition

You can reuse the compilation results of a design partition exported from another Intel Quartus Prime project. Reuse of a design partition allows you to share a synthesized or final design block with another designer. Refer to Intel Quartus Prime Pro Edition User Guide: Block-Based Design for more information about reuse of design partitions.

To reuse an exported design partition in another project, you assign the exported partition .qdb to an appropriately configured design partition in the target project via the Design Partition Window:

1. Export a design partition with the appropriate snapshot, as Exporting a Design Partition on page 29 describes.
2. Open the target Intel Quartus Prime project that you want to reuse the exported partition.
3. Click Processing ➤ Start ➤ Start Analysis & Elaboration.
4. Click Assignments ➤ Design Partitions Window, and then create an appropriately sized design partition to contain the logic and compilation results of the exported .qdb.
5. Click the Partition Database File option for the new partition and select the exported .qdb file.

![Partition Database File Setting in Design Partitions Window](image)

6. Specify any other properties of the design partition in the Design Partitions Window. The Compiler uses the partition's assigned .qdb as the source.

2.7.6. Viewing Quartus Database File Information

Although you cannot directly read a .qdb file, you can view helpful attributes about the file to quickly identify its contents and suitability for use.

The Intel Quartus Prime software automatically stores metadata about the project of origin when you export a Quartus Database File (.qdb). The Intel Quartus Prime software automatically stores metadata about the project of origin and resource utilization when you export a Partition Database File (.qdb) from your project. You can then use the Quartus Database File Viewer to display the attributes any of these .qdb files.
Figure 26.  Quartus Database File Viewer

Follow these steps to view the attributes of a .qdb file:

1. In the Intel Quartus Prime software, click File ➤ Open, select Design Files for Files of Type, and select a .qdb file.

2. Click Open. The Quartus Database File Viewer displays project and resource utilization attributes of the .qdb.

Alternatively, run the following command-line equivalent:

```bash
quartus_cdb --extract_metadata --file <archive_name.qdb> \
--type quartus --dir <extraction_directory> \
[--overwrite]
```

2.7.6.1. QDB File Attribute Types

The Quartus Database Viewer can display the following attributes of a .qdb file:

<table>
<thead>
<tr>
<th>QDB Attribute Types</th>
<th>Attribute</th>
<th>Example</th>
</tr>
</thead>
<tbody>
<tr>
<td>Project Information</td>
<td>Contents</td>
<td>Partition</td>
</tr>
<tr>
<td></td>
<td>Date</td>
<td>Thu Jan 23 10:56:23 2018</td>
</tr>
<tr>
<td></td>
<td>Device</td>
<td>10AX016C3U19E2LG</td>
</tr>
<tr>
<td></td>
<td>Entity (if Partition)</td>
<td>Counter</td>
</tr>
<tr>
<td></td>
<td>Family</td>
<td>Arria 10</td>
</tr>
<tr>
<td></td>
<td>Partition Name</td>
<td>root_partition</td>
</tr>
</tbody>
</table>
### Resource Utilization (exported for partition QDB only)

<table>
<thead>
<tr>
<th>Revision Name</th>
<th>Top</th>
</tr>
</thead>
<tbody>
<tr>
<td>Revision Type</td>
<td>PR_BASE</td>
</tr>
<tr>
<td>Snapshot</td>
<td>synthesized</td>
</tr>
<tr>
<td>Version</td>
<td>18.1.0 Pro Edition</td>
</tr>
<tr>
<td>Version-Compatible</td>
<td>Yes</td>
</tr>
</tbody>
</table>

For synthesized snapshot partition lists data from the **Synthesis Resource Usage Summary** report.

- Average fan-out: 1.6
- Dedicated logic registers: 14
- Estimate of Logic utilization: 1
- I/O pins: 35
- Maximum fan-out: 2
- Maximum fan-out node: counter[23]
- Total DSP Blocks: 0
- Total fan-out: 6

For the final snapshot partition, lists data from the **Fitter Partition Statistics** report.

- Average fan-out: 1.6
- Combinational ALUTs: 16
- I/O Registers
- M20Ks

---

#### 2.7.7. Clearing Compilation Results

You can clean the project database if you want to remove prior compilation results for all project revisions or for specific revisions. For example, you must clear previous compilation results before importing a version-compatible database to an existing project.

1. Click **Project > Clean Project**.
2. Select **All revisions** to clear the databases for all revisions of the current project, or specify a **Revision name** to clear only the revision’s database you specify.
3. Click **OK**. A message indicates when the database is clean.

**Figure 27. Clean Project Dialog Box Cleans the Project Database**
2.8. Migrating Projects Across Operating Systems

Consider the following cross-platform issues when moving your project from one operating system to another (for example, from Windows* to Linux*).

2.8.1. Migrating Design Files and Libraries

Consider file naming differences when migrating projects across operating systems.

- Use appropriate case for your platform in file path references.
- Use a character set common to both platforms.
- Do not change the forward-slash (/) and back-slash (\) path separators in the .qsf. The Intel Quartus Prime software automatically changes all back-slash (\) path separators to forward-slashes (/) in the .qsf.
- Observe the target platform’s file name length limit.
- Use underscore instead of spaces in file and directory names.
- Change library absolute path references to relative paths in the .qsf.
- Ensure that any external project library exists in the new platform’s file system.
- Specify file and directory paths as relative to the project directory. For example, for a project titled foo_design, specify the source files as: top.v, foo_folder /foo1.v, foo_folder /foo2.v, and foo_folder/bar_folder/bar1.vhdl.
- Ensure that all the subdirectories are in the same hierarchical structure and relative path as in the original platform.

Figure 28. All Inclusive Project Directory Structure

2.8.1.1. Use Relative Paths

Express file paths using relative path notation (../).

For example, in the directory structure shown you can specify top.v as ../source/top.v and foo1.v as ../source/foo_folder/foo1.v.
2.8.2. Design Library Migration Guidelines

The following guidelines apply to library migration across computing platforms:

1. The project directory takes precedence over the project libraries.
2. For Linux, the Intel Quartus Prime software creates the file in the `altera.quartus` directory under the `<home>` directory.
3. All library files are relative to the libraries. For example, if you specify the `user_lib1` directory as a project library and you want to add the `/user_lib1/foo1.v` file to the library, you can specify the `foo1.v` file in the `.qsf` as `foo1.v`. The Intel Quartus Prime software includes files in specified libraries.
4. If the directory is outside of the project directory, an absolute path is created by default. Change the absolute path to a relative path before migration.
5. When copying projects that include libraries, you must either copy your project library files along with the project directory or ensure that your project library files exist in the target platform.
   - On Windows, the Intel Quartus Prime software searches for the `quartus2.ini` file in the following directories and order:
     - USERPROFILE, for example, C:\Documents and Settings\<user name>
     - Directory specified by the TMP environmental variable
     - Directory specified by the TEMP environmental variable
     - Root directory, for example, C:\

2.9. Archiving Projects

You can optionally save the elements of a project in a single, compressed Intel Quartus Prime Archive File (.qar) by clicking **Project > Archive Project**. The .qar preserves logic design, project, and settings files required to restore the project.
Use this technique to share projects between designers, or to transfer your project to a new version of the Intel Quartus Prime software, or to Intel support. Optionally add compilation results, Platform Designer system files, and third-party EDA tool files to the archive.

**Related Information**

Project Archive Commands on page 39

### 2.9.1. Manually Adding Files To Archives

Follow these steps to add files to a project archive manually:

1. Click **Project ➤ Archive Project** and specify the archive file name.
2. Click **Advanced**.
3. Select the **File set** for archive or select **Custom**. Turn on **File subsets** for the archive.
4. Click **Add** and select Platform Designer system or EDA tool files. Click **OK**.
5. Click **Archive**.

### 2.9.2. Archiving Projects for Service Requests

When archiving projects for a service request, include all needed file types for proper debugging by customer support.

To identify and include appropriate archive files for an Intel service request:

1. Click **Project > Archive Project** and specify the archive file name.
2. Click **Advanced**.
3. In **File set**, select **Service request** to include files for Intel Support.
   - Project source and setting files (.v, .vhd, .vqm, .qsf, .sdc, .qip, .qpf, .cmp)
   - Automatically detected source files (various)
   - Programming output files (.jdi, .sof, .pof)
   - Report files (.rpt, .pin, .summary, .smsg)
4. Click **OK**, and then click **Archive**.
2.9.3. Using External Revision Control

Your project may involve different team members with distributed responsibilities, such as sub-module design, device and system integration, simulation, and timing closure. In such cases, it may be useful to track and protect file revisions in an external revision control system.

While Intel Quartus Prime project revisions preserve various project setting and constraint combinations, external revision control systems can also track and merge RTL source code, simulation testbenches, and build scripts. External revision control supports design file version experimentation through branching and merging different versions of source code from multiple designers. Refer to your external revision control documentation for setup information.

2.9.3.1. Files to Include In External Revision Control

Include the following project file types in external revision control systems:

- Logic design files (.v, .vdh, .bdf, .edf, .vqm)
- Timing constraint files (.sdc)
- Quartus project settings and constraints (.qdf, .qpf, .qsf)
• IP files (.ip, .v, .sv, .vhd, .qip, .sip, .qsys)
• Platform Designer-generated files (.qsys, .ip, .sip)
• EDA tool files (.vo, .vho)

Generate or modify these files manually if you use a scripted design flow. If you use an external source code control system, check-in project files anytime you modify assignments and settings.

2.10. Command-Line Interface

You can optionally use command-line executables or scripts to run project commands, rather than using the GUI. This technique can be helpful if you have many settings and wish to track them in a single file or spreadsheet for iterative comparison. The .qsf supports only a limited subset of Tcl commands. Therefore, pass settings and constraints using a Tcl script:

1. Create a text file with the extension .tcl that contains your assignments in Tcl format.
2. Source the Tcl script file by adding the following line to the .qsf:

   set_global_assignment -name SOURCE_TCL_SCRIPT_FILE <filename>.

2.10.1. Project Revision Commands

create_revision Command

create_revision defines the properties of a new project revision.

create_revision <name> -based_on <revision_name> -set_current -new_rev_type \\
<rev_type> -root_partition_qdb_file <root_qdb>

Table 7. create_revision Command Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>based_on (optional)</td>
<td>Specifies the revision name on which the new revision bases its settings.</td>
</tr>
<tr>
<td>set_current (optional)</td>
<td>Sets the new revision as the current revision.</td>
</tr>
<tr>
<td>-new_rev_type</td>
<td>Specifies a base or impl (implementation) type for a new revision.</td>
</tr>
<tr>
<td>root_partition_qdb_file</td>
<td>Specifies the name of a static region .qdb if already known when creating a revision.</td>
</tr>
</tbody>
</table>

get_project_revisions Command

get_project_revisions returns a list of all revisions in the project.

get_project_revisions <project_name>

delete_revision Command

delete_revision deletes the revision you specify from your project.

deadle_revision <revision name>
set_current_revision Command

set_current_revision sets the revision you specify as the current revision.

set_current_revision -force <revision name>

Related Information
Optimize Settings with Project Revisions on page 20

2.10.2. Project Archive Commands

project_archive Command

project_archive archives your project into a single, compressed .qar file.

project_archive <name>.qar

Table 8. project_archive Command Options

<table>
<thead>
<tr>
<th>Options</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-all_revisions</td>
<td>Includes all revisions of the current project in the archive.</td>
</tr>
<tr>
<td>-common_directory /&lt;name&gt;</td>
<td>Preserves original project directory structure in specified subdirectory.</td>
</tr>
<tr>
<td>-include_libraries</td>
<td>Includes libraries in archive.</td>
</tr>
<tr>
<td>-include_outputs</td>
<td>Includes output files in archive.</td>
</tr>
<tr>
<td>-use_file_set &lt;file_set&gt;</td>
<td>Includes specified fileset in archive.</td>
</tr>
<tr>
<td>-version_compatible_database</td>
<td>Includes version-compatible database files in archive.</td>
</tr>
</tbody>
</table>

restore_archive Command

Restores an archived project to a destination directory with optional overwriting of current contents.

project_restore <name>.qar -destination <directory name> -overwrite

Related Information
Archiving Projects on page 35

2.10.3. Project Database Commands

export_database Command

export_design exports the specified project database to the .qdb file you specify.

These commands require the quartus_cdb executable.

quartus_cdb <revision name> --export_design --file <file name>.qdb \   --snapshot <synthesized/final>
import_database Command

import_design imports the specified project database to the .qdb file you specify.

quartus_cdb <revision name> --import_design --file <file name>.qdb

export_block Command

export_block exports the specified partition database to the .qdb file you specify.

quartus_cdb -r <project name> -c <revision name> --export_block \
--partition_name <partition name> --snapshot <name> --file <file name>.qdb

2.10.3.1. quartus_cdb Executables to Manage Version-Compatible Databases

The command-line arguments to the quartus_cdb executable in the Quartus Prime Pro software are export_design and import_design. The exported version-compatible design files are archived in a file (with a .qdb extension). This differs from the Intel Quartus Prime Standard Edition software, which writes all files to a directory.

In the Intel Quartus Prime Standard Edition software, the flow exports both post-map and post-fit databases. In the Intel Quartus Prime Pro Edition software, the export command requires the snapshot argument to indicate the target snapshot to export. If the specified snapshot has not been compiled, the flow exits with an error. In ACDS 16.0, export is limited to “synthesized” and “final” snapshots.

quartus_cdb <project_name> [-c <revision_name>] --export_design 
--snapshot <snapshot_name> --file <filename>.qdb

The import command takes the exported *.qdb file and the project to which you want to import the design.

quartus_cdb <project_name> [-c <revision_name>] --import_design 
--file <archive>.qdb [--overwrite] [--timing_analysis_mode]

The --timing_analysis_mode option is only available for Intel Arria 10 designs. The option disables legality checks for certain configuration rules that may have changed from prior versions of the Intel Quartus Prime software. Use this option only if you cannot successfully import your design without it. After you have imported a design in timing analysis mode, you cannot use it to generate programming files.

2.11. Managing Projects Revision History

<table>
<thead>
<tr>
<th>Document Version</th>
<th>Intel Quartus Prime Version</th>
<th>Changes</th>
</tr>
</thead>
</table>
| 2018.09.24       | 18.1.0                     | • Subdivided "Exporting, Archiving, and Migrating Projects" into separate sections.  
                     • Described migration of full chip database in "Exporting a Version-Compatible Compilation Database" topic.  
                     • Described automated .qdb partition export in "Exporting a Design Partition" topic.  
                     • Added "Viewing Quartus Database File Information" topic.  
                     • Added "Specifying the Target Device or Board" topic. 

continued...
## Changes

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
</tr>
</thead>
</table>
| 2018.05.07 | 18.0.0  | - Initial release as chapter of Getting Started User Guide.  
- Revised "Exporting a Design Partition" topic to add Include entity-bound SDC files for the selected partition option, to add prerequisite steps, and to remove import step covered in separate topic.  
- Changed title of "Managing Team-Based Designs" to "Exporting, Archiving, and Migrating Projects" and updated content.  
- Changed title of "Migrating Compilation Results Across Software Versions" to "Exporting the Compilation Database" and updated content.  
- Changed title of "Exporting the Results Database" to "Exporting a Version-Compatible Design Compilation Database" and updated content.  
- Changed title of "Importing the Results Database" to "Importing a Version-Compatible Design Compilation Database" and updated content.  
- Changed title of "Cleaning the Project Database" to "Cleaning the Project Compilation Database."  
- Updated screenshots of IP Catalog and Parameter Editor for latest IP names. |
| 2017.11.06 | 17.1.0  | - Revised product branding for Intel standards.  
- Revised topics on Intel FPGA IP Evaluation Mode (formerly OpenCore).  
- Removed `-compatible` attribute from `export_design` command content.  
- Updated figure: IP Upgrade Alert in Project Navigator.  
- Updated IP Core Upgrade Status table with new icons, and added row for IP Component Outdated status. |
| 2017.05.08 | 17.0.0  | - Added Project Tasks pane and update New Project Wizard.  
- Updated Compilation Dashboard image to show concurrent analysis.  
- Removed Smart Compilation option from Settings dialog box screenshot.  
- Updated IP Catalog screenshots for latest GUIs.  
- Added topic on Back-Annotate Assignments command.  
- Added Exporting a Design Partition topic.  
- Removed mentions to deprecated Incremental Compilation.  
- Added reference to Block-Level Design Flows. |
| 2016.10.31 | 16.1.0  | - Added references to compilation stages and snapshots.  
- Removed support for comparing revisions.  
- Added references to `.ip` file creation during Intel Quartus Prime Pro Edition stand-alone IP generation.  
- Updated IP Core Generation Output files list and diagram.  
- Added Support for IP Core Encryption topic.  
- Rebranding for Intel continued... |
<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
</tr>
</thead>
</table>
| 2016.05.03  | 16.0.0  | • Removed statements about serial equivalence when using multiple processors.  
• Added the "Preserving Compilation Results" section.  
• Added the "Migrating Results Across Quartus Prime Software" section and its subsections for information about importing and exporting compilation results between different versions of Quartus Prime.  
• Added the "Project Database Commands" section and its subsections. |
| 2016.02.09  | 15.1.1  | • Clarified instructions for Generating a Combined Simulator Setup Script.  
• Clarified location of [Save project output files in specified directory](#) option. |
| 2015.11.02  | 15.1.0  | • Added Generating Version-Independent IP Simulation Scripts topic.  
• Added example IP simulation script templates for supported simulators.  
• Added Incorporating IP Simulation Scripts in Top-Level Scripts topic.  
• Added Troubleshooting IP Upgrade topic.  
• Updated IP Catalog and parameter editor descriptions for GUI changes.  
• Updated IP upgrade and migration steps for latest GUI changes.  
• Updated Generating IP Cores process for GUI changes.  
• Updated Files Generated for IP Cores and Qsys system description.  
• Removed references to devices and features not supported in version 15.1.  
• Changed instances of Quartus II to Intel Quartus Prime. |
| 2015.05.04  | 15.0.0  | • Added description of design templates feature.  
• Updated screenshot for DSE II GUI.  
• Added qsys_script IP core instantiation information.  
• Described changes to generating and processing of instance and entity names.  
• Added description of upgrading IP cores at the command line.  
• Updated procedures for upgrading and migrating IP cores.  
• Gate level timing simulation supported only for Cyclone IV and Stratix IV devices. |
| 2014.12.15  | 14.1.0  | • Updated content for DSE II GUI and optimizations.  
• Added information about new Assignments ➤ Settings ➤ IP Settings that control frequency of synthesis file regeneration and automatic addition of IP files to the project. |
| 2014.08.18  | 14.0a10.0  | • Added information about specifying parameters for IP cores targeting Arria 10 devices.  
• Added information about the latest IP output for version 14.0a10 targeting Arria 10 devices.  
• Added information about individual migration of IP cores to the latest devices.  
• Added information about editing existing IP variations. |
| 2014.06.30  | 14.0.0  | • Replaced MegaWizard Plug-In Manager information with IP Catalog.  
• Added standard information about upgrading IP cores.  
• Added standard installation and licensing information.  
• Removed outdated device support level information. IP core device support is now available in IP Catalog and parameter editor. |
| November 2013 | 13.1.0  | • Conversion to DITA format |
| May 2013    | 13.0.0  | • Overhaul for improved usability and updated information. |
## Related Information

### Documentation Archive

For previous versions of the *Intel Quartus Prime Handbook*, search the documentation archives.

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>June 2012</td>
<td>12.0.0</td>
<td>• Removed survey link.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Updated information about <code>VERILOG_INCLUDE_FILE</code>.</td>
</tr>
<tr>
<td>November 2011</td>
<td>10.1.1</td>
<td>Template update.</td>
</tr>
<tr>
<td>December 2010</td>
<td>10.1.0</td>
<td>• Changed to new document template.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Removed Figure 4–1, Figure 4–6, Table 4–2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Moved &quot;Hiding Messages&quot; to Help.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Removed references about the <code>set_user_option</code> command.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Removed Classic Timing Analyzer references.</td>
</tr>
</tbody>
</table>
3. Design Planning

3.1. Design Planning

Design planning is an essential step in advanced FPGA design. System architects must consider the target device characteristics in order to plan for interface I/O, integration of IP, on-chip debugging tools, and use of other EDA tools. Designers must consider device power consumption and programming methods when planning the layout. You can solve potential problems early in the design cycle by following the design planning considerations in this chapter.

By default, the Intel Quartus Prime software optimizes designs for the best overall results; however, you can adjust settings to better optimize one aspect of your design, such as performance, routability, area, or power utilization. Consider your own design priorities and trade-offs when reviewing the techniques in this chapter. For example, certain device features, density, and performance requirements can increase system cost. Signal integrity and board issues can impact I/O pin locations. Power, timing performance, and area utilization all affect one another. Compilation time is affected when optimizing these priorities.

Determining your design priorities early on helps you to choose the best device, tools, features, and methodologies for your design.

3.2. Create a Design Specification and Test Plan

Before you create your design logic or complete your system design, it is best practice to create detailed design specifications that define the system, specify the I/O interfaces for the FPGA, identify the different clock domains, and include a block diagram of basic design functions.

In addition, creating a test plan helps you to design for verification and ease of manufacture. For example, your test plan can include validation of interfaces incorporated in your design. To perform any built-in self-test functions to drive interfaces, you can use a UART interface with a Nios® II processor inside the FPGA device.

If more than one designer contributes to the design, consider a common design directory structure or source control system to make design integration easier. Consider whether you want to standardize on an interface protocol for each design block.

3.3. Plan for the Target Device

Intel offers a broad portfolio of FPGA and PLD devices. The Intel device that you select determines factors of performance, density, and board layout. To avoid costly design changes, it is best to carefully consider and determine the target device family early in
the design cycle. Intel FPGA device families differ in cost, size, density, performance, power consumption, packaging, I/O standards, and other factors. Select the device family that best suits your most critical design requirements.

**Device Family Selection Guidelines**

- Refer to the Product Selector tool on the Intel website to quickly find and compare the specifications and features of Intel FPGA devices and development kits.
- Once you identify the target device family, refer to the device family technical documentation for detailed device characteristics. Each device family includes complete documentation, including a datasheet and user guide or handbook. You can also view a summary of each device’s resources by selecting a device in the **Device** dialog box (Assignments ➤ Device)

**Figure 31. Device Dialog Box**

- Consider whether the device family meets any requirements you have for high-speed transceivers, global or regional clock networks, and the number of phase-locked loops (PLLs)
- Consider the density requirements of your design. Devices with more logic resources and higher I/O counts can implement larger and more complex designs, but at a higher cost. Smaller devices use lower static power. Select a device larger than what your design requires if you may want to add more logic later in the design cycle, or to reserve logic and memory for on-chip debugging.
- Consider requirements for types of dedicated logic blocks, such as memory blocks of different sizes, or digital signal processing (DSP) blocks to implement certain arithmetic functions.

**Related Information**

Product Selector Guide Tool
To help you choose your device.
3.3.1. Device Migration Planning

Determine whether you want to migrate your design to another device density to allow flexibility when your design nears completion. You may want to target a smaller (and less expensive) device and then move to a larger device if necessary to meet your design requirements. Other designers may prototype their design in a larger device to reduce optimization time and achieve timing closure more quickly, and then migrate to a smaller device after prototyping. If you want the flexibility to migrate your design, you must specify these migration options in the Intel Quartus Prime software at the beginning of your design cycle.

Selecting a migration device impacts pin placement because some pins may serve different functions in different device densities or package sizes. If you make pin assignments in the Intel Quartus Prime software, the Pin Migration View in the Pin Planner highlights pins that change function between your migration devices.

3.4. Plan for Intellectual Property Cores

Intel and third-party intellectual property (IP) partners offer a large selection of standardized IP cores optimized for Intel FPGA devices. The IP you select often affects system design and performance, especially if the FPGA interfaces with other devices in the system. Plan which I/O interfaces or other blocks in the system that you want to implement using IP cores. Whenever possible, plan to incorporate these functions into your design using Intel FPGA IP cores, many of which are available for production use in the Intel Quartus Prime software without additional license.

Figure 32. IP Catalog

For IP cores that require additional license for production use, the Intel FPGA IP Evaluation Mode, allows you to program the FPGA to verify the IP in the hardware before you purchase the IP license. Refer to Introduction to Intel FPGA IP Cores on page 60 for general information on using Intel FPGA IP cores.
3.5. Plan for Standard Interfaces

To reduce design iterations and costly design changes, plan for use of standard interfaces in system design. Using standard interfaces ensures compatibility between design blocks from different design teams or vendors.

You can use the Intel Quartus Prime Interface Planner to help you accurately plan constraints for design implementation. Use Interface Planner to prototype interface implementations and rapidly define a legal device floorplan. Standard interfaces simplify the interface logic to each design block, and enable individual team members to test their individual design blocks against the specification for the interface protocol to ease system integration.

You can use the Intel Quartus Prime Platform Designer system integration tool to use standard interfaces and speed-up system-level integration. Platform Designer components use Avalon® standard interfaces for physical connections, allowing you to connect any logical device (either on-chip or off-chip) that has an Avalon interface. Platform Designer allows you to define system components in a GUI, and then automatically generates the required interconnect logic, along with clock-crossing and width adapters.

The Avalon standard includes two interface types:

- Avalon Memory-Mapped (Avalon-MM)—allow a component to use an address-mapped read or write protocol that connects master components to slave components.
- Avalon Streaming (Avalon-ST)—enables point-to-point connections between streaming components that send and receive data using a high-speed, unidirectional system interconnect between source and sink ports.

Related Information
Creating a System with Platform Designer

3.6. Plan for Device Programming

You must plan for the devices and hardware that you require for programming or configuration of the device. Comprehensive system planning includes determining what companion devices, if any, your system requires. Your programming or configuration method also impacts the board layout planning. For example, some programming options require a JTAG interface connection, requiring a JTAG chain on the board.

You can define a configuration scheme on the Configuration tab of the Device and Pin Options dialog box. The Intel Quartus Prime software uses the settings for the configuration scheme, configuration device, and configuration device voltage to enable the appropriate dual purpose pins as regular I/O pins after you complete configuration. The Intel Quartus Prime software performs voltage compatibility checks of those pins during compilation of your design.
The technical documentation for each device family describes the available configuration options.

### 3.7. Plan for Device Power Consumption

You can use the Intel Quartus Prime power estimation and analysis tools to estimate power consumption and guide PCB board and system design. You must accurately estimate device power consumption to develop an appropriate power budget and to design the power supplies, voltage regulators, heat sink, and cooling system. You can use the Early Power Estimator (EPE) spreadsheet to estimate power consumption before running a compilation or creating any source code. Then, you can use the Intel Quartus Prime Power Analyzer to perform a more accurate analysis after your design is complete.

**Note:**
Because power consumption is heavily dependent on actual design and environmental conditions, make sure to verify the actual power consumption during device operation.

Power estimation and analysis helps you ensure that your design satisfies thermal and power supply requirements:
- **Thermal**—ensure that the cooling solution is sufficient to dissipate the heat generated by the device. The computed junction temperature must fall within normal device specifications.
- **Power supply**—ensure that the power supplies provide adequate current to support device operation.
Early Power Estimator (EPE) Spreadsheet

The Early Power Estimator (EPE) spreadsheet allows you to estimate power utilization for your design. Estimating power consumption early in the design cycle allows planning of power budgets and avoids unexpected results when designing the PCB.

Figure 34. Early Power Estimator (EPE) Spreadsheet

You can manually enter data into the EPE spreadsheet, or use the Intel Quartus Prime software to generate device resource information for your design.

To manually enter data into the EPE spreadsheet, enter the device resources, operating frequency, toggle rates, and other parameters for your design. If you do not have an existing design, estimate the number of device resources used in your design, and then enter the data into the EPE spreadsheet manually.

If you have an existing design or a partially completed design, you can use the Intel Quartus Prime software to generate the Early Power Estimator File (.txt, .csv) to assist you in completing the EPE spreadsheet.

The EPE spreadsheet includes the Import Data macro that parses the information in the EPE File and transfers the information into the spreadsheet. If you do not want to use the macro, you can manually transfer the data into the EPE spreadsheet. For example, after importing the EPE File information into the EPE spreadsheet, you can add device resource information. If the existing Intel Quartus Prime project represents only a portion of your full design, manually enter the additional device resources you use in the final design.
Intel Quartus Prime Power Analyzer

After you complete your design, you can use the Intel Quartus Prime Power Analyzer to perform a complete post-fit power analysis to check the power consumption more accurately. The Power Analyzer provides an accurate estimation of power, ensuring that thermal and supply limitations are met.

Figure 35. Intel Quartus Prime Power Analyzer

Related Information
- Early Power Estimator and Power Analyzer Web Page

3.8. Plan for Interface I/O Pins

In many design environments, FPGA designers want to plan the top-level FPGA I/O pins early to help board designers begin the PCB design and layout. The I/O capabilities and board layout guidelines of the FPGA device influence pin locations and other types of assignments. If the board design team specifies an FPGA pin-out, the pin locations must be verified in the FPGA placement and routing software to avoid board design changes.

You can create a preliminary pin-out for an Intel FPGA with the Intel Quartus Prime Pin Planner before you develop the source code, based on standard I/O interfaces (such as memory and bus interfaces) and any other I/O requirements for your system.
The Intel Quartus Prime I/O Assignment Analysis checks that the pin locations and assignments are supported in the target FPGA architecture. You can then use I/O Assignment Analysis to validate I/O-related assignments that you create or modify throughout the design process. When you compile your design in the Intel Quartus Prime software, I/O Assignment Analysis runs automatically in the Fitter to validate that the assignments meet all the device requirements and generates error messages.

Early in the design process, before creating the source code, the system architect has information about the standard I/O interfaces (such as memory and bus interfaces), the IP cores in your design, and any other I/O-related assignments defined by system requirements. You can use this information with the Early Pin Planning feature in the Pin Planner to specify details about the design I/O interfaces. You can then create a top-level design file that includes all I/O information.

The Pin Planner interfaces with the IP core parameter editor, which allows you to create or import custom IP cores that use I/O interfaces. You can configure how to connect the functions and cores to each other by specifying matching node names for selected ports. You can create other I/O-related assignments for these interfaces or other design I/O pins in the Pin Planner, as described in this section. The Pin Planner creates virtual pin assignments for internal nodes, so internal nodes are not assigned to device pins during compilation.

You can use the I/O analysis results to change pin assignments or IP parameters even before you create your design, and repeat the checking process until the I/O interface meets your design requirements and passes the pin checks in the Intel Quartus Prime software. When you complete initial pin planning, you can create a revision based on
the Intel Quartus Prime-generated netlist. You can then use the generated netlist to
develop the top-level design file for your design, or disregard the generated netlist
and use the generated Intel Quartus Prime Settings File (.qsf) with your design.

During this early pin planning, after you have generated a top-level design file, or
when you have developed your design source code, you can assign pin locations and
assignments with the Pin Planner.

With the Pin Planner, you can identify I/O banks, voltage reference (VREF) groups, and
differential pin pairings to help you through the I/O planning process. If you selected a
migration device, the Pin Migration View highlights the pins that have changed
functions in the migration device when compared to the currently selected device.
Selecting the pins in the Device Migration view cross-probes to the rest of the Pin
Planner, so that you can use device migration information when planning your pin
assignments. You can also configure board trace models of selected pins for use in
“board-aware” signal integrity reports generated with the Enable Advanced I/O
Timing option. This option ensures that you get accurate I/O timing analysis. You can
use a Microsoft Excel spreadsheet to start the I/O planning process if you normally use
a spreadsheet in your design flow, and you can export a Comma-Separated Value File
(.csv) containing your I/O assignments for spreadsheet use when you assign all pins.

When you complete your pin planning, you can pass pin location information to PCB
designers. The Pin Planner is tightly integrated with certain PCB design EDA tools, and
can read pin location changes from these tools to check suggested changes. Your pin
assignments must match between the Intel Quartus Prime software and your
schematic and board layout tools to ensure the FPGA works correctly on the board,
especially if you must make changes to the pin-out. The system architect uses the
Intel Quartus Prime software to pass pin information to team members designing
individual logic blocks, allowing them to achieve better timing closure when they
compile their design.

Start FPGA planning before you complete the HDL for your design to improve the
confidence in early board layouts, reduce the chance of error, and improve the overall
time to market of the design. When you complete your design, use the Fitter reports
for the final sign-off of pin assignments. After compilation, the Intel Quartus Prime
software generates the Pin-Out File (.pin), and you can use this file to verify that
each pin is correctly connected in board schematics.

Related Information
For more information about I/O assignment and analysis.

3.8.1. Simultaneous Switching Noise Analysis

Simultaneous switching noise (SSN) is a noise voltage inducted onto a victim I/O pin
of a device due to the switching behavior of other aggressor I/O pins in the device.

Intel provides tools for SSN analysis and estimation, including SSN characterization
reports, an Early SSN Estimator (ESE) spreadsheet tool, and the SSN Analyzer in the
Intel Quartus Prime software. SSN often leads to the degradation of signal integrity by
causing signal distortion, thereby reducing the noise margin of a system. You must
address SSN with estimation early in your system design, to minimize later board
design changes. When your design is complete, verify your board design by
performing a complete SSN analysis of your FPGA in the Intel Quartus Prime software.
3.9. Plan for other EDA Tools

Your complete FPGA design flow may include third-party EDA tools in addition to the Intel Quartus Prime software. Determine which tools you want to use with the Intel Quartus Prime software to ensure that they are supported and set up properly, and that you are aware of their capabilities.

3.9.1. Third-Party Synthesis Tools

You can use supported standard third-party EDA synthesis tools to synthesize your Verilog HDL or VHDL design, and then compile the resulting output netlist file in the Intel Quartus Prime software.

Different synthesis tools may give different results for each design. To determine the best tool for your application, you can experiment by synthesizing typical designs for your application and coding style. Perform placement and routing in the Intel Quartus Prime software to get accurate timing analysis and logic utilization results.

The synthesis tool you choose may allow you to create an Intel Quartus Prime project and pass constraints, such as the EDA tool setting, device selection, and timing requirements that you specified in your synthesis project. You can save time when setting up your Intel Quartus Prime project for placement and routing.

Tool vendors frequently add new features, fix tool issues, and enhance performance for Intel devices, you must use the most recent version of third-party synthesis tools.

3.9.2. Third-Party Simulation Tools

Intel provides the Mentor Graphics ModelSim* - Intel FPGA Edition simulator with the Intel Quartus Prime software. You can also purchase the ModelSim - Intel FPGA Edition or a full license of the ModelSim software to support large designs and achieve faster simulation performance. The Intel Quartus Prime software generates both functional and timing netlist files for ModelSim and other supported third-party simulators.

Use the simulator version that your Intel Quartus Prime software version supports for best results. You must also use the model libraries provided with your Intel Quartus Prime software version. Libraries can change between versions, which might cause a mismatch with your simulation netlist.

Related Information

3.10. Plan for On-Chip Debugging Tools

Consider whether to include on-chip debugging tools early in the design process. Adding the debugging tools late in the design process can be more time consuming and error prone.
The Intel Quartus Prime in-system debugging tools offer different advantages and trade-offs, depending on the characteristics of your design. Consider the following debugging requirements when planning your design to support debugging tools:

- **JTAG connections**—required to perform in-system debugging with JTAG tools. Plan your system and board with JTAG ports that are available for debugging.
- **Additional logic resources (ALR)**—required to implement JTAG hub logic. If you set up the appropriate tool early in your design cycle, you can include these device resources in your early resource estimations to ensure that you do not overload the device with logic.
- **Reserve device memory**—required if your tool uses device memory to capture data during system operation. To ensure that you have enough memory resources to take advantage of this debugging technique, consider reserving device memory to use during debugging.
- **Reserve I/O pins**—required if you use the Logic Analyzer Interface (LAI), which require I/O pins for debugging. If you reserve I/O pins for debugging, you do not have to later change your design or board. The LAI can multiplex signals with design I/O pins if required. Ensure that your board supports a debugging mode, in which debugging signals do not affect system operation.
- **Instantiate an IP core in your HDL code**—required if your debugging tool uses an Intel FPGA IP core.
- **Instantiate the Signal Tap Logic Analyzer IP core**—required if you want to manually connect the Signal Tap Logic Analyzer to nodes in your design and ensure that the tapped node names do not change during synthesis.

### Table 9. Factors to Consider When Using Debugging Tools During Design Planning Stages

<table>
<thead>
<tr>
<th>Design Planning Factor</th>
<th>Signal Tap Logic Analyzer</th>
<th>System Console</th>
<th>In-System Memory Content Editor</th>
<th>Logic Analyzer Interface (LAI)</th>
<th>Signal Probe</th>
<th>In-System Sources and Probes</th>
<th>Virtual JTAG IP Core</th>
</tr>
</thead>
<tbody>
<tr>
<td>JTAG connections</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>—</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Additional logic resources</td>
<td>—</td>
<td>Yes</td>
<td>—</td>
<td>Yes</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Reserve device memory</td>
<td>Yes</td>
<td>Yes</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Yes</td>
</tr>
<tr>
<td>Reserve I/O pins</td>
<td>—</td>
<td>—</td>
<td>Yes</td>
<td>Yes</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Instantiate IP core in your HDL code</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>

### Related Information


### 3.11. Plan HDL Coding Styles

When you develop complex FPGA designs, design practices and coding styles have an enormous impact on the timing performance, logic utilization, and system reliability of your device.
3.11.1. Design Recommendations

Use synchronous design practices to consistently meet your design goals. Problems with asynchronous design techniques include reliance on propagation delays in a device, incomplete timing analysis, and possible glitches.

In a synchronous design, a clock signal triggers all events. When you meet all register timing requirements, a synchronous design behaves in a predictable and reliable manner for all process, voltage, and temperature (PVT) conditions. You can easily target synchronous designs to different device families or speed grades.

Clock signals have a large effect on the timing accuracy, performance, and reliability of your design. Problems with clock signals can cause functional and timing problems in your design. Use dedicated clock pins and clock routing for best results, and if you have PLLs in your target device, use the PLLs for clock inversion, multiplication, and division. For clock multiplexing and gating, use the dedicated clock control block or PLL clock switchover feature instead of combinational logic, if these features are available in your device. If you must use internally-generated clock signals, register the output of any combinational logic used as a clock signal to reduce glitches.

Consider the architecture of the device you choose so that you can use specific features in your design. For example, the control signals should use the dedicated control signals in the device architecture. Sometimes, you might need to limit the number of different control signals used in your design to achieve the best results.

3.11.2. Recommended HDL Coding Styles

HDL coding styles can have a significant effect on the quality of results for programmable logic designs.

If you design memory and DSP functions, you must understand the target architecture of your device so you can use the dedicated logic block sizes and configurations. Follow the coding guidelines for inferring Intel FPGA IP and targeting dedicated device hardware, such as memory and DSP blocks.

Related Information

3.11.3. Managing Metastability

Metastability problems can occur in digital design when a signal is transferred between circuitry in unrelated or asynchronous clock domains, because the designer cannot guarantee that the signal meets the setup and hold time requirements during the signal transfer.

Designers commonly use a synchronization chain to minimize the occurrence of metastable events. Ensure that your design accounts for synchronization between any asynchronous clock domains. Consider using a synchronizer chain of more than two registers for high-frequency clocks and frequently-toggling data signals to reduce the chance of a metastability failure.

You can use the Intel Quartus Prime software to analyze the average mean time between failures (MTBF) due to metastability when a design synchronizes asynchronous signals, and optimize your design to improve the metastability MTBF. The MTBF due to metastability is an estimate of the average time between instances...
when metastability could cause a design failure. A high MTBF (such as hundreds or thousands of years between metastability failures) indicates a more robust design. Determine an acceptable target MTBF given the context of your entire system and the fact that MTBF calculations are statistical estimates.

The Intel Quartus Prime software can help you determine whether you have enough synchronization registers in your design to produce a high enough MTBF at your clock and data frequencies.

**Related Information**

### 3.12. Plan for Hierarchical and Team-Based Designs

The Intel Quartus Prime Compiler supports hierarchical design methodologies to reduce design compilation times and preserve performance. In a flat compilation flow, the design hierarchy is flattened without design partitions. In block-based (hierarchical) flows, you can subdivide your design by creating design partitions.

Hierarchical flows allow you to isolate, optimize, and preserve compilation results for specific design blocks, but require more design planning to ensure effective results.

#### 3.12.1. Flat Compilation without Design Partitions

In a flat compilation flow without any design partitions, the Intel Quartus Prime software compiles the entire design in a “flat” netlist.

Although the source code may be hierarchical, the Compiler flattens and synthesizes all the design logic. Whenever you re-compile the project, the Compiler re-performs all available logic and placement optimizations on the entire design.

The flat compilation flow does not require any planning for design partitions. However, because the Intel Quartus Prime software recompiles the entire design whenever you change your design, flat design practices may require more overall compilation time for large designs. Additionally, you may find that the results for one part of the design change when you change a different part of your design. You can run **Rapid Recompile** to preserve portions of previous placement and routing in subsequent compilations. **Rapid Recompile** can reduce your compilation time in a flat or partitioned design when you make small changes to your design.

### 3.13. Design Planning Revision History

<table>
<thead>
<tr>
<th>Document Version</th>
<th>Intel Quartus Prime Version</th>
<th>Changes</th>
</tr>
</thead>
</table>
| 2018.09.24       | 18.1.0                      | • Moved information about specifying the target board to "Specifying the Target Device or Board" in Managing Projects chapter.  
• Retitled "Creating Design Specifications" to "Create a Design Specification and Test Plan."  
• Retitled "Selecting Intellectual Property Cores" to "Plan for Intellectual Property Cores."  
• Retitled "Using Standard Interfaces" to "Plan for Standard Interfaces." Corrected references to Platform Designer. |

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<table>
<thead>
<tr>
<th>Document Version</th>
<th>Intel Quartus Prime Version</th>
<th>Changes</th>
</tr>
</thead>
</table>
|                 |                            | • Retitled "Device Selection" to "Plan for the Target Device."
|                 |                            | • Updated this content to correct Platform Designer names. |
|                 |                            | • Moved "Setting Pin Assignments" to Managing Projects chapter as "Generating Pin Assignments for a Target Board." |
|                 |                            | • Retitled "Estimating Power" to "Plan for Device Power Consumption." Reorganized this topic into sections for EPE and Power Analyzer. |
|                 |                            | • Added link to “Simulator Support, Third-Party Simulation User Guide” |
|                 |                            | • Retitled "Planning for Device Programming or Configuration" to "Plan for Device Programming" |
|                 |                            | • Retitled "Selecting Third-Party EDA Tools" to "Plan for other EDA Tools."
|                 |                            | • Retitled "Planning for On-Chip Debugging Tools" to "Plan for On-Chip Debugging Tools."
|                 |                            | • Retitled Design Planning with the Intel Quartus Prime Software to Design Planning |

2018.05.07  18.0  Initial release as separate chapter of Getting Started User Guide.

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>2017.11.06</td>
<td>17.1.0</td>
<td>• Changed instances of OpenCore Plus to Intel FPGA IP Evaluation Mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Changed instances of Qsys to Platform Designer (Standard)</td>
</tr>
<tr>
<td>2017.05.08</td>
<td>17.0.0</td>
<td>• Removed mentions to Integrated Synthesis.</td>
</tr>
<tr>
<td>2016.10.31</td>
<td>16.1.0</td>
<td>• Implemented Intel rebranding.</td>
</tr>
<tr>
<td>2016.05.03</td>
<td>16.0.0</td>
<td>• Added information about Development Kit selection.</td>
</tr>
<tr>
<td>2015.11.02</td>
<td>15.1.0</td>
<td>• Added references to Interface Planning chapter.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Changed instances of Quartus II to Intel Quartus Prime.</td>
</tr>
<tr>
<td>2015.05.04</td>
<td>15.0.0</td>
<td>• Remove support for Early Timing Estimate feature.</td>
</tr>
<tr>
<td>2014.06.30</td>
<td>14.0.0</td>
<td>• Updated document format.</td>
</tr>
<tr>
<td>November 2013</td>
<td>13.1.0</td>
<td>• Removed HardCopy device information.</td>
</tr>
<tr>
<td>November, 2012</td>
<td>12.1.0</td>
<td>• Update for changes to early pin planning feature</td>
</tr>
<tr>
<td>June 2012</td>
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<td>• Editorial update.</td>
</tr>
<tr>
<td>November 2011</td>
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<td>• Template update.</td>
</tr>
<tr>
<td>May 2011</td>
<td>11.0.0</td>
<td>• Added link to System Design with Qsys in &quot;Creating Design Specifications&quot; on page 1–2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Updated “Simultaneous Switching Noise Analysis” on page 1–8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Updated &quot;Planning for On-Chip Debugging Tools&quot; on page 1–10</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Removed information from &quot;Planning Design Partitions and Floorplan Location Assignments&quot; on page 1–15</td>
</tr>
</tbody>
</table>

December 2010  10.1.0  • Changed to new document template |
|                |         | • Updated “System Design and Standard Interfaces” on page 1–3 to include information about the Qsys system integration tool |
|                |         | • Added link to the Product Selector in "Device Selection" on page 1–3 |

continued...
<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>July 2010</td>
<td>10.0.0</td>
<td>• Converted information into new table (Table 1–1) in “Planning for On-Chip Debugging Options” on page 1–10</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Simplified description of incremental compilation usages in “Incremental Compilation with Design Partitions” on page 1–14</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added information about the Rapid Recompile option in “Flat Compilation Flow with No Design Partitions” on page 1–14</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Removed details and linked to Intel Quartus Prime Help in “Fast Synthesis and Early Timing Estimation” on page 1–16</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added new section “System Design” on page 1–3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Removed details about debugging tools from “Planning for On-Chip Debugging Options” on page 1–10 and referred to other handbook chapters for more information</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Updated information on recommended design flows in “Incremental Compilation with Design Partitions” on page 1–14 and removed “Single-Project Versus Multiple-Project Incremental Flows” heading</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Merged the “Planning Design Partitions” section with the “Creating a Design Floorplan” section. Changed heading title to “Planning Design Partitions and Floorplan Location Assignments” on page 1–15</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Removed ”Creating a Design Floorplan” section</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Removed ”Referenced Documents” section</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Minor updates throughout chapter</td>
</tr>
<tr>
<td>November 2009</td>
<td>9.1.0</td>
<td>• Added details to “Creating Design Specifications” on page 1–2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added details to “Intellectual Property Selection” on page 1–2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Updated information on “Device Selection” on page 1–3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added reference to “Device Migration Planning” on page 1–4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Removed information from “Planning for Device Programming or Configuration” on page 1–4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added details to “Early Power Estimation” on page 1–5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Updated information on “Early Pin Planning and I/O Analysis” on page 1–6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Updated information on “Creating a Top-Level Design File for I/O Analysis” on page 1–8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added new “Simultaneous Switching Noise Analysis” section</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Updated information on “Synthesis Tools” on page 1–9</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Updated information on “Simulation Tools” on page 1–9</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Updated information on “Planning for On-Chip Debugging Options” on page 1–10</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added new “Managing Metastability” section</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Changed heading title “Top-Down Versus Bottom-Up Incremental Flows” to “Single-Project Versus Multiple-Project Incremental Flows”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Updated information on “Creating a Design Floorplan” on page 1–18</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Updated information from “Fast Synthesis and Early Timing Estimation” on page 1–18</td>
</tr>
</tbody>
</table>

continued...
<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>March 2009</td>
<td>9.0.0</td>
<td>• No change to content</td>
</tr>
<tr>
<td>November 2008</td>
<td>8.1.0</td>
<td>• Changed to 8-1/2 x 11 page size. No change to content.</td>
</tr>
<tr>
<td>May 2008</td>
<td>8.0.0</td>
<td>• Organization changes</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added &quot;Creating Design Specifications&quot; section</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added reference to new details in the In-System Design Debugging section of volume 3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added more details to the &quot;Design Practices and HDL Coding Styles&quot; section</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added references to the new Best Practices for Incremental Compilation and Floorplan Assignments chapter</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added reference to the Intel Quartus Prime Language Templates</td>
</tr>
</tbody>
</table>

**Related Information**

**Documentation Archive**

For previous versions of the *Intel Quartus Prime Handbook*, search the documentation archives.
4. Introduction to Intel FPGA IP Cores

Intel and strategic IP partners offer a broad portfolio of configurable IP cores optimized for Intel FPGA devices.

The Intel Quartus Prime software installation includes the Intel FPGA IP library. Integrate optimized and verified Intel FPGA IP cores into your design to shorten design cycles and maximize performance. The Intel Quartus Prime software also supports integration of IP cores from other sources. Use the IP Catalog (Tools ➤ IP Catalog) to efficiently parameterize and generate synthesis and simulation files for your custom IP variation. The Intel FPGA IP library includes the following types of IP cores:

- Basic functions
- DSP functions
- Interface protocols
- Low power functions
- Memory interfaces and controllers
- Processors and peripherals

This document provides basic information about parameterizing, generating, upgrading, and simulating stand-alone IP cores in the Intel Quartus Prime software.

Figure 37. IP Catalog

![IP Catalog Diagram](image)
4.1. IP Catalog and Parameter Editor

The IP Catalog displays the IP cores available for your project, including Intel FPGA IP and other IP that you add to the IP Catalog search path. Use the following features of the IP Catalog to locate and customize an IP core:

- Filter IP Catalog to **Show IP for active device family** or **Show IP for all device families**. If you have no project open, select the **Device Family** in IP Catalog.
- Type in the Search field to locate any full or partial IP core name in IP Catalog.
- Right-click an IP core name in IP Catalog to display details about supported devices, to open the IP core's installation folder, and for links to IP documentation.
- Click **Search for Partner IP** to access partner IP information on the web.

The parameter editor prompts you to specify an IP variation name, optional ports, and output file generation options. The parameter editor generates a top-level Intel Quartus Prime IP file (.ip) for an IP variation in Intel Quartus Prime Pro Edition projects.

4.1.1. The Parameter Editor

The parameter editor helps you to configure IP core ports, parameters, and output file generation options. The basic parameter editor controls include the following:

- Use the **Presets** window to apply preset parameter values for specific applications (for select cores).
- Use the **Details** window to view port and parameter descriptions, and click links to documentation.
- Click **Generate ➤ Generate Testbench System** to generate a testbench system (for select cores).
- Click **Generate ➤ Generate Example Design** to generate an example design (for select cores).
- Click **Validate System Integrity** to validate a system's generic components against companion files. (Platform Designer systems only)
- Click **Sync All System Info** to validate a system's generic components against companion files. (Platform Designer systems only)

The IP Catalog is also available in Platform Designer (**View ➤ IP Catalog**). The Platform Designer IP Catalog includes exclusive system interconnect, video and image processing, and other system-level IP that are not available in the Intel Quartus Prime IP Catalog. Refer to **Creating a System with Platform Designer** or **Creating a System with Platform Designer** for information on use of IP in Platform Designer and Platform Designer, respectively.

**Related Information**

Creating a System with Platform Designer
4.1.2. Adding IP Components to IP Catalog

The IP Catalog automatically displays Intel FPGA IP and other IP components that have a corresponding _hw.tcl or .ipx file located in the project directory, in the default Intel Quartus Prime installation directory, or in the IP search path. You can optionally add your own custom or third-party IP component to IP Catalog by adding the component's _hw.tcl or .ipx file to the IP search path.

Follow these steps to add custom or third-party IP to the IP Catalog:

1. In the Intel Quartus Prime software, click Tools ➤ Options ➤ IP Search Path) to open the IP Search Path Options dialog box.

Figure 38. Specifying IP Search Locations

2. Click Add or Remove to add/remove a location that contains IP.

3. To refresh the IP Catalog, click Refresh IP Catalog in the Intel Quartus Prime Platform Designer, or click File ➤ Refresh System in Platform Designer.
4.1.3. IP General Settings

The following settings control how the Intel Quartus Prime software manages IP cores in a project:

Table 10. Location of IP Core General Settings in the Intel Quartus Prime Software

<table>
<thead>
<tr>
<th>Setting</th>
<th>Description</th>
<th>Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Platform Designer memory usage size</td>
<td>Increase if you experience slow processing for large systems, or for out of memory errors.</td>
<td>Tools ➤ Options ➤ IP Settings Or Tasks pane ➤ Settings ➤ IP Settings</td>
</tr>
<tr>
<td>IP generation HDL preference</td>
<td>The parameter editor generates the HDL you specify for IP variations.</td>
<td></td>
</tr>
<tr>
<td>IP Regeneration Policy</td>
<td>Controls when synthesis files regenerate for each IP variation. Typically, you <strong>Always regenerate synthesis files for IP cores</strong> after making changes to an IP variation.</td>
<td></td>
</tr>
<tr>
<td>Generate IP simulation model when generating IP</td>
<td>Enables automatic generation of simulation models every time you generate the IP.</td>
<td></td>
</tr>
<tr>
<td>Use available processors for parallel generation of Quartzus project IPs</td>
<td>Directs Platform Designer to generate IPs in parallel, using the number of processors that you specify in the Compilation Process Settings pane of the Intel Quartus Prime project settings.</td>
<td>Tools ➤ Options ➤ IP Catalog Search Locations Or Tasks pane ➤ Settings ➤ IP Catalog Search Locations</td>
</tr>
<tr>
<td>Additional project and global IP search locations. The Intel Quartus Prime software searches for IP cores in the project directory, in the Intel Quartus Prime installation directory, and in the IP search path.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
4.1.4. Installing and Licensing Intel FPGA IP Cores

The Intel Quartus Prime software installation includes the Intel FPGA IP library. This library provides many useful IP cores for your production use without the need for an additional license. Some Intel FPGA IP cores require purchase of a separate license for production use. The Intel FPGA IP Evaluation Mode allows you to evaluate these licensed Intel FPGA IP cores in simulation and hardware, before deciding to purchase a full production IP core license. You only need to purchase a full production license for licensed Intel IP cores after you complete hardware testing and are ready to use the IP in production.

The Intel Quartus Prime software installs IP cores in the following locations by default:

Figure 40. IP Core Installation Path

<table>
<thead>
<tr>
<th>Location</th>
<th>Software</th>
<th>Platform</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>&lt;drive&gt;:\intelFPGA_pro\quartus\ip\altera</code></td>
<td>Intel Quartus Prime Pro Edition</td>
<td>Windows</td>
</tr>
<tr>
<td><code>&lt;drive&gt;:\intelFPGA\quartus\ip\altera</code></td>
<td>Intel Quartus Prime Standard Edition</td>
<td>Windows</td>
</tr>
<tr>
<td><code>&lt;home directory&gt;:/intelFPGA_pro/quartus/ip/altera</code></td>
<td>Intel Quartus Prime Pro Edition</td>
<td>Linux</td>
</tr>
<tr>
<td><code>&lt;home directory&gt;:/intelFPGA/quartus/ip/altera</code></td>
<td>Intel Quartus Prime Standard Edition</td>
<td>Linux</td>
</tr>
</tbody>
</table>

Note: The Intel Quartus Prime software does not support spaces in the installation path.

4.1.5. Best Practices for Intel FPGA IP

Use the following best practices when working with Intel FPGA IP:
4.2. Generating IP Cores (Intel Quartus Prime Pro Edition)

Quickly configure Intel FPGA IP cores in the Intel Quartus Prime parameter editor. Double-click any component in the IP Catalog to launch the parameter editor. The parameter editor allows you to define a custom variation of the IP core. The parameter editor generates the IP variation synthesis and optional simulation files, and adds the .ip file representing the variation to your project automatically.
Follow these steps to locate, instantiate, and customize an IP core in the parameter editor:

1. Create or open an Intel Quartus Prime project (.qpf) to contain the instantiated IP variation.

2. In the IP Catalog (Tools > IP Catalog), locate and double-click the name of the IP core to customize. To locate a specific component, type some or all of the component’s name in the IP Catalog search box. The New IP Variation window appears.

3. Specify a top-level name for your custom IP variation. Do not include spaces in IP variation names or paths. The parameter editor saves the IP variation settings in a file named <your_ip>.ip. Click OK. The parameter editor appears.

Figure 41.  IP Parameter Editor (Intel Quartus Prime Pro Edition)

4. Set the parameter values in the parameter editor and view the block diagram for the component. The Parameterization Messages tab at the bottom displays any errors in IP parameters:
   - Optionally, select preset parameter values if provided for your IP core. Presets specify initial parameter values for specific applications.
   - Specify parameters defining the IP core functionality, port configurations, and device-specific features.
   - Specify options for processing the IP core files in other EDA tools.
   
   Note: Refer to your IP core user guide for information about specific IP core parameters.

5. Click Generate HDL. The Generation dialog box appears.
6. Specify output file generation options, and then click Generate. The synthesis and simulation files generate according to your specifications.

7. To generate a simulation testbench, click Generate ➤ Generate Testbench System. Specify testbench generation options, and then click Generate.

8. To generate an HDL instantiation template that you can copy and paste into your text editor, click Generate ➤ Show Instantiation Template.

9. Click Finish. Click Yes if prompted to add files representing the IP variation to your project.

10. After generating and instantiating your IP variation, make appropriate pin assignments to connect ports.

   Note: Some IP cores generate different HDL implementations according to the IP core parameters. The underlying RTL of these IP cores contains a unique hash code that prevents module name collisions between different variations of the IP core. This unique code remains consistent, given the same IP settings and software version during IP generation. This unique code can change if you edit the IP core's parameters or upgrade the IP core version. To avoid dependency on these unique codes in your simulation environment, refer to Generating a Combined Simulator Setup Script.

4.2.1. IP Core Generation Output (Intel Quartus Prime Pro Edition)

   The Intel Quartus Prime software generates the following output file structure for individual IP cores that are not part of a Platform Designer system.
Figure 42. Individual IP Core Generation Output (Intel Quartus Prime Pro Edition)

```
<Project Directory>
  <your_ip>.ip - Top-level IP variation file
  <your_ip> - IP core variation files
    <your_ip>.bsf - Block symbol schematic file
    <your_ip>.cmp - VHDL component declaration
    <your_ip>.ppf - XML I/O pin information file
    <your_ip>.qip - Lists files for IP core synthesis
    <your_ip>.spd - Simulation startup scripts
    <your_ip>_bb.v - Verilog HDL black box EDA synthesis file *
    <your_ip>__generation.rpt - IP generation report
    <your_ip>_inst.v or .vhd - Lists file for IP core synthesis
    <your_ip>.qgsimc - Simulation caching file (Platform Designer)
    <your_ip>.qgsynthc - Synthesis caching file (Platform Designer)
  sim - IP simulation files
    <your_ip>.v or .vhd - Top-level simulation file
    <simulator vendor> - Simulator setup scripts
    <simulator_setup_scripts>
  synth - IP synthesis files
    <your_ip>.v or .vhd - Top-level IP synthesis file
    <IP Submodule>_<version> - IP Submodule Library
      sim - IP submodule 1 simulation files
        <HDL files>
      synth - IP submodule 1 synthesis files
        <HDL files>
  <your_ip>_tb - IP testbench system *
    <your_testbench>_tb.qsys - testbench system file
  <your_ip>_tb - IP testbench files
    <your_testbench>_tb.csv or .spd - testbench file
  sim - IP testbench simulation files
```

* If supported and enabled for your IP core variation.

Table 12. Output Files of Intel FPGA IP Generation

<table>
<thead>
<tr>
<th>File Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;your_ip&gt;.ip</td>
<td>Top-level IP variation file that contains the parameterization of an IP core in your project. If the IP variation is part of a Platform Designer system, the parameter editor also generates a .qsys file.</td>
</tr>
<tr>
<td>&lt;your_ip&gt;.cmp</td>
<td>The VHDL Component Declaration (.cmp) file is a text file that contains local generic and port definitions that you use in VHDL design files.</td>
</tr>
<tr>
<td>&lt;your_ip&gt;__generation.rpt</td>
<td>IP or Platform Designer generation log file. Displays a summary of the messages during IP generation.</td>
</tr>
</tbody>
</table>

*continued...*
<table>
<thead>
<tr>
<th>File Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>&lt;your_ip&gt;.qgsimc</code></td>
<td>Simulation caching file that compares the <code>.qsys</code> and <code>.ip</code> files with the current parameterization of the Platform Designer system and IP core. This comparison determines if Platform Designer can skip regeneration of the HDL.</td>
</tr>
<tr>
<td><code>&lt;your_ip&gt;.qgsynth</code></td>
<td>Synthesis caching file that compares the <code>.qsys</code> and <code>.ip</code> files with the current parameterization of the Platform Designer system and IP core. This comparison determines if Platform Designer can skip regeneration of the HDL.</td>
</tr>
<tr>
<td><code>&lt;your_ip&gt;.csv</code></td>
<td>Contains information about the upgrade status of the IP component.</td>
</tr>
<tr>
<td><code>&lt;your_ip&gt;.bsf</code></td>
<td>A symbol representation of the IP variation for use in Block Diagram Files (.bdf).</td>
</tr>
<tr>
<td><code>&lt;your_ip&gt;.spd</code></td>
<td>Input file that <code>ip-make-simscript</code> requires to generate simulation scripts. The .spd file contains a list of files you generate for simulation, along with information about memories that you initialize.</td>
</tr>
<tr>
<td><code>&lt;your_ip&gt;.ppf</code></td>
<td>The Pin Planner File (.ppf) stores the port and node assignments for IP components you create for use with the Pin Planner.</td>
</tr>
<tr>
<td><code>&lt;your_ip&gt;_bb.v</code></td>
<td>Use the Verilog blackbox (_bb.v) file as an empty module declaration for use as a blackbox.</td>
</tr>
<tr>
<td><code>&lt;your_ip&gt;_inst.v</code></td>
<td>HDL example instantiation template. Copy and paste the contents of this file into your HDL file to instantiate the IP variation.</td>
</tr>
<tr>
<td><code>&lt;your_ip&gt;.regmap</code></td>
<td>If the IP contains register information, the Intel Quartus Prime software generates the .regmap file. The .regmap file describes the register map information of master and slave interfaces. This file complements the .sopcinfo file by providing more detailed register information about the system. This file enables register display views and user customizable statistics in System Console.</td>
</tr>
<tr>
<td><code>&lt;your_ip&gt;.svd</code></td>
<td>Allows HPS System Debug tools to view the register maps of peripherals that connect to HPS within a Platform Designer system.</td>
</tr>
<tr>
<td><code>&lt;your_ip&gt;.v</code></td>
<td>HDL files that instantiate each submodule or child IP core for synthesis or simulation.</td>
</tr>
<tr>
<td><code>&lt;your_ip&gt;.vhd</code></td>
<td></td>
</tr>
<tr>
<td><code>mentor/</code></td>
<td>Contains a msim_setup.tcl script to set up and run a ModelSim simulation.</td>
</tr>
<tr>
<td><code>aldec/</code></td>
<td>Contains a Riviera-PRO* script rivierapro_setup.tcl to set up and run a simulation.</td>
</tr>
<tr>
<td><code>/synopsys/vcs</code></td>
<td>Contains a shell script vcs_setup.sh to set up and run a VCS* simulation.</td>
</tr>
<tr>
<td><code>/synopsys/vcsmx</code></td>
<td>Contains a shell script vcsmx_setup.sh and synopsys_sim.setup file to set up and run a VCS MX simulation.</td>
</tr>
<tr>
<td><code>/cadence</code></td>
<td>Contains a shell script ncsim_setup.sh and other setup files to set up and run an NCSim simulation.</td>
</tr>
<tr>
<td><code>/xcelium</code></td>
<td>Contains an Xcelium* Parallel simulator shell script xcelium_setup.sh and other setup files to set up and run a simulation.</td>
</tr>
<tr>
<td><code>/submodules</code></td>
<td>Contains HDL files for the IP core submodule.</td>
</tr>
<tr>
<td><code>&lt;IP submodule&gt;/</code></td>
<td>Platform Designer generates /synth and /sim sub-directories for each IP submodule directory that Platform Designer generates.</td>
</tr>
</tbody>
</table>
4.2.2. Scripting IP Core Generation

Use the qsys-script and qsys-generate utilities to define and generate an IP core variation outside of the Intel Quartus Prime GUI.

To parameterize and generate an IP core at command-line, follow these steps:

1. Run qsys-script to start a Tcl script that instantiates the IP and sets parameters:

   ```
   qsys-script --script=<script_file>.tcl
   ```

2. Run qsys-generate to generate the IP core variation:

   ```
   qsys-generate <IP variation file>.qsys
   ```

4.3. Modifying an IP Variation

After generating an IP core variation, use any of the following methods to modify the IP variation in the parameter editor.

Table 13.   Modifying an IP Variation

<table>
<thead>
<tr>
<th>Menu Command</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>File ➤ Open</strong></td>
<td>Select the top-level HDL (.v, or .vhd) IP variation file to launch the parameter editor and modify the IP variation. Regenerate the IP variation to implement your changes.</td>
</tr>
<tr>
<td><strong>View ➤ Project Navigator ➤ IP Components</strong></td>
<td>Double-click the IP variation to launch the parameter editor and modify the IP variation. Regenerate the IP variation to implement your changes.</td>
</tr>
<tr>
<td><strong>Project ➤ Upgrade IP Components</strong></td>
<td>Select the IP variation and click Upgrade in Editor to launch the parameter editor and modify the IP variation. Regenerate the IP variation to implement your changes.</td>
</tr>
</tbody>
</table>

4.4. Upgrading IP Cores

Any Intel FPGA IP variations that you generate from a previous version or different edition of the Intel Quartus Prime software, may require upgrade before compilation in the current software edition or version. The Project Navigator displays a banner indicating the IP upgrade status. Click Launch IP Upgrade Tool or Project ➤ Upgrade IP Components to upgrade outdated IP cores.
Figure 43. **IP Upgrade Alert in Project Navigator**

Icons in the **Upgrade IP Components** dialog box indicate when IP upgrade is required, optional, or unsupported for an IP variation in the project. Upgrade IP variations that require upgrade before compilation in the current version of the Intel Quartus Prime software.

*Note:* Upgrading IP cores may append a unique identifier to the original IP core entity names, without similarly modifying the IP instance name. There is no requirement to update these entity references in any supporting Intel Quartus Prime file, such as the Intel Quartus Prime Settings File (.qsf), Synopsys* Design Constraints File (.sdc), or Signal Tap File (.stp), if these files contain instance names. The Intel Quartus Prime software reads only the instance name and ignores the entity name in paths that specify both names. Use only instance names in assignments.

**Table 14.** **IP Core Upgrade Status**

<table>
<thead>
<tr>
<th>IP Core Status</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IP Upgraded</td>
<td>Indicates that your IP variation uses the latest version of the Intel FPGA IP core.</td>
</tr>
<tr>
<td>IP Component Outdated</td>
<td>Indicates that your IP variation uses an outdated version of the IP core.</td>
</tr>
<tr>
<td>IP End of Life</td>
<td>Indicates that Intel designates the IP core as end-of-life status. You may or may not be able to edit the IP core in the parameter editor. Support for this IP core discontinues in future releases of the Intel Quartus Prime software.</td>
</tr>
<tr>
<td>IP Core Status</td>
<td>Description</td>
</tr>
<tr>
<td>--------------------------------------</td>
<td>---------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>IP Upgrade Mismatch Warning</td>
<td>Provides warning of non-critical IP core differences in migrating IP to another device family.</td>
</tr>
<tr>
<td>IP has incompatible subcores</td>
<td>Indicates that the current version of the Intel Quartus Prime software does not support compilation of your IP variation, because the IP has incompatible subcores</td>
</tr>
<tr>
<td>Compilation of IP Not Supported</td>
<td>Indicates that the current version of the Intel Quartus Prime software does not support compilation of your IP variation. This can occur if another edition of the Intel Quartus Prime software, such as the Intel Quartus Prime Standard Edition, generated this IP. Replace this IP component with a compatible component in the current edition.</td>
</tr>
</tbody>
</table>

Follow these steps to upgrade IP cores:

1. In the latest version of the Intel Quartus Prime software, open the Intel Quartus Prime project containing an outdated IP core variation. The **Upgrade IP Components** dialog box automatically displays the status of IP cores in your project, along with instructions for upgrading each core. To access this dialog box manually, click **Project ➤ Upgrade IP Components**.

2. To upgrade one or more IP cores that support automatic upgrade, ensure that you turn on the **Auto Upgrade** option for the IP cores, and click **Auto Upgrade**. The **Status** and **Version** columns update when upgrade is complete. Example designs that any Intel FPGA IP core provides regenerate automatically whenever you upgrade an IP core.

3. To manually upgrade an individual IP core, select the IP core and click **Upgrade in Editor** (or simply double-click the IP core name). The parameter editor opens, allowing you to adjust parameters and regenerate the latest version of the IP core.

**Figure 44. Upgrading IP Cores**

- Opens Editor for Manual IP Upgrade
- Runs “Auto Upgrade” on all Outdated Cores
- Generates/Updates Combined Simulation Setup Script for all Project IP
Note: Intel FPGA IP cores older than Intel Quartus Prime software version 12.0 do not support upgrade. Intel verifies that the current version of the Intel Quartus Prime software compiles the previous two versions of each IP core. The Intel FPGA IP Core Release Notes reports any verification exceptions for Intel FPGA IP cores. Intel does not verify compilation for IP cores older than the previous two releases.

Related Information
Intel FPGA IP Release Notes

4.4.1. Upgrading IP Cores at Command-Line

Optionally, upgrade an Intel FPGA IP core at the command-line, rather than using the GUI. IP cores that do not support automatic upgrade do not support command-line upgrade.

- To upgrade a single IP core at the command-line, type the following command:

```bash
quartus_sh -ip_upgrade -variation_files <my_ip>.<qsys,.v, .vhd> \ <quartus_project>
```

Example:
```
quartus_sh -ip_upgrade -variation_files mega/pll25.qsys hps_testx
```

- To simultaneously upgrade multiple IP cores at the command-line, type the following command:

```bash
quartus_sh -ip_upgrade -variation_files "<my_ip1>.<qsys,.v, .vhd>> \ ; <my_ip_filepath/my_ip2>.<hdl>" <quartus_project>
```

Example:
```
quartus_sh -ip_upgrade -variation_files "mega/pll_tx2.qsys;mega/pll3.qsys" hps_testx
```

4.4.2. Migrating IP Cores to a Different Device

Migrate an Intel FPGA IP variation when you want to target a different (often newer) device. Most Intel FPGA IP cores support automatic migration. Some IP cores require manual IP regeneration for migration. A few IP cores do not support device migration, requiring you to replace them in the project. The Upgrade IP Components dialog box identifies the migration support level for each IP core in the design.

1. To display the IP cores that require migration, click Project ➤ Upgrade IP Components. The Description field provides migration instructions and version differences.

2. To migrate one or more IP cores that support automatic upgrade, ensure that the Auto Upgrade option is turned on for the IP cores, and click Perform Automatic Upgrade. The Status and Version columns update when upgrade is complete.

3. To migrate an IP core that does not support automatic upgrade, double-click the IP core name, and click OK. The parameter editor appears. If the parameter editor specifies a Currently selected device family, turn off Match project/default, and then select the new target device family.
4. Click **Generate HDL**, and confirm the **Synthesis** and **Simulation** file options. Verilog HDL is the default output file format. If you specify VHDL as the output format, select **VHDL** to retain the original output format.

5. Click **Finish** to complete migration of the IP core. Click **OK** if the software prompts you to overwrite IP core files. The **Device Family** column displays the new target device name when migration is complete.

6. To ensure correctness, review the latest parameters in the parameter editor or generated HDL.

   *Note:* IP migration may change ports, parameters, or functionality of the IP variation. These changes may require you to modify your design or to re-parameterize your IP variant. During migration, the IP variation's HDL generates into a library that is different from the original output location of the IP core. Update any assignments that reference outdated locations. If a symbol in a supporting Block Design File schematic represents your upgraded IP core, replace the symbol with the newly generated `<my_ip>.bsf`. Migration of some IP cores requires installed support for the original and migration device families.

**Related Information**

Intel FPGA IP Release Notes

### 4.4.3. Troubleshooting IP or Platform Designer System Upgrade

The **Upgrade IP Components** dialog box reports the version and status of each IP core and Platform Designer system following upgrade or migration.

If any upgrade or migration fails, the **Upgrade IP Components** dialog box provides information to help you resolve any errors.

*Note:* Do not use spaces in IP variation names or paths.

During automatic or manual upgrade, the Messages window dynamically displays upgrade information for each IP core or Platform Designer system. Use the following information to resolve upgrade errors:

**Table 15. IP Upgrade Error Information**

<table>
<thead>
<tr>
<th>Upgrade IP Components Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Status</td>
<td>Displays the “Success” or “Failed” status of each upgrade or migration. Click the status of any upgrade that fails to open the <strong>IP Upgrade Report</strong>.</td>
</tr>
<tr>
<td>Version</td>
<td>Dynamically updates the version number when upgrade is successful. The text is red when the IP requires upgrade.</td>
</tr>
<tr>
<td>Device Family</td>
<td>Dynamically updates to the new device family when migration is successful. The text is red when the IP core requires upgrade.</td>
</tr>
<tr>
<td>Auto Upgrade</td>
<td>Runs automatic upgrade on all IP cores that support auto upgrade. Also, automatically generates a <code>&lt;Project Directory&gt;/ip_upgrade_port_diff_report</code> report for IP cores or Platform Designer systems that fail upgrade. Review these reports to determine any port differences between the current and previous IP core version.</td>
</tr>
</tbody>
</table>
Use the following techniques to resolve errors if your IP core or Platform Designer system "Failed" to upgrade versions or migrate to another device. Review and implement the instructions in the Description field, including one or more of the following:

- If the current version of the software does not support the IP variant, right-click the component and click Remove IP Component from Project. Replace this IP core or Platform Designer system with the one supported in the current version of the software.
- If the current target device does not support the IP variant, select a supported device family for the project, or replace the IP variant with a suitable replacement that supports your target device.
- If an upgrade or migration fails, click Failed in the Status field to display and review details of the IP Upgrade Report. Click the Release Notes link for the latest known issues about the IP core. Use this information to determine the nature of the upgrade or migration failure and make corrections before upgrade.
- Run Auto Upgrade to automatically generate an IP Ports Diff report for each IP core or Platform Designer system that fails upgrade. Review the reports to determine any port differences between the current and previous IP core version. Click Upgrade in Editor to make specific port changes and regenerate your IP core or Platform Designer system.
- If your IP core or Platform Designer system does not support Auto Upgrade, click Upgrade in Editor to resolve errors and regenerate the component in the parameter editor.
4.5. Simulating Intel FPGA IP Cores

The Intel Quartus Prime software supports IP core RTL simulation in specific EDA simulators. IP generation creates simulation files, including the functional simulation model, any testbench (or example design), and vendor-specific simulator setup scripts for each IP core. Use the functional simulation model and any testbench or example design for simulation. IP generation output may also include scripts to compile and run any testbench. The scripts list all models or libraries you require to simulate your IP core.

The Intel Quartus Prime software provides integration with many simulators and supports multiple simulation flows, including your own scripted and custom simulation flows. Whichever flow you choose, IP core simulation involves the following steps:

1. Generate simulation model, testbench (or example design), and simulator setup script files.
2. Set up your simulator environment and any simulation scripts.
3. Compile simulation model libraries.
4. Run your simulator.
4.5.1. Generating IP Simulation Files

The Intel Quartus Prime software optionally generates the functional simulation model, any testbench (or example design), and vendor-specific simulator setup scripts when you generate an IP core. To control the generation of IP simulation files:

- To specify your supported simulator and options for IP simulation file generation, click **Assignment ➤ Settings ➤ EDA Tool Settings ➤ Simulation**.
- To parameterize a new IP variation, enable generation of simulation files, and generate the IP core synthesis and simulation files, click **Tools ➤ IP Catalog**.
- To edit parameters and regenerate synthesis or simulation files for an existing IP core variation, click **View ➤ Project Navigator ➤ IP Components**.

Table 16. Intel FPGA IP Simulation Files

<table>
<thead>
<tr>
<th>File Type</th>
<th>Description</th>
<th>File Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simulator setup scripts</td>
<td>Vendor-specific scripts to compile, elaborate, and simulate Intel FPGA IP models and simulation model library files.</td>
<td><code>&lt;my_dir&gt;/aldec/riviera_setup.tcl</code>&lt;br&gt;<code>&lt;my_dir&gt;/cadence/ncsim__setup.sh</code>&lt;br&gt;<code>&lt;my_dir&gt;/xcelium/xcelium_setup.sh</code>&lt;br&gt;<code>&lt;my_dir&gt;/mentor/msim_setup.tcl</code>&lt;br&gt;<code>&lt;my_dir&gt;/synopsys/vcs/vcs_setup.sh</code>&lt;br&gt;<code>&lt;my_dir&gt;/synopsys/vcsmx/vcsmx_setup.sh</code></td>
</tr>
</tbody>
</table>

**Note:** Intel FPGA IP cores support a variety of cycle-accurate simulation models, including simulation-specific IP functional simulation models and encrypted RTL models, and plain text RTL models. The models support fast functional simulation of your IP core instance using industry-standard VHDL or Verilog HDL simulators. For some IP cores, generation only produces the plain text RTL model, and you can simulate that model. Use the simulation models only for simulation and not for synthesis or any other purposes. Using these models for synthesis creates a nonfunctional design.

4.5.2. Scripting IP Simulation

The Intel Quartus Prime software supports the use of scripts to automate simulation processing in your preferred simulation environment. Use the scripting methodology that you prefer to control simulation.

Use a version-independent, top-level simulation script to control design, testbench, and IP core simulation. Because Intel Quartus Prime-generated simulation file names may change after IP upgrade or regeneration, your top-level simulation script must "source" the generated setup scripts, rather than using the generated setup scripts directly. Follow these steps to generate or regenerate combined simulator setup scripts:
Figure 46. Incorporating Generated Simulator Setup Scripts into a Top-Level Simulation Script

1. Click **Project ➤ Upgrade IP Components ➤ Generate Simulator Script for IP** (or run the `ip-setup-simulation` utility) to generate or regenerate a combined simulator setup script for all IP for each simulator.

2. Use the templates in the generated script to source the combined script in your top-level simulation script. Each simulator’s combined script file contains a rudimentary template that you adapt for integration of the setup script into a top-level simulation script.

   This technique eliminates manual update of simulation scripts if you modify or upgrade the IP variation.

**4.5.2.1. Generating a Combined Simulator Setup Script (Intel Quartus Prime Pro Edition)**

You can run the **Generate Simulator Setup Script for IP** command to generate a combined simulator setup script.

*Note:* This feature is available in the Intel Quartus Prime Pro Edition software for all devices. This feature is available in the Intel Quartus Prime Standard Edition software for only Intel Arria 10 devices.

Source this combined script from a top-level simulation script. Click **Tools ➤ Generate Simulator Setup Script for IP** (or use of the `ip-setup-simulation` utility at the command-line) to generate or update the combined scripts, after any of the following occur:

- IP core initial generation or regeneration with new parameters
- Intel Quartus Prime software version upgrade
- IP core version upgrade

To generate a combined simulator setup script for all project IP cores for each simulator:
1. Generate, regenerate, or upgrade one or more IP core. Refer to Generating IP Cores or Upgrading IP Cores.

2. Click Tools ➤ Generate Simulator Setup Script for IP (or run the ip-setup-simulation utility). Specify the Output Directory and library compilation options. Click OK to generate the file. By default, the files generate into the /<project directory>/simulator/ directory using relative paths.

3. To incorporate the generated simulator setup script into your top-level simulation script, refer to the template section in the generated simulator setup script as a guide to creating a top-level script:
   a. Copy the specified template sections from the simulator-specific generated scripts and paste them into a new top-level file.
   b. Remove the comments at the beginning of each line from the copied template sections.
   c. Specify the customizations you require to match your design simulation requirements, for example:
      - Specify the TOP_LEVEL_NAME variable to the design’s simulation top-level file. The top-level entity of your simulation is often a testbench that instantiates your design. Then, your design instantiates IP cores or Platform Designer systems. Set the value of TOP_LEVEL_NAME to the top-level entity.
      - If necessary, set the QSYS_SIMDIR variable to point to the location of the generated IP simulation files.
      - Compile the top-level HDL file (for example, a test program) and all other files in the design.
      - Specify any other changes, such as using the grep command-line utility to search a transcript file for error signatures, or e-mail a report.


Table 17. Simulation Script Utilities

<table>
<thead>
<tr>
<th>Utility</th>
<th>Syntax</th>
</tr>
</thead>
<tbody>
<tr>
<td>ip-setup-simulation generates a combined, version-independent simulation script for all Intel FPGA IP cores in your project. The command also automates regeneration of the script after upgrading software or IP versions. Use the compile-to-work option to compile all simulation files into a single work library if your simulation environment requires. Use the --use-relative-paths option to use relative paths whenever possible.</td>
<td>ip-setup-simulation --quartus-project=&lt;my proj&gt; --output-directory=&lt;my_dir&gt; --use-relative-paths --compile-to-work --use-relative-paths and --compile-to-work are optional. For command-line help listing all options for these executables, type: &lt;utility name&gt; --help.</td>
</tr>
<tr>
<td>ip-make-simscript generates a combined simulation script for all IP cores that you specify on the command line. Specify one or more .spd files and an output directory in the command. Running the script compiles IP simulation models into various simulation libraries.</td>
<td>ip-make-simscript --spd=&lt;ipA.spd,ipB.spd&gt; --output-directory=&lt;directory&gt;</td>
</tr>
</tbody>
</table>

continued...
4.5.2.1.1. Sourcing Aldec ActiveHDL* or Riviera Pro* Simulator Setup Scripts

Follow these steps to incorporate the generated ActiveHDL* or Riviera Pro* simulation scripts into a top-level project simulation script.

1. The generated simulation script contains the following template lines. Cut and paste these lines into a new file. For example, sim_top.tcl.

```
# Start of template
# If the copied and modified template file is "aldec.do", run it as:
# vsim -c -do aldec.do
#
# Source the generated sim script
# source rivierapro_setup.tcl
# Compile eda/sim_lib contents first
dev_com
# Override the top-level name (so that elab is useful)
# set TOP_LEVEL_NAME top
# Compile the standalone IP.
# com
# Compile the top-level
vlog -sv2K5 ../../top.sv
# Elaborate the design.
elab
# Run the simulation
run
# Report success to the shell
exit -code 0
# End of template
```

2. Delete the first two characters of each line (comment and space):

```
# Start of template
# If the copied and modified template file is "aldec.do", run it as:
# vsim -c -do aldec.do
#
# Source the generated sim script source rivierapro_setup.tcl
# Compile eda/sim_lib contents first dev_com
# Override the top-level name (so that elab is useful)
set TOP_LEVEL_NAME top
# Compile the standalone IP.
com
# Compile the top-level
vlog -sv2k5 ../../top.sv
# Elaborate the design.
elab
# Run the simulation
run
# Report success to the shell
exit -code 0
# End of template
```

3. Modify the TOP_LEVEL_NAME and compilation step appropriately, depending on the simulation's top-level file. For example:

```
set TOP_LEVEL_NAME sim_top
vlog -sv2k5 ../../sim_top.sv
```
4. If necessary, add the QSYS_SIMDIR variable to point to the location of the generated IP simulation files. Specify any other changes that you require to match your design simulation requirements. The scripts offer variables to set compilation or simulation options. Refer to the generated script for details.

5. Run the new top-level script from the generated simulation directory:

vsim -c -do <path to sim_top>.tcl

4.5.2.1.2. Sourcing Cadence Incisive* Simulator Setup Scripts

Follow these steps to incorporate the generated Cadence Incisive* IP simulation scripts into a top-level project simulation script.

1. The generated simulation script contains the following template lines. Cut and paste these lines into a new file. For example, ncsim.sh.

```bash
#!/usr/bin/env bash

# Start of template
# If the copied and modified template file is "ncsim.sh", run it as:
# ./ncsim.sh

# Do the file copy, dev_com and com steps
source ncsim_setup.sh
SKIP_ELAB=1
SKIP_SIM=1

# Compile the top level module
ncvlog -sv "${QSYS_SIMDIR}/../top.sv"

# Do the elaboration and sim steps
# Override the top-level name
# Override the sim options, so the simulation runs forever (until $finish()).
source ncsim_setup.sh
SKIP_FILE_COPY=1
SKIP_DEV_COM=1
SKIP_COM=1
TOP_LEVEL_NAME=top
USER_DEFINED_SIM_OPTIONS=""

# End of template
```

2. Delete the first two characters of each line (comment and space):

```bash
#!/usr/bin/env bash

# Start of template
# If the copied and modified template file is "ncsim.sh", run it as:
# ./ncsim.sh

# Do the file copy, dev_com and com steps
source ncsim_setup.sh
SKIP_ELAB=1
SKIP_SIM=1

# Compile the top level module
ncvlog -sv "${QSYS_SIMDIR}/../top.sv"

# Do the elaboration and sim steps
# Override the top-level name
# Override the sim options, so the simulation runs forever (until $finish()).
source ncsim_setup.sh
SKIP_FILE_COPY=1
SKIP_DEV_COM=1
SKIP_COM=1
TOP_LEVEL_NAME=top
USER_DEFINED_SIM_OPTIONS=""

# End of template
```
3. Modify the `TOP_LEVEL_NAME` and compilation step appropriately, depending on the simulation’s top-level file. For example:

```
TOP_LEVEL_NAME=sim_top \
nclog -sv "@QSYS_SIMDIR/../top.sv"
```

4. If necessary, add the `QSYS_SIMDIR` variable to point to the location of the generated IP simulation files. Specify any other changes that you require to match your design simulation requirements. The scripts offer variables to set compilation or simulation options. Refer to the generated script for details.

5. Run the resulting top-level script from the generated simulation directory by specifying the path to `ncsim.sh`.

### 4.5.2.1.3. Sourcing Cadence Xcelium Simulator Setup Scripts

1. The generated simulation script contains the following template lines. Cut and paste these lines into a new file. For example, `xmsim.sh`.

```bash
# Start of template
# Xcelium Simulation Script.
# If the copied and modified template file is "xmsim.sh", run it as: 
# ./xmsim.sh
#
# Do the file copy, dev_com and com steps
source <script generation output directory>/xcelium/xcelium_setup.sh \
SKIP_ELAB=1 \
SKIP_SIM=1 \
USER_DEFINED_COMPILE_OPTIONS=<compilation options for your design> \
USER_DEFINED_VHDL_COMPILE_OPTIONS=<VHDL compilation options for your design> \
USER_DEFINED_VERILOG_COMPILE_OPTIONS=<Verilog compilation options for your design> \
QSYS_SIMDIR=<script generation output directory>
#
# Compile all design files and testbench files, including the top level. 
# (These are all the files required for simulation other than the files compiled by the IP script)
# xmvlog <compilation options> <design and testbench files>
#
# TOP_LEVEL_NAME is used in this script to set the top-level simulation or testbench module/entity name.
#
# Run the IP script again to elaborate and simulate the top level:
# - Specify TOP_LEVEL_NAME and USER_DEFINED_ELAB_OPTIONS.
# - Override the default USER_DEFINED_SIM_OPTIONS. For example, to run until $finish(), set to an empty string: USER_DEFINED_SIM_OPTIONS="".
#
# source <script generation output directory>/xcelium/xcelium_setup.sh \
# SKIP_FILE_COPY=1 \
# SKIP_DEV_COM=1 \
# SKIP_COM=1 \
# TOP_LEVEL_NAME=<simulation top> \
# USER_DEFINED_ELAB_OPTIONS=<elaboration options for your design> \
# USER_DEFINED_SIM_OPTIONS=<simulation options for your design>
#
# End of template
```

2. Delete the first two characters of each line (comment and space):
4. Introduction to Intel FPGA IP Cores

3. If necessary, add the QSYS_SIMDIR variable to point to the location of the generated IP simulation files. Specify any other changes that you require to match your design simulation requirements. The scripts offer variables to set compilation or simulation options. Refer to the generated script for details.

4. Run the resulting top-level script from the generated simulation directory by specifying the path to xmsim.sh.

4.5.2.1.4. Sourcing Mentor Graphics ModelSim Simulator Setup Scripts

Follow these steps to incorporate the generated ModelSim IP simulation scripts into a top-level project simulation script.

1. The generated simulation script contains the following template lines. Cut and paste these lines into a new file. For example, sim_top.tcl.

```tcl
# # Start of template
# # If the copied and modified template file is "mentor.do", run it
# as: vsim -c -do mentor.do
#
# Source the generated sim script
source msim_setup.tcl
# Compile eda/sim_lib contents first
# dev_com
# Override the top-level name (so that elab is useful)
set TOP_LEVEL_NAME top
# Compile the standalone IP.
# com
# Compile the top-level
vlog -sv ../../top.sv
# Elaborate the design.
elab
# Run the simulation
run -a
```
2. Delete the first two characters of each line (comment and space):

```
# Start of template
# If the copied and modified template file is "mentor.do", run it
# as: vsim -c -do mentor.do
# Source the generated sim script source msim_setup.tcl
# Compile eda/sim_lib contents first
dev_com
# Override the top-level name (so that elab is useful)
set TOP_LEVEL_NAME top
# Compile the standalone IP.
com
# Compile the top-level vlog -sv ../../top.sv
# Elaborate the design.
elab
# Run the simulation
run -a
# Report success to the shell
exit -code 0
# End of template
```

3. Modify the `TOP_LEVEL_NAME` and compilation step appropriately, depending on the simulation’s top-level file. For example:

```
set TOP_LEVEL_NAME sim_top vlog -sv ../..sim_top.sv
```

4. If necessary, add the `QSYS_SIMDIR` variable to point to the location of the generated IP simulation files. Specify any other changes required to match your design simulation requirements. The scripts offer variables to set compilation or simulation options. Refer to the generated script for details.

5. Run the resulting top-level script from the generated simulation directory:

```
vsim -c -do <path to sim_top>.tcl
```

### 4.5.2.1.5. Sourcing Synopsys VCS Simulator Setup Scripts

Follow these steps to incorporate the generated Synopsys VCS simulation scripts into a top-level project simulation script.

1. The generated simulation script contains these template lines. Cut and paste the lines preceding the “helper file” into a new executable file. For example, `synopsys_vcs.f`.

```
# # Start of template
# # If the copied and modified template file is "vcs_sim.sh", run it
# # as: ./vcs_sim.sh
# # Override the top-level name
# # specify a command file containing elaboration options
# # (system verilog extension, and compile the top-level).
# # Override the sim options, so the simulation
# # runs forever (until $finish()).
# source vcs_setup.sh
# TOP_LEVEL_NAME=top
# USER_DEFINED_ELAB_OPTIONS="'-f ../..../synopsys_vcs.f"
# USER_DEFINED_SIM_OPTIONS=""
# # helper file: synopsys_vcs.f
```
2. Delete the first two characters of each line (comment and space) for the `vcs.sh` file, as shown below:

```bash
# Start of template
# If the copied and modified template file is "vcs_sim.sh", run it as: ./vcs_sim.sh
# Override the top-level name
# specify a command file containing elaboration options
# (system verilog extension, and compile the top-level).
# Override the sim options, so the simulation runs forever (until $finish()).
source vcs_setup.sh
TOP_LEVEL_NAME=top
USER_DEFINED_ELAB_OPTIONS="'-f ../../../synopsys_vcs.f'"
USER_DEFINED_SIM_OPTIONS=""
```

3. Delete the first two characters of each line (comment and space) for the `synopsys_vcs.f` file, as shown below:

```bash
# helper file: synopsys_vcs.f
+systemverilogext+.sv
../../../top.sv
# End of template
```

4. Modify the `TOP_LEVEL_NAME` and compilation step appropriately, depending on the simulation’s top-level file. For example:

```bash
TOP_LEVEL_NAME=sim_top
```

5. If necessary, add the `QSYS_SIMDIR` variable to point to the location of the generated IP simulation files. Specify any other changes required to match your design simulation requirements. The scripts offer variables to set compilation or simulation options. Refer to the generated script for details.

6. Run the resulting top-level script from the generated simulation directory by specifying the path to `vcs_sim.sh`.

### 4.5.2.1.6. Sourcing Synopsys VCS MX Simulator Setup Scripts

Follow these steps to incorporate the generated Synopsys VCS MX simulation scripts for use in top-level project simulation scripts.

1. The generated simulation script contains these template lines. Cut and paste the lines preceding the “helper file” into a new executable file. For example, `vcsmx.sh`.

```bash
# Start of template
# If the copied and modified template file is "vcsmx_sim.sh", run it as: ./vcsmx_sim.sh
# Do the file copy, dev_com and com steps
source vcsmx_setup.sh
SKIP_ELAB=1
SKIP_SIM=1
# Compile the top level module vlogan +v2k
+systemverilogext+.sv "$QSYS_SIMDIR/../top.sv"
# Do the elaboration and sim steps
# Override the top-level name
```

---

4. Introduction to Intel FPGA IP Cores

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2. Delete the first two characters of each line (comment and space), as shown below:

```bash
# Start of template
# If the copied and modified template file is "vcsmx_sim.sh", run
# it as: ./vcsmx_sim.sh
#
# Do the file copy, dev_com and com steps
source vcsmx_setup.sh
SKIP_ELAB=1
SKIP_SIM=1

# Compile the top level module
vlogan +v2k +systemverilogext+.sv "$QSYS_SIMDIR/../top.sv"

# Do the elaboration and sim steps
# Override the top-level name
# Override the sim options, so the simulation runs
# forever (until $finish()).
source vcsmx_setup.sh
SKIP_FILE_COPY=1
SKIP_DEV_COM=1
SKIP_COM=1
TOP_LEVEL_NAME="'-top top'"
USER_DEFINED_SIM_OPTIONS=""
# End of template
```

3. Modify the `TOP_LEVEL_NAME` and compilation step appropriately, depending on the simulation's top-level file. For example:

```bash
TOP_LEVEL_NAME="'-top sim_top'"
```

4. Make the appropriate changes to the compilation of the your top-level file, for example:

```bash
vlogan +v2k +systemverilogext+.sv "$QSYS_SIMDIR/../sim_top.sv"
```

5. If necessary, add the `QSYS_SIMDIR` variable to point to the location of the generated IP simulation files. Specify any other changes required to match your design simulation requirements. The scripts offer variables to set compilation or simulation options. Refer to the generated script for details.

6. Run the resulting top-level script from the generated simulation directory by specifying the path to `vcsmx_sim.sh`.

### 4.6. Synthesizing IP Cores in Other EDA Tools

Optionally, use another supported EDA tool to synthesize a design that includes Intel FPGA IP cores. When you generate the IP core synthesis files for use with third-party EDA synthesis tools, you can create an area and timing estimation netlist. To enable generation, turn on **Create timing and resource estimates for third-party EDA synthesis tools** when customizing your IP variation.
The area and timing estimation netlist describes the IP core connectivity and
architecture, but does not include details about the true functionality. This information
enables certain third-party synthesis tools to better report area and timing estimates.
In addition, synthesis tools can use the timing information to achieve timing-driven
optimizations and improve the quality of results.

The Intel Quartus Prime software generates the `<variant name>_syn.v` netlist file
in Verilog HDL format, regardless of the output file format you specify. If you use this
netlist for synthesis, you must include the IP core wrapper file `<variant name>.v` or
`<variant name>.vhd` in your Intel Quartus Prime project.

4.7. Instantiating IP Cores in HDL

Instantiate an IP core directly in your HDL code by calling the IP core name and
declaring the IP core's parameters. This approach is similar to instantiating any other
module, component, or subdesign. When instantiating an IP core in VHDL, you must
include the associated libraries.

4.7.1. Example Top-Level Verilog HDL Module

Verilog HDL ALTFP_MULT in Top-Level Module with One Input Connected to Multiplexer.

```verilog
module MF_top (a, b, sel, datab, clock, result);
    input [31:0] a, b, datab;
    input clock, sel;
    output [31:0] result;
    wire [31:0] wire_dataa;

    assign wire_dataa = (sel)? a : b;
    altfp_mult inst1
        (.dataa(wire_dataa), .datab(datab), .clock(clock), .result(result));

    defparam
        inst1.pipeline = 11,
        inst1.width_exp = 8,
        inst1.width_man = 23,
        inst1.exception_handling = "no";
endmodule
```

4.7.2. Example Top-Level VHDL Module

VHDL ALTFP_MULT in Top-Level Module with One Input Connected to Multiplexer.

```vhdl
library ieee;
use ieee.std_logic_1164.all;
library altera_mf;
use altera_mf.altera_mf_components.all;

entity MF_top is
    port (clock, sel : in  std_logic;
        a, b, datab : in  std_logic_vector(31 downto 0);
        result : out std_logic_vector(31 downto 0));
end entity;

architecture arch_MF_top of MF_top is
    signal wire_dataaa : std_logic_vector(31 downto 0);
begin
    wire_dataaa <= a when (sel = '1') else b;
    inst1 : altfp_mult
```

4. Introduction to Intel FPGA IP Cores
4.8. Support for the IEEE 1735 Encryption Standard

The Intel Quartus Prime Pro Edition software supports the IEEE 1735 v1 encryption standard for IP core file decryption. You can encrypt the Verilog HDL or VHDL IP files with the `encrypt_1735` utility, or with a third-party encryption tool that supports the IEEE 1735 standard. You can then use the encrypted files in the Intel Quartus Prime Pro Edition software and simulation tools that support the IEEE 1735 encryption standard.

Type `encrypt_1735 --help` at the Intel Quartus Prime command line to view syntax and all supported options for the `encrypt_1735` utility.

Adding the following Verilog or VHDL pragma to your RTL, along with the public key, enables the Intel Quartus Prime software to use the key to decrypt IP core files.

**Verilog/SystemVerilog Encryption Pragma (Third-Party Tools):**

```
'pragma protect key_keyowner="Intel Corporation"
'pragma protect data_method="aes128-cbc"
'pragma protect key_method="rsa"
'pragma protect key_keyname="Intel-FPGA-Quartus-RSA-1"
'pragma protect key_public_key
<encrypted session key>

'pragma protect begin
'pragma protect end
```

**VHDL Encryption Pragma (Third-Party Tools):**

```
'protect key_keyowner = "Intel Corporation"
'protect data_method="aes128-cbc"
'protect key_method = "rsa"
```
Only file encryption with a third-party tool requires the public encryption key. File encryption with the Intel Quartus Prime Pro Edition software does not require the public encryption key.

Use one of the following methods to obtain the public encryption key:

- To obtain the encryption key, login or register for a My-Intel account, and then submit an Intel Premier Support case requesting the encryption key.
- If you are ineligible for Intel Premier Support, you can submit a question regarding the "IEEE 1735 Encryption Public Key" to the Intel Community Forum for assistance.

*Note:* The Intel Quartus Prime Standard Edition software does not support IEEE 1735 encryption.

**Related Information**

- My-Intel.com
- Intel Community Forum

### 4.9. Introduction to Intel FPGA IP Cores Revision History

This chapter has the following revision history.

<table>
<thead>
<tr>
<th>Document Version</th>
<th>Intel Quartus Prime Version</th>
<th>Changes</th>
</tr>
</thead>
</table>
| 2019.05.13       | 18.1.0                     | • Added archives topic.  
|                  |                            | • Updated the keyname and added --help information to "Support for the IEEE 1735 Encryption Standard." |
| 2018.10.24       | 18.1.0                     | • Updated information about obtaining IEEE 1735 Encryption key. |
| 2018.09.24       | 18.1.0                     | • Added statement that the Intel Quartus Prime software installer does not support spaces in the installation path.  
|                  |                            | • Added "Intel FPGA IP Best Practices" topic.  
|                  |                            | • Divided "Introduction to Intel FPGA IP Cores" into separate chapter of Getting Started User Guide. |
| 2018.05.07       | 18.0.0                     | • Updated screenshots of IP Catalog and Parameter Editor for latest IP names.  
|                  |                            | • Added note about Generate Combined Simulator Setup Scripts command limitations.  
|                  |                            | • Added information about generation of simulation files for Xcelium*. |
| 2017.11.06       | 17.1.0                     | • Revised product branding for Intel standards.  
|                  |                            | • Revised topics on Intel FPGA IP Evaluation Mode (formerly OpenCore). |

*continued...*
## 4. Introduction to Intel FPGA IP Cores

<table>
<thead>
<tr>
<th>Document Version</th>
<th>Intel Quartus Prime Version</th>
<th>Changes</th>
</tr>
</thead>
</table>
| 2017.05.08       | 17.0.0                      | • Added note that IP core encryption is supported only in Intel Quartus Prime Pro Edition.  
                      • Revised product branding for Intel standards. |
| 2016.10.31       | 16.1.0                      | • Removed references to `.qsys` file creation during Intel Quartus Prime Pro Edition stand-alone IP generation.  
                      • Added references to `.ip` file creation during Intel Quartus Prime Pro Edition stand-alone IP generation.  
                      • Updated IP Core Generation Output files list and diagram.  
                      • Added Support for IP Core Encryption topic. |
| 2018.05.07       | 18.0                        | Initial release as separate chapter of *Getting Started User Guide*. |
5. Migrating to Intel Quartus Prime Pro Edition


Note: The migration steps for Quartus Prime Lite Edition, Intel Quartus Prime Standard Edition, and the Quartus II software are identical. For brevity, this section refers to these design tools collectively as "other Quartus software products."

Migrating to Intel Quartus Prime Pro Edition requires the following changes to other Quartus software product projects:

1. Upgrade project assignments and constraints with equivalent Intel Quartus Prime Pro Edition assignments.
2. Upgrade all Intel FPGA IP core variations and Platform Designer systems in your project.
3. Upgrade design RTL to standards-compliant VHDL, Verilog HDL, or SystemVerilog.

This document describes each migration step in detail.

5.1. Keep Pro Edition Project Files Separate

The Intel Quartus Prime Pro Edition software does not support project or constraint files from other Quartus software products. Do not place project files from other Quartus software products in the same directory as Intel Quartus Prime Pro Edition project files. In general, use Intel Quartus Prime Pro Edition project files and directories only for Intel Quartus Prime Pro Edition projects, and use other Quartus software product files only with those software tools.

Intel Quartus Prime Pro Edition projects do not support compilation in other Quartus software products, and vice versa. The Intel Quartus Prime Pro Edition software generates an error if the Compiler detects other Quartus software product's features in project files.

Before migrating other Quartus software product projects, click Project ➤ Archive Project to save a copy of your original project before making modifications for migration.

5.2. Upgrade Project Assignments and Constraints

Intel Quartus Prime Pro Edition software introduces changes to handling of project assignments and constraints that the Quartus Settings File (.qsf) stores. Upgrade other Quartus software product project assignments and constraints for migration to the Intel Quartus Prime Pro Edition software. Upgrade other Quartus software product assignments with Assignments ➤ Assignment Editor, by editing the .qsf file directly, or by using a Tcl script.
The following sections detail each type project assignment upgrade that migration requires.

Related Information
- Modify Entity Name Assignments on page 92
- Resolve Timing Constraint Entity Names on page 92
- Verify Generated Node Name Assignments on page 93
- Replace Logic Lock (Standard) Regions on page 93
- Modify Signal Tap Logic Analyzer Files on page 95
- Remove Unsupported Feature Assignments on page 96

5.2.1. Modify Entity Name Assignments

Intel Quartus Prime Pro Edition software supports assignments that include instance names without a corresponding entity name.

- "a_entity:a|b_entity:b|c_entity:c" (includes deprecated entity names)
- “a|b|c” (omits deprecated entity names)

While the current version of the Intel Quartus Prime Pro Edition software still accepts entity names in the .qsf, the Compiler ignores the entity name. The Compiler generates a warning message upon detection of an entity names in the .qsf. Whenever possible, you should remove entity names from assignments, and discontinue reliance on entity-based assignments. Future versions of the Intel Quartus Prime Pro Edition software may eliminate all support for entity-based assignments.

5.2.2. Resolve Timing Constraint Entity Names


Use .sdc files from other Quartus software products without modification. However, any scripts that include custom processing of names that the .sdc command returns, such as get_registers may require modification. Your scripts must reflect that returned strings do not include entity names.

The .sdc commands respect wildcard patterns containing entity names. Review the Timing Analyzer reports to verify application of all constraints. The following example illustrates differences between functioning and non-functioning .sdc scripts:

```
# Apply a constraint to all registers named "acc" in the entity "counter".
# This constraint functions in both SE and PE, because the SDC
# command always understands wildcard patterns with entity names in them
set_false_path -to [get_registers "counter:*|*acc"]

# This does the same thing, but first it converts all register names to
# strings, which includes entity names by default in the SE
# but excludes them by default in the PE. The regexp will therefore
# fail in PE by default.
#
# This script would also fail in the SE, and earlier
# versions of Quartus II, if entity name display had been disabled
# in the QSF.
set all_reg_strs [query_collection -list -all [get_registers *]]
foreach keeper $all_reg_strs {
    if {([regexp {counter:*|:*acc} $keeper])} {
```
Removal of the entity name processing from `.sdc` files may not be possible due to complex processing involving node names. Use standard `.sdc` whenever possible to replace such processing. Alternatively, add the following code to the top and bottom of your script to temporarily re-enable entity name display in the `.sdc` file:

```bash
# This script requires that entity names be included
due to custom name processing
set old_mode [set_project_mode -get_mode_value always_show_entity_name]
set_project_mode -always_show_entity_name on

<... the rest of your script goes here ...>

# Restore the project mode
set_project_mode -always_show_entity_name $old_mode
```

### 5.2.3. Verify Generated Node Name Assignments

Intel Quartus Prime synthesis generates and automatically names internal design nodes during processing. The Intel Quartus Prime Pro Edition uses different conventions than other Quartus software products to generate node names during synthesis. When you synthesize your other Quartus software product project in Intel Quartus Prime Pro Edition, the synthesis-generated node names may change. If any scripts or constraints depend on the synthesis-generated node names, update the scripts or constraints to match the Intel Quartus Prime Pro Edition synthesis node names.

Avoid dependence on synthesis-generated names due to frequent changes in name generation. In addition, verify the names of duplicated registers and PLL clock outputs to ensure compatibility with any script or constraint.

### 5.2.4. Replace Logic Lock (Standard) Regions

Intel Quartus Prime Pro Edition software introduces more simplified and flexible Logic Lock constraints, compared with previous Logic Lock regions. You must replace all Logic Lock (Standard) assignments with compatible Logic Lock assignments for migration.

To convert Logic Lock (Standard) regions to Logic Lock regions:

1. Edit the `.qsf` to delete or comment out all of the following Logic Lock assignments:

```bash
set_global_assignment -name LL_ENABLED*
set_global_assignment -name LL_AUTO_SIZE*
set_global_assignment -name LL_STATE FLOATING*
set_global_assignment -name LL_RESERVED*
set_global_assignment -name LL_CORE_ONLY*
set_global_assignment -name LL_SECURITY_ROUTING_INTERFACE*
set_global_assignment -name LL_IGNORE_IO_BANK_SECURITY_CONSTRAINT*
set_global_assignment -name LL_PR_REGION*
set_global_assignment -name LL_ROUTING_REGION_EXPANSION_SIZE*
set_global_assignment -name LL_WIDTH*
set_global_assignment -name LL_HEIGHT
set_global_assignment -name LL_ORIGIN
set_instance_assignment -name LL_MEMBER_OF
```
2. Edit the .qsf file or click Tools ➤ Chip Planner to define new Logic Lock regions. Logic Lock constraint syntax is simplified, for example:

```
set_instance_assignment -name PLACE_REGION "1 1 20 20" -to fifo1
set_instance_assignment -name RESERVE_PLACE_REGION OFF -to fifo1
set_instance_assignment -name CORE_ONLY_PLACE_REGION OFF -to fifo1
```

Compilation fails if synthesis finds other Quartus software product’s Logic Lock assignments in an Intel Quartus Prime Pro Edition project. The following table compares other Quartus software product region constraint support with the Intel Quartus Prime Pro Edition software.

<table>
<thead>
<tr>
<th>Constraint Type</th>
<th>Logic Lock (Standard) Region Support Other Quartus Software Products</th>
<th>Logic Lock Region Support Intel Quartus Prime Pro Edition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fixed rectangular, nonrectangular or non-contiguous regions</td>
<td>Full support.</td>
<td>Full support.</td>
</tr>
<tr>
<td>Chip Planner entry</td>
<td>Full support.</td>
<td>Full support.</td>
</tr>
<tr>
<td>Periphery element assignments</td>
<td>Supported in some instances.</td>
<td>Full support. Use “core-only” regions to exclude the periphery.</td>
</tr>
<tr>
<td>Nested (“hierarchical”) regions</td>
<td>Supported but separate hierarchy from the user instance tree.</td>
<td>Supported in same hierarchy as user instance tree.</td>
</tr>
<tr>
<td>Reserved regions</td>
<td>Limited support for nested or nonrectangular reserved regions. Reserved regions typically cannot cross I/O columns; use non-contiguous regions instead.</td>
<td>Full support for nested and nonrectangular regions. Reserved regions can cross I/O columns without affecting periphery logic if the regions are &quot;core-only&quot;.</td>
</tr>
<tr>
<td>Routing regions</td>
<td>Limited support via &quot;routing expansion.&quot; No support with hierarchical regions.</td>
<td>Full support (including future support for hierarchical regions).</td>
</tr>
<tr>
<td>Floating or autosized regions</td>
<td>Full support.</td>
<td>No support.</td>
</tr>
<tr>
<td>Region names</td>
<td>Regions have names.</td>
<td>Regions are identified by the instance name of the constrained logic.</td>
</tr>
<tr>
<td>Multiple instances in the same region</td>
<td>Full support.</td>
<td>Support for non-reserved regions. Create one region per instance, and then specify the same definition for multiple instances to assign to the same area. Not supported for reserved regions.</td>
</tr>
<tr>
<td>Member exclusion</td>
<td>Full support.</td>
<td>No support for arbitrary logic. Use a core-only region to exclude periphery elements. Use non-rectangular regions to include more RAM or DSP columns as needed.</td>
</tr>
</tbody>
</table>

**5.2.4.1. Logic Lock Region Assignment Examples**

These examples show the syntax of Logic Lock region assignments in the .qsf file. Optionally, enter these assignments in the Assignment Editor, the Logic Lock Regions Window, or the Chip Planner.
Example 1. **Assign Rectangular Logic Lock Region**

Assigns a rectangular Logic Lock region to a lower right corner location of (10,10), and an upper right corner of (20,20) inclusive.

```
set_instance_assignment -name PLACE_REGION -to a|b|c "X10 Y10 X20 Y20"
```

Example 2. **Assign Non-Rectangular Logic Lock Region**

Assigns instance with full hierarchical path "x|y|z" to non-rectangular L-shaped Logic Lock region. The software treats each set of four numbers as a new box.

```
set_instance_assignment -name PLACE_REGION -to x|y|z "X10 Y10 X20 Y50; X20 Y10 X50 Y20"
```

Example 3. **Assign Subordinate Logic Lock Instances**

By default, the Intel Quartus Prime software constrains every child instance to the Logic Lock region of its parent. Any constraint to a child instance intersects with the constraint of its ancestors. For example, in the following example, all logic beneath "a|b|c|d" constrains to box (10,10), (15,15), and not (0,0), (15,15). This result occurs because the child constraint intersects with the parent constraint.

```
set_instance_assignment -name PLACE_REGION -to a|b|c "X10 Y10 X20 Y20"
set_instance_assignment -name PLACE_REGION -to a|b|c|d "X0 Y0 X15 Y15"
```

Example 4. **Assign Multiple Logic Lock Instances**

By default, a Logic Lock region constraint allows logic from other instances to share the same region. These assignments place instance c and instance g in the same location. This strategy is useful if instance c and instance g are heavily interacting.

```
set_instance_assignment -name PLACE_REGION -to a|b|c "X10 Y10 X20 Y20"
set_instance_assignment -name PLACE_REGION -to e|f|g "X10 Y10 X20 Y20"
```

Example 5. **Assigned Reserved Logic Lock Regions**

Optionally reserve an entire Logic Lock region for one instance and any of its subordinate instances.

```
set_instance_assignment -name PLACE_REGION -to a|b|c "X10 Y10 X20 Y20"
set_instance_assignment -name RESERVE_PLACE_REGION -to a|b|c ON

# The following assignment causes an error. The logic in e|f|g is not legally placeable anywhere:
# set_instance_assignment -name PLACE_REGION -to e|f|g "X10 Y10 X20 Y20"

# The following assignment does *not* cause an error, but is effectively constrained to the box (20,10), (30,20), since the (10,10), (20,20) box is reserved
# for a|b|c
set_instance_assignment -name PLACE_REGION -to e|f|g "X10 Y10 X30 Y20"
```

5.2.5. **Modify Signal Tap Logic Analyzer Files**

Intel Quartus Prime Pro Edition introduces new methodology for entity names, settings, and assignments. These changes impact the processing of Signal Tap Logic Analyzer Files (.stp).
If you migrate a project that includes .stp files generated by other Quartus software products, you must make the following changes to migrate to the Intel Quartus Prime Pro Edition:

1. Remove entity names from .stp files. The Signal Tap Logic Analyzer allows without error, but ignores, entity names in .stp files. Remove entity names from .stp files for migration to Intel Quartus Prime Pro Edition:
   a. Click View ➤ Node Finder to locate and remove appropriate nodes. Use Node Finder options to filter on nodes.
   b. Click Processing ➤ Start ➤ Start Analysis & Elaboration to repopulate the database and add valid node names.

2. Remove post-fit nodes. Intel Quartus Prime Pro Edition uses a different post-fit node naming scheme than other Quartus software products.
   a. Remove post-fit tap node names originating from other Quartus software products.
   b. Click View ➤ Node Finder to locate and remove post-fit nodes. Use Node Finder options to filter on nodes.
   c. Click Processing ➤ Start Compilation to repopulate the database and add valid post-fit nodes.

3. Run an initial compilation in Intel Quartus Prime Pro Edition from the GUI. The Compiler automatically removes Signal Tap assignments originating other Quartus software products. Alternatively, from the command-line, run quartus_stp once on the project to remove outmoded assignments.

   Note: quartus_stp introduces no migration impact in the Intel Quartus Prime Pro Edition. Your scripts require no changes to quartus_stp for migration.

4. Modify .sdc constraints for JTAG. Intel Quartus Prime Pro Edition does not support embedded .sdc constraints for JTAG signals. Modify the timing template to suit the design's JTAG driver and board.

## 5.2.6. Remove References to .qip Files

In Intel Quartus Prime Standard Edition projects, Platform Designer (Standard) generates .qip files. These files describe the parameterized IP cores to the Compiler, and appear as assignments in the project’s .qsf file. However, in Intel Quartus Prime Pro Edition projects, the parameterized IP core description occurs in .ip files. Moreover, references to .qip files in a project’s .qsf file cause synthesis errors during compilation.

- When migrating a project to Intel Quartus Prime Pro Edition, remove all references to .qip files from the .qsf file.

## 5.2.7. Remove Unsupported Feature Assignments

The Intel Quartus Prime Pro Edition software does not support some feature assignments that other Quartus software products support. Remove the following unsupported feature assignments from other Quartus software product .qsf files for migration to the Intel Quartus Prime Pro Edition software.
• Incremental Compilation (partitions)—The current version of the Intel Quartus Prime Pro Edition software does not support Intel Quartus Prime Standard Edition incremental compilation. Remove all incremental compilation feature assignments from other Quartus software product .qsf files before migration.

• Intel Quartus Prime Standard Edition Physical synthesis assignments. Intel Quartus Prime Pro Edition software does not support Intel Quartus Prime Standard Edition Physical synthesis assignments. Remove any of the following assignments from the .qsf file or design RTL (instance assignments) before migration.

- PHYSICAL_SYNTHESIS_COMBO_LOGIC_FOR_AREA
- PHYSICAL_SYNTHESIS_COMBO_LOGIC
- PHYSICAL_SYNTHESIS_REGISTER_DUPLICATION
- PHYSICAL_SYNTHESIS_REGISTER_RETIMING
- PHYSICAL_SYNTHESISASYNCHRONOUS_SIGNAL_PIPELINING
- PHYSICAL_SYNTHESIS_MAP_LOGIC_TO_MEMORY_FOR_AREA

5.3. Upgrade IP Cores and Platform Designer Systems

Upgrade all IP cores and Platform Designer systems in your project for migration to the Intel Quartus Prime Pro Edition software. The Intel Quartus Prime Pro Edition software uses standards-compliant methodology for instantiation and generation of IP cores and Platform Designer systems. Most Intel FPGA IP cores and Platform Designer systems upgrade automatically in the Upgrade IP Components dialog box.

Other Quartus software products use a proprietary Verilog configuration scheme within the top level of IP cores and Platform Designer systems for synthesis files. The Intel Quartus Prime Pro Edition does not support this scheme. To upgrade all IP cores and Platform Designer systems in your project, click Project ➤ Upgrade IP Components.(1)

Table 19. IP Core and Platform Designer System Differences

<table>
<thead>
<tr>
<th>Other Quartus Software Products</th>
<th>Intel Quartus Prime Pro Edition</th>
</tr>
</thead>
</table>
| IP and Platform Designer system generation use a proprietary Verilog HDL configuration scheme within the top level of IP cores and Platform Designer systems for synthesis files. This proprietary Verilog HDL configuration scheme prevents RTL entities from ambiguous instantiation errors during synthesis. However, these errors may manifest in simulation. Resolving this issue requires writing a Verilog HDL configuration to disambiguate the instantiation, delete the duplicate entity from the project, or rename one of the conflicting entities. Intel Quartus Prime Pro Edition IP strategy resolves these issues. | IP and Platform Designer system generation does not use proprietary Verilog HDL configurations. The compilation library scheme changes in the following ways:
- Compiles all variants of an IP core into the same compilation library across the entire project. Intel Quartus Prime Pro Edition identically names IP cores with identical functionality and parameterization to avoid ambiguous entity instantiation errors. For example, the files for every Intel Arria 10 PCI Express* IP core variant compile into the altera_pcie_a10_hip_151 compilation library.
- Simulation and synthesis file sets for IP cores and systems instantiate entities in the same manner.
- The generated RTL directory structure now matches the compilation library structure. |

Note: For complete information on upgrading IP cores, refer to Managing Intel Quartus Prime Projects.

Related Information

- Introduction to Intel FPGA IP Cores on page 60

(1) For brevity, this section refers to Intel Quartus Prime Standard Edition, Intel Quartus Prime Lite Edition, and the Quartus II software collectively as "other Quartus software products."
5.4. Upgrade Non-Compliant Design RTL

The Intel Quartus Prime Pro Edition software introduces a new synthesis engine (quartus_syn executable).

The quartus_syn synthesis enforces stricter industry-standard HDL structures and supports the following enhancements in this release:

- Support for modules with SystemVerilog Interfaces
- Improved support for VHDL2008
- New RAM inference engine infers RAMs from GENERATE statements or array of integers
- Stricter syntax/semantics check for improved compatibility with other EDA tools

Account for these synthesis differences in existing RTL code by ensuring that your design uses standards-compliant VHDL, Verilog HDL, or SystemVerilog. The Compiler generates errors when processing non-compliant RTL. Use the guidelines in this section to modify existing RTL for compatibility with the Intel Quartus Prime Pro Edition synthesis.

Related Information

- Verify Verilog Compilation Unit on page 98
- Update Entity Auto-Discovery on page 99
- Ensure Distinct VHDL Namespace for Each Library on page 100
- Remove Unsupported Parameter Passing on page 100
- Remove Unsized Constant from WYSIWYG Instantiation on page 100
- Remove Non-Standard Pragmas on page 101
- Declare Objects Before Initial Values on page 101
- Confine SystemVerilog Features to SystemVerilog Files on page 101
- Avoid Assignment Mixing in Always Blocks on page 102
- Avoid Unconnected, Non-Existent Ports on page 102
- Avoid Illegal Parameter Ranges on page 102
- Update Verilog HDL and VHDL Type Mapping on page 103

5.4.1. Verify Verilog Compilation Unit

Intel Quartus Prime Pro Edition synthesis uses a different method to define the compilation unit. The Verilog LRM defines the concept of compilation unit as "a collection of one or more Verilog source files compiled together" forming the compilation-unit scope. Items visible only in the compilation-unit scope include macros, global declarations, and default net types. The contents of included files become part of the compilation unit of the parent file. Modules, primitives, programs, interfaces, and packages are visible in all compilation units. Ensure that your RTL accommodates these changes.
Table 20. Verilog Compilation Unit Differences

<table>
<thead>
<tr>
<th>Other Quartus Software Products</th>
<th>Intel Quartus Prime Pro Edition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Synthesis in other Quartus software products follows the Multi-file compilation unit (MFCU) method to select compilation unit files. In MFCU, all files compile in the same compilation unit. Global definitions and directives are visible in all files. However, the default net type is reset at the start of each file.</td>
<td>Intel Quartus Prime Pro Edition synthesis follows the Single-file compilation unit (SFCU) method to select compilation unit files. In SFCU, each file is a compilation unit, file order is irrelevant, and the macro is only defined until the end of the file.</td>
</tr>
</tbody>
</table>

Note: You can optionally change the MFCU mode using the following assignment:
```
set_global_assignment -name VERILOG_CU_MODE MFCU
```

5.4.1.1. Verilog HDL Configuration Instantiation

Intel Quartus Prime Pro Edition synthesis requires instantiation of the Verilog HDL configuration, and not the module. In other Quartus software products, synthesis automatically finds any Verilog HDL configuration relating to a module that you instantiate. The Verilog HDL configuration then instantiates the design.

If your top-level entity is a Verilog HDL configuration, set the Verilog HDL configuration, rather than the module, as the top-level entity.

Table 21. Verilog HDL Configuration Instantiation

<table>
<thead>
<tr>
<th>Other Quartus Software Products</th>
<th>Intel Quartus Prime Pro Edition</th>
</tr>
</thead>
<tbody>
<tr>
<td>From the Example RTL, synthesis automatically finds the mid_config Verilog HDL configuration relating to the instantiated module.</td>
<td>From the Example RTL, synthesis does not find the mid_config Verilog HDL configuration. You must instantiate the Verilog HDL configuration directly.</td>
</tr>
</tbody>
</table>

Example RTL:
```
config mid_config;
design good_lib.mid;
instance mid.sub_inst use good_lib.sub;
endconfig

module test (input a1, output b);
mid_config mid_inst ( .a1(a1), .b(b));
// in other Quartus products preceding line would have been:
//mid mid_inst ( .a1(a1), .b(b));
enmodule

module mid (input a1, output b);
sub sub_inst (.a1(a1), .b(b));
enmodule
```

5.4.2. Update Entity Auto-Discovery

All editions of the Intel Quartus Prime and Quartus II software search your project directory for undefined entities. For example, if you instantiate entity “sub” in your design without specifying “sub” as a design file in the Quartus Settings File (.qsf), synthesis searches for sub.v, sub.vhd, and so on. However, Intel Quartus Prime Pro Edition performs auto-discovery at a different stage in the flow. Ensure that your RTL code accommodates these auto-discovery changes.
Table 22. Entity Auto-Discovery Differences

<table>
<thead>
<tr>
<th>Other Quartus Software Products</th>
<th>Intel Quartus Prime Pro Edition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Always automatically searches your project directory and search path for undefined entities.</td>
<td>Always automatically searches your project directory and search path for undefined entities. Intel Quartus Prime Pro Edition synthesis performs auto-discovery earlier in the flow than other Quartus software products. This results in discovery of more syntax errors. Optionally disable auto-discovery with the following .qsf assignment: set_global_assignment -name AUTO_DISCOVER_AND_SORT OFF</td>
</tr>
</tbody>
</table>

5.4.3. Ensure Distinct VHDL Namespace for Each Library

Intel Quartus Prime Pro Edition synthesis requires that VHDL namespaces are distinct for each library. The stricter library binding requirement complies with VHDL language specifications and results in deterministic behavior. This benefits team-based projects by avoiding unintentional name collisions. Confirm that your RTL respects this change.

Table 23. VHDL Namespace Differences

<table>
<thead>
<tr>
<th>Other Quartus Software Products</th>
<th>Intel Quartus Prime Pro Edition</th>
</tr>
</thead>
<tbody>
<tr>
<td>For the Example RTL, the analyzer searches all libraries in an unspecified order until the analyzer finds package utilities_pack and uses items from that package. If another library, for example projectLib also contains utilities_pack, the analyzer may use this library instead of myLib.utilities_pack if found before the analyzer searches myLib.</td>
<td>For the Example RTL, the analyzer uses the specific utilities_pack in myLib. If utilities_pack does not exist in library myLib, the analyzer generates an error.</td>
</tr>
</tbody>
</table>

Example RTL:

```vhdl
library myLib; use myLib.utilities_pack.all;
```

5.4.4. Remove Unsupported Parameter Passing

Intel Quartus Prime Pro Edition synthesis does not support parameter passing using set_parameter in the .qsf. Synthesis in other Quartus software products supports passing parameters with this method. Except for the top-level of the design where permitted, ensure that your RTL does not depend on this type of parameter passing.

Table 24. SystemVerilog Feature Differences

<table>
<thead>
<tr>
<th>Other Quartus Software Products</th>
<th>Intel Quartus Prime Pro Edition</th>
</tr>
</thead>
<tbody>
<tr>
<td>From the Example RTL, synthesis overwrites the value of parameter SIZE in the instance of my_ram instantiated from entity mid-level.</td>
<td>From the Example RTL, synthesis generates a syntax error for detection of parameter passing assignments in the .qsf. Specify parameters in the RTL. The following example shows the supported top-level parameter passing format. This example applies only to the top-level and sets a value of 4 to parameter N: set_parameter -name N 4</td>
</tr>
</tbody>
</table>

Example RTL:

```vhdl
set_parameter -entity mid_level -to my_ram -name SIZE 16
```

5.4.5. Remove Unsized Constant from WYSIWYG Instantiation

Intel Quartus Prime Pro Edition synthesis does not allow use of an unsized constant for WYSIWYG instantiation. Synthesis in other Quartus software products allows use of SystemVerilog (.sv) unsized constants when instantiating a WYSIWYG in a .v file.
Intel Quartus Prime Pro Edition synthesis allows use of unsized constants in .sv files for uses other than WYSIWYG instantiation. Ensure that your RTL code does not use unsized constants for WYSIWYG instantiation. For example, specify a sized literal, such as 2'b11, rather than '1.

### 5.4.6. Remove Non-Standard Pragmas

Intel Quartus Prime Pro Edition synthesis does not support the vhdl(verilog)_input_version pragma or the library pragma. Synthesis in other Quartus software products supports these pragmas. Remove any use of the pragmas from RTL for Intel Quartus Prime Pro Edition migration. Use the following guidelines to implement the pragma functionality in Intel Quartus Prime Pro Edition:

- **vhdl(verilog)_input_version** Pragma—allows change to the input version in the middle of an input file. For example, to change VHDL 1993 to VHDL 2008. For Intel Quartus Prime Pro Edition migration, specify the input version for each file in the .qsf.
- **library** Pragma—allows changes to the VHDL library into which files compile. For Intel Quartus Prime Pro Edition migration, specify the compilation library in the .qsf.

### 5.4.7. Declare Objects Before Initial Values

Intel Quartus Prime Pro Edition synthesis requires declaration of objects before initial value. Ensure that your RTL declares objects before initial value. Other Quartus software products allow declaration of initial value prior to declaration of the object.

<table>
<thead>
<tr>
<th>Table 25. Object Declaration Differences</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Other Quartus Software Products</strong></td>
</tr>
<tr>
<td>From the Example RTL, synthesis initializes the output p_prog_io1 with the value of p_progio1_reg, even though the register declaration occurs in Line 2.</td>
</tr>
<tr>
<td><strong>Example RTL:</strong></td>
</tr>
<tr>
<td>1 output p_prog_io1 = p_progio1_reg;</td>
</tr>
</tbody>
</table>

### 5.4.8. Confine SystemVerilog Features to SystemVerilog Files


To use SystemVerilog features in your existing Verilog HDL files, rename your Verilog HDL (.v) files as SystemVerilog (.sv) files. Alternatively, you can set the file type in the .qsf, as shown in the following example:

```qsf
set_global_assignment -name SYSTEMVERILOG_FILE <file>.v
```
Table 26. SystemVerilog Feature Differences

<table>
<thead>
<tr>
<th>Other Quartus Software Products</th>
<th>Intel Quartus Prime Pro Edition</th>
</tr>
</thead>
<tbody>
<tr>
<td>From the Example RTL, synthesis interprets $clog2 in a .v file, even though the Verilog LRM does not define the $clog2 feature. Other Quartus software products allow other SystemVerilog features in .v files.</td>
<td>From the Example RTL, synthesis generates a syntax error for detection of any non-Verilog HDL construct in .v files. Intel Quartus Prime Pro Edition synthesis honors SystemVerilog features only in .sv files.</td>
</tr>
</tbody>
</table>

Example RTL:

```verbatim
localparam num_mem_locations = 1050;
wire mem_addr [$clog2(num_mem_locations)-1 : 0];
```

5.4.9. Avoid Assignment Mixing in Always Blocks

Intel Quartus Prime Pro Edition synthesis does not allow mixed use of blocking and non-blocking assignments within ALWAYS blocks. Other Quartus software products allow mixed use of blocking and non-blocking assignments within ALWAYS blocks. To avoid syntax errors, ensure that ALWAYS block assignments are of the same type for Intel Quartus Prime Pro Edition migration.

Table 27. ALWAYS Block Assignment Differences

<table>
<thead>
<tr>
<th>Other Quartus Software Products</th>
<th>Intel Quartus Prime Pro Edition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Synthesis honors the mixed blocking and non-blocking assignments, although the Verilog Language Specification no longer supports this construct.</td>
<td>Synthesis generates a syntax error for detection of mixed blocking and non-blocking assignments within an ALWAYS block.</td>
</tr>
</tbody>
</table>

5.4.10. Avoid Unconnected, Non-Existential Ports

Intel Quartus Prime Pro Edition synthesis requires that a port exists in the module prior to instantiation and naming. Other Quartus software products allow you to instantiate and name an unconnected port that does not exist in the module. Modify your RTL to match this requirement.

To avoid syntax errors, remove all unconnected and non-existent ports for Intel Quartus Prime Pro Edition migration.

Table 28. Unconnected, Non-Existential Port Differences

<table>
<thead>
<tr>
<th>Other Quartus Software Products</th>
<th>Intel Quartus Prime Pro Edition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Synthesis allows you to instantiate and name unconnected or non-existent ports that do not exist on the module.</td>
<td>Synthesis generates a syntax error for detection of mixed blocking and non-blocking assignments within an ALWAYS block.</td>
</tr>
</tbody>
</table>

5.4.11. Avoid Illegal Parameter Ranges

Intel Quartus Prime Pro Edition synthesis generates an error for detection of constant numeric (integer or floating point) parameter values that exceed the language specification. Other Quartus software products allow constant numeric (integer or floating point) values for parameters that exceed the language specifications. To avoid syntax errors, ensure that constant numeric (integer or floating point) values for parameters conform to the language specifications.
5.4.12. Update Verilog HDL and VHDL Type Mapping

Intel Quartus Prime Pro Edition synthesis requires that you use 0 for "false" and 1 for "true" in Verilog HDL files (.v). Other Quartus software products map "true" and "false" strings in Verilog HDL to TRUE and FALSE Boolean values in VHDL. Intel Quartus Prime Pro Edition synthesis generates an error for detection of non-Verilog HDL constructs in .v files. To avoid syntax errors, ensure that your RTL accommodates these standards.

5.5. Migrating to Intel Quartus Prime Pro Edition Revision History

This chapter has the following revision history.

<table>
<thead>
<tr>
<th>Document Version</th>
<th>Intel Quartus Prime Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>2018.09.24</td>
<td>18.1.0</td>
<td>Added information about removing assignments from the qsf file that point to legacy output files.</td>
</tr>
<tr>
<td>2018.05.07</td>
<td>18.0.0</td>
<td>First release as separate chapter of Getting Started User Guide.</td>
</tr>
</tbody>
</table>
| 2017.11.06       | 17.1.0                      | • Added Verilog HDL Macro example.  
                     |                | • Updated for latest Intel branding conventions. |
| 2017.05.08       | 17.0.0                      | • Removed statement about limitations for safe state machines. The Compiler supports safe state machines. State machine inference is enabled by default. |
| 2016.10.31       | 16.1.0                      | • Implemented Intel rebranding.  
                     |                | • Described unsupported Intel Quartus Prime Standard Edition physical synthesis options.  
                     |                | • Changed title from "Remove Filling Vectors" to "Remove Unsized Constant". |
| 2016.05.03       | 16.0.0                      | • Added topic on Safe State Machine encoding.  
                     |                | • Corrected statement about Verilog Compilation Unit.  
                     |                | • Corrected typo in Modify Entity Name Assignments.  
                     |                | • Clarified limitations for multiple Logic Lock instances in the same region. |
| 2015.11.02       | 15.1.0                      | • First version of document. |
A. Intel Quartus Prime Pro Edition User Guides

Refer to the following user guides for comprehensive information on all phases of the Intel Quartus Prime Pro Edition FPGA design flow.

Related Information

  Introduces the basic features, files, and design flow of the Intel Quartus Prime Pro Edition software, including managing Intel Quartus Prime Pro Edition projects and IP, initial design planning considerations, and project migration from previous software versions.

  Describes creating and optimizing systems using Platform Designer, a system integration tool that simplifies integrating customized IP cores in your project. Platform Designer automatically generates interconnect logic to connect intellectual property (IP) functions and subsystems.

  Describes best design practices for designing FPGAs with the Intel Quartus Prime Pro Edition software. HDL coding styles and synchronous design practices can significantly impact design performance. Following recommended HDL coding styles ensures that Intel Quartus Prime Pro Edition synthesis optimally implements your design in hardware.

  Describes set up, running, and optimization for all stages of the Intel Quartus Prime Pro Edition Compiler. The Compiler synthesizes, places, and routes your design before generating a device programming file.

  Describes Intel Quartus Prime Pro Edition settings, tools, and techniques that you can use to achieve the highest design performance in Intel FPGAs. Techniques include optimizing the design netlist, addressing critical chains that limit retiming and timing closure, optimizing device resource usage, device floorplanning, and implementing engineering change orders (ECOs).

  Describes operation of the Intel Quartus Prime Pro Edition Programmer, which allows you to configure Intel FPGA devices, and program CPLD and configuration devices, via connection with an Intel FPGA download cable.

- Intel Quartus Prime Pro Edition User Guide: Block-Based Design
  Describes block-based design flows, also known as modular or hierarchical design flows. These advanced flows enable preservation of design blocks (or logic that comprises a hierarchical design instance) within a project, and reuse of design blocks in other projects.
• **Intel Quartus Prime Pro Edition User Guide: Partial Reconfiguration**
  Describes Partial Reconfiguration, an advanced design flow that allows you to reconfigure a portion of the FPGA dynamically, while the remaining FPGA design continues to function. Define multiple personas for a particular design region, without impacting operation in other areas.

• **Intel Quartus Prime Pro Edition User Guide: Third-party Simulation**
  Describes RTL- and gate-level design simulation support for third-party simulation tools by Aldec*, Cadence*, Mentor Graphics*, and Synopsys that allow you to verify design behavior before device programming. Includes simulator support, simulation flows, and simulating Intel FPGA IP.

• **Intel Quartus Prime Pro Edition User Guide: Third-party Synthesis**
  Describes support for optional synthesis of your design in third-party synthesis tools by Mentor Graphics*, and Synopsys. Includes design flow steps, generated file descriptions, and synthesis guidelines.

• **Intel Quartus Prime Pro Edition User Guide: Third-party Logic Equivalence Checking Tools**
  Describes support for optional logic equivalence checking (LEC) of your design in third-party LEC tools by OneSpin*. Describes how to verify the logic equivalence between compilation netlists.

• **Intel Quartus Prime Pro Edition User Guide: Debug Tools**
  Describes a portfolio of Intel Quartus Prime Pro Edition in-system design debugging tools for real-time verification of your design. These tools provide visibility by routing (or “tapping”) signals in your design to debugging logic. These tools include System Console, Signal Tap logic analyzer, Transceiver Toolkit, In-System Memory Content Editor, and In-System Sources and Probes Editor.

• **Intel Quartus Prime Pro Edition User Guide: Timing Analyzer**
  Explains basic static timing analysis principals and use of the Intel Quartus Prime Pro Edition Timing Analyzer, a powerful ASIC-style timing analysis tool that validates the timing performance of all logic in your design using an industry-standard constraint, analysis, and reporting methodology.

• **Intel Quartus Prime Pro Edition User Guide: Power Analysis and Optimization**
  Describes the Intel Quartus Prime Pro Edition Power Analysis tools that allow accurate estimation of device power consumption. Estimate the power consumption of a device to develop power budgets and design power supplies, voltage regulators, heat sink, and cooling systems.

• **Intel Quartus Prime Pro Edition User Guide: Design Constraints**
  Describes timing and logic constraints that influence how the Compiler implements your design, such as pin assignments, device options, logic options, and timing constraints. Use the Interface Planner to prototype interface implementations, plan clocks, and quickly define a legal device floorplan. Use the Pin Planner to visualize, modify, and validate all I/O assignments in a graphical representation of the target device.

• **Intel Quartus Prime Pro Edition User Guide: PCB Design Tools**
  Describes support for optional third-party PCB design tools by Mentor Graphics* and Cadence*. Also includes information about signal integrity analysis and simulations with HSPICE and IBIS Models.
  Describes use of Tcl and command line scripts to control the Intel Quartus Prime Pro Edition software and to perform a wide range of functions, such as managing projects, specifying constraints, running compilation or timing analysis, or generating reports.
# 7. Document Archives

If an Intel Quartus Prime version is not listed, the user guide for the previous Intel Quartus Prime version applies.

<table>
<thead>
<tr>
<th>Intel Quartus Prime Version</th>
<th>User Guide</th>
</tr>
</thead>
</table>