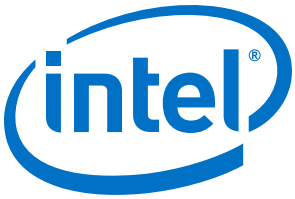

Serial Lite III Streaming Intel Stratix 10 FPGA IP Design Example User Guide

Updated for Intel® Quartus® Prime Design Suite: **18.1**

UG-20065 | 2018.12.28
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Contents

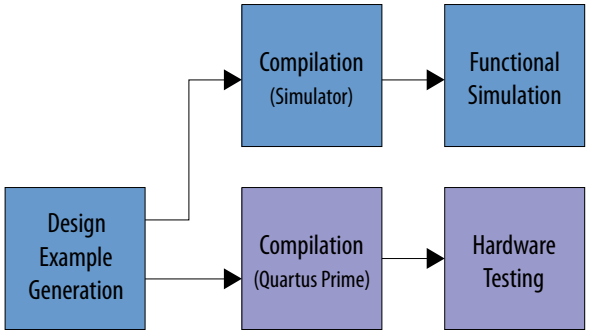
1. Quick Start Guide

The Serial Lite III Streaming Intel® FPGA IP provides the capability of generating design examples for selected configurations.

The Serial Lite III Streaming Intel FPGA IP offers eight preset settings for Intel Stratix® 10 H-tile and L-tile devices in both simplex and duplex modes and Intel Stratix 10 E-tile devices in duplex mode.

- Standard Clocking Mode 6x12.5G
- Standard Clocking Mode 6x17.4G
- Standard Clocking Mode 2x25G
- Standard Clocking Mode 4x28G
- Advanced Clocking Mode 6x12.5G
- Advanced Clocking Mode 6x17.4G
- Advanced Clocking Mode 2x25G
- Advanced Clocking Mode 4x28G

Figure 1. Development Stages for the Design Example



Related Information

- Serial Lite III Knowledge Base
- Serial Lite III Streaming IP Core User Guide

1.1. Directory Structure

The Intel Quartus® Prime software generates the design example files in the following folders:

- `<user_defined_design_example_directory>/ed_sim`
- `<user_defined_design_example_directory>/ed_synth`
- `<user_defined_design_example_directory>/ed_hwtest`

The following diagrams show the directories that contain the generated files for the design examples.

Figure 2. Directory Structure for Intel Stratix 10 Serial Lite III Streaming Design Example

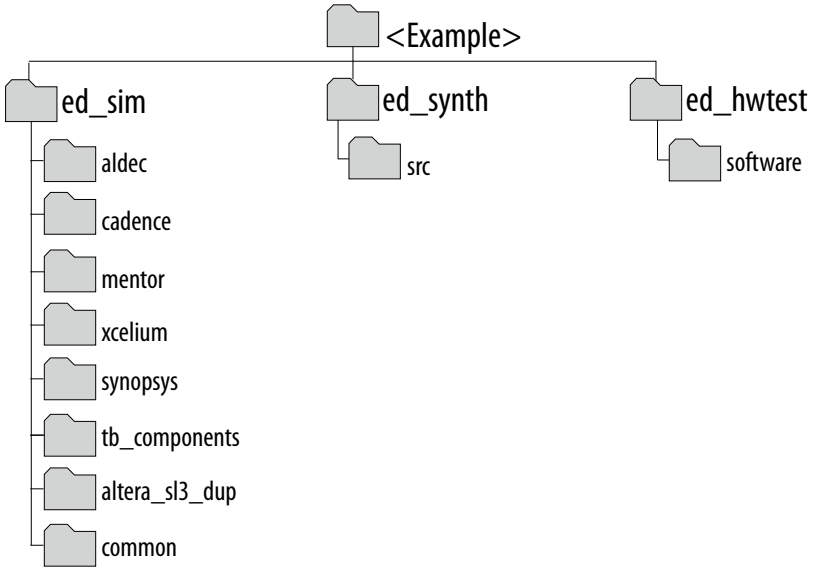


Table 1. Directory and File Description for Design Example Folder

Directory/File	Description
`ed_sim/tb_components`	The folder that contains the testbench files.
`ed_sim/common`	The folder that contains the `.tcl` scripts for all the simulators.

`ed_sim/cadence`
`ed_sim/aldec`
`ed_sim/mentor`
`ed_sim/xcelium`
`ed_sim/synopsys/vcs` or `ed_sim/synopsys/vcsmx`
	The folder that contains the simulation script. It also serves as a working area for the simulator.

`ed_sim/altera_sl3_dup`	The folder that contains the design example simulation source files.
`ed_synth/seriallite_iii_streaming_demo.qpf`	Quartus project file.
`ed_synth/seriallite_iii_streaming_demo.qsf`	Quartus settings file.
`ed_synth/seriallite_iii_streaming_demo.sdc`	Synopsys Design Constraints (SDC) file.
`ed_synth/src`	The folder that contains the design example synthesizable components.
`ed_synth/src/seriallite_iii_streaming_demo.v`	Design example top-level HDL.

continued...

Directory/File	Description
ed_synth/altera_sl3_dup/synth/altera_sl3_dup.v	Design example DUT top-level files.
ed_synth/demo_control	The folder for each synthesizable component including Platform Designer generated IPs, such as demo_mgmt and demo_control.
ed_hwtest	The folder that contains the design example hardware setup files.
ed_hwtest/Readme.txt	Instruction file to download the generated design example on the development kit.
ed_hwtest/master_export.v	User interface Verilog design file. This file is available when you instantiate a design with Synthesis enabled.
ed_hwtest/master_export_hw.tcl	Component description file for master export custom IP. This file is available when you instantiate a design with Synthesis enabled.
ed_hwtest/software	The folder that contains scripts to download the demo_control program into Nios® II processor and open an interactive terminal to run the design example.

1.2. Design Example Block Diagrams

Figure 3. High-Level Block Diagram for Intel Stratix 10 H-tile and L-tile Design Examples

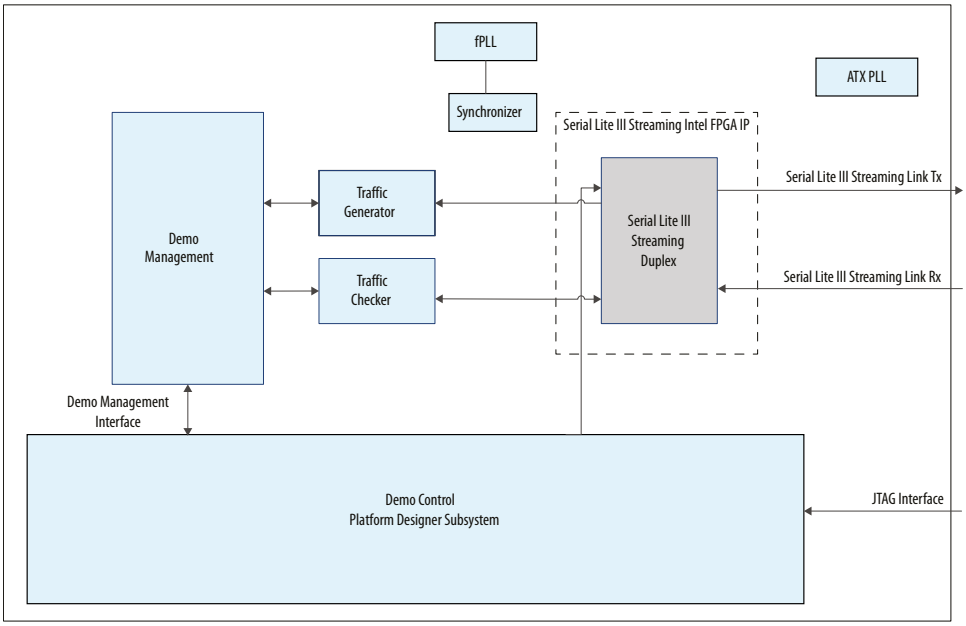
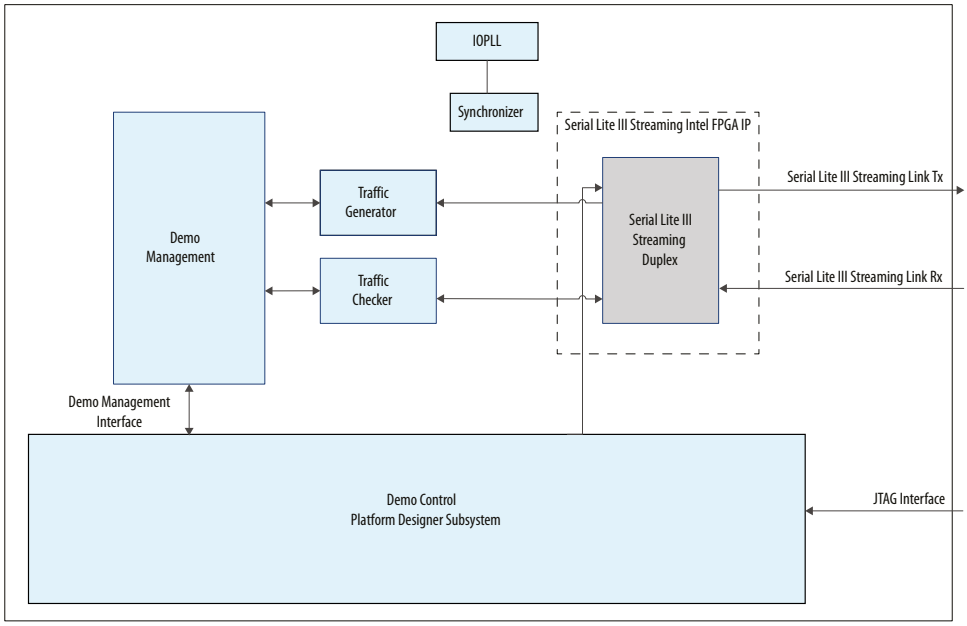


Figure 4. High-Level Block Diagram for Intel Stratix 10 E-tile Design Examples



1.3. Generating the Design

You can use the Serial Lite III Streaming IP core parameter editor in the Intel Quartus Prime software to generate the design example.

Figure 5. Procedure

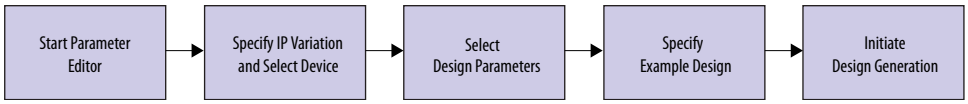
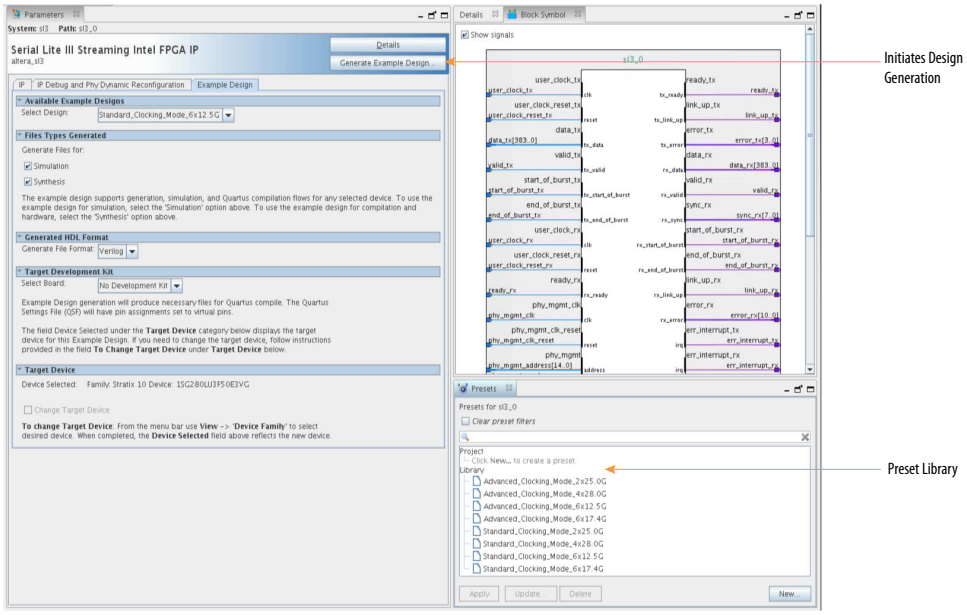


Figure 6. Example Design Tab



1.3.1. Procedure

This is a general procedure on how to generate the design example.

To generate the design example from the IP parameter editor:

1. In the IP Catalog (`Tools > IP Catalog`), locate and select **Serial Lite III Streaming**. The IP parameter editor appears.
2. Specify a top-level name and the folder for your custom IP variation. Click **OK**.
3. Select a design from the **Presets** library and click **Apply**. When you select a design, the system automatically populates the IP parameters for the design.

   Note: If you select another design, the settings of the IP parameters change accordingly.
4. Specify the parameters for your design.
5. Click the **Generate Example Design** button.

The software generates all design files in the sub-directories. These files are required to run simulation, compilation, and hardware testing.

1.3.2. Design Example Parameters

The Serial Lite III Streaming IP parameter editor includes an *Example Design* tab for you to specify certain parameters before generating the design example.

Table 2. Parameters in the Example Design Tab

Parameter	Description
Select Design	Available example designs for the IP parameter settings. When you select a design from the Preset library, this field shows the selected design.
Generate Files for	The files to generate for different development phases. Simulation—when selected, the necessary files for simulating the design example are generated. Synthesis—when selected, the synthesis files are generated. Use these files to compile the design in the Intel Quartus Prime software for hardware testing.
Generate File Format	The format of the RTL files for simulation—Verilog or VHDL.
Select Board	Supported hardware for design implementation. When you select an Intel FPGA development board, the *Target Device* is the one that matches the device on the Development Kit. If this menu is grayed out, there is no supported board for the options that you select. **Intel Stratix 10 GX Signal Integrity Development Kit:** This option allows you to test the design example on selected Intel FPGA IP development kit. This selection automatically selects the *Target Device* to match the device on the Intel FPGA IP development kit. If your board revision has a different speed grade, you can change the target device. **Custom Development Kit:** This option allows you to test the design example on a third party development kit with Intel FPGA IP device, a custom designed board with Intel FPGA IP device, or a standard Intel FPGA IP development kit not available for selection. You can also select a custom device for the custom development kit. **No Development Kit**: This option excludes the hardware aspects for the design example.
Change Target Device	Select a different device grade for Intel FPGA IP development kit. For device-specific details, refer to the device datasheet on the Intel FPGA website.

1.3.3. Presets

Standard presets allow instant entry of pre-selected parameter values in the **IP** and **Example Design** tabs. You can select the presets at the lower right window in the parameter editor.

The parameter values chosen for the presets belong to the group of supported Serial Lite III Streaming IP configurations for design example generation. You can select one of the presets available for your target device to quickly generate a design example without having to manually set each parameter in the **IP** tab and verifying that the parameter matches the supported configurations set. There are eight preset settings available in the library that support Duplex, Sink and Source modes:

- Standard Clocking Mode 6x12.5G
- Standard Clocking Mode 6x17.4G
- Standard Clocking Mode 2x25G
- Standard Clocking Mode 4x28G
- Advanced Clocking Mode 6x12.5G
- Advanced Clocking Mode 6x17.4G
- Advanced Clocking Mode 2x25G
- Advanced Clocking Mode 4x28G

Note: Serial Lite III Streaming Intel FPGA IP design examples for Intel Stratix 10 devices are only available in Intel Quartus Prime Pro Edition.

Table 3. Parameter Settings for Intel Stratix 10 Design Example Standard Clocking Presets

Presets	Standard Clocking Mode 6x12.5G	Standard Clocking Mode 6x17.4G	Standard Clocking Mode 2x25G	Standard Clocking Mode 4x28G
Direction	• Simplex and Duplex (H-tile and L-tile) • Duplex (E-tile)	• Simplex and Duplex (H-tile and L-tile) • Duplex (E-tile)	• Simplex and Duplex (H-tile and L-tile) • Duplex (E-tile)	• Simplex and Duplex (H-tile and L-tile) • Duplex (E-tile)
Number of lanes	6	6	2	4
Meta frame length in words	200	200	200	200
Transceiver reference clock frequency (MHz)	312.5	600.0	312.5	200.0
Enable M20K ECC support	ON/OFF The default value is OFF.	ON/OFF The default value is OFF.	ON/OFF The default value is OFF.	ON/OFF The default value is OFF.
Clocking Mode	Standard clocking mode	Standard clocking mode	Standard clocking mode	Standard clocking mode
Required user clock frequency (MHz)	177.556818	247.159091	355.113636	397.727273
Transceiver data rate (Gbps)	12.5	17.4	25.0	28.0
Streaming Mode	Full	Full	Full	Full
VCCR_GXB and VCCT_GXB supply voltage for the transceiver	1.0 V (applicable only for L-tile and H-tile devices)	1.0 V (applicable only for L-tile and H-tile devices)	1.1 (applicable only for L-tile and H-tile devices)	1.1 (applicable only for L-tile and H-tile devices)
Transceiver Channel Type	GX (applicable only for L-tile and H-tile devices)	GX (applicable only for L-tile and H-tile devices)	GXT (applicable only for L-tile and H-tile devices)	GXT (applicable only for L-tile and H-tile devices)
Transceiver Tile	L-tile, H-tile, and E-tile devices	L-tile, H-tile, and E-tile devices	L-tile, H-tile, and E-tile devices	L-tile, H-tile, and E-tile devices

Table 4. Parameter Settings for Intel Stratix 10 Design Example Advanced Clocking Presets

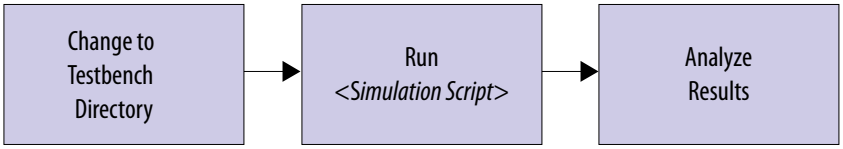
Presets	Advanced Clocking Mode 6x12.5G	Advanced Clocking Mode 6x17.4G	Advanced Clocking Mode 2x25G	Advanced Clocking Mode 4x28G
Direction	• Simplex and Duplex (H-tile and L-tile) • Duplex (E-tile)	• Simplex and Duplex (H-tile and L-tile) • Duplex (E-tile)	• Simplex and Duplex (H-tile and L-tile) • Duplex (E-tile)	• Simplex and Duplex (H-tile and L-tile) • Duplex (E-tile)
Number of lanes	6	6	2	4
Meta frame length in words	200	200	200	200
Transceiver reference clock frequency (MHz)	312.5	600.0	312.5	200.0

continued...

Presets	Advanced Clocking Mode 6x12.5G	Advanced Clocking Mode 6x17.4G	Advanced Clocking Mode 2x25G	Advanced Clocking Mode 4x28G
Enable M20K ECC support	ON/OFF The default value is OFF.	ON/OFF The default value is OFF.	ON/OFF The default value is OFF.	ON/OFF The default value is OFF.
Clocking Mode	Advanced clocking mode	Advanced clocking mode	Advanced clocking mode	Advanced clocking mode
Required user clock frequency (MHz)	182.835821	254.507463	365.671642	409.552239
Transceiver data rate (Gbps)	12.5	17.4	25.0	28.0
Streaming Mode	Full	Full	Full	Full
VCCR_GXB and VCCT_GXB supply voltage for the transceiver	1.0 V (applicable only for L-tile and H-tile devices)	1.0 V (applicable only for L-tile and H-tile devices)	1.1 (applicable only for L-tile and H-tile devices)	1.1 (applicable only for L-tile and H-tile devices)
Transceiver Channel Type	GX (applicable only for L-tile and H-tile devices)	GX (applicable only for L-tile and H-tile devices)	GXT (applicable only for L-tile and H-tile devices)	GXT (applicable only for L-tile and H-tile devices)
Transceiver Tile	L-tile, H-tile, and E-tile devices	L-tile, H-tile, and E-tile devices	L-tile, H-tile, and E-tile devices	L-tile, H-tile, and E-tile devices

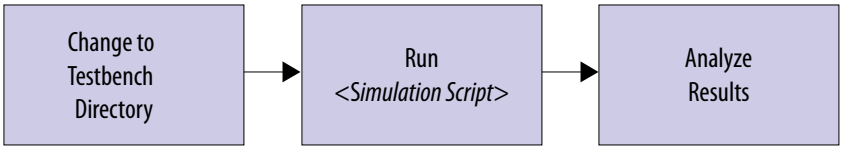
1.4. Simulating the Design

These general steps describe how to compile and run the design example simulation. For specific commands for each design example variant, refer to its respective section.



1.4.1. Procedure

To compile and simulate the design:



1. Change the working directory to <*example_design_directory*>/ed_sim/<*simulator*>.
2. Run the simulation script for the simulator of your choice.

Simulator	Command
ModelSim*	`do run_tb.tcl`
VCS*/VCS MX	`sh run_tb.sh`

continued...

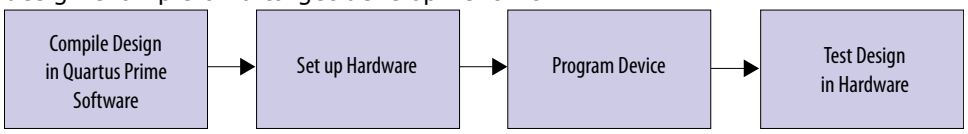
Simulator	Command
Riviera-PRO* *Note:* This simulator is not supported for Intel Stratix 10 E-tile design examples.	`do run_tb.tcl`
NCSim	`sh run_tb.sh`
Xcelium*	`sh run_tb.sh`

A successful simulation ends with the following message, "Test Passed."

After successful completion, you can analyze the results.

1.5. Compiling and Testing the Design

The Serial Lite III Streaming IP Core parameter editor allows you to compile and run the design example on a target development kit.



Follow these steps to compile and test the design in hardware:

1. Launch the Intel Quartus Prime software and change the directory to `example_design_dir/ed_synth/` and open the `seriallite_iii_streaming_demo.qpf` file.
2. Click **Processing**> **Start Compilation** to compile the design.

   The timing constraints for the design example and the design components are automatically loaded during compilation.
3. Connect the development board to the host computer.
4. Configure the FPGA on the development board using the generated **.sof** file (**Tools**> **Programmer**).

The design examples target the Intel Stratix 10 GX and Intel Stratix 10 TX Signal Integrity Development Kits.

The design includes an SDC script as well as a QSF with verified constraints in loopback mode. If you use the design example with another device or development board, you may need to update the device setting and constraints in the QSF file.

You must use correct pin constraints when using the core in simplex mode.

Note: The Intel Stratix 10 E-tile designs do not support simplex mode.

Related Information

Serial Lite III Streaming IP Core User Guide

2. Detailed Description for Intel Stratix 10 H-tile and L-tile Serial Lite III Streaming Standard Clocking Mode Design Example

This design example demonstrates the functionality of data streaming using standard clocking mode.

To generate the design example, select any of the following presets:

- Standard Clocking Mode 2x25.0G
- Standard Clocking Mode 4x28.0G
- Standard Clocking Mode 6x12.5G
- Standard Clocking Mode 6x17.4G

Note: By default, the design examples are generated as duplex core. To generate the design examples in simplex core, select **Simplex** for the **Direction** parameter.

2.1. Features

Features for Standard Clocking Mode design example includes:

- Support up to 12 lanes for 17.4 Gbps and 4 lanes for 28 Gbps transceiver data rate
- Support for simplex and duplex transmission mode
- Traffic checker for data verification and lane de-skew verification
- Support for CRC error injection using Nios II processor
- Slave test mode for master and slave testing

2.2. Hardware and Software Requirements

Intel uses the following hardware and software to test the example designs in a Linux system:

- Intel Quartus Prime software
- ModelSim, Riviera-PRO, Xcelium, NCSim (Verilog only), or VCS/VCS MX simulator
- Intel Stratix 10 GX Signal Integrity Development Kit (1SG280HU1F50E2VG) for hardware testing

2.3. Functional Description

The Intel Stratix 10 H-tile and L-tile design examples consist of various components. The following block diagrams show the design components and the top level connections of the design examples.

Figure 7. Design Example for Simplex Core in Standard Clocking Mode

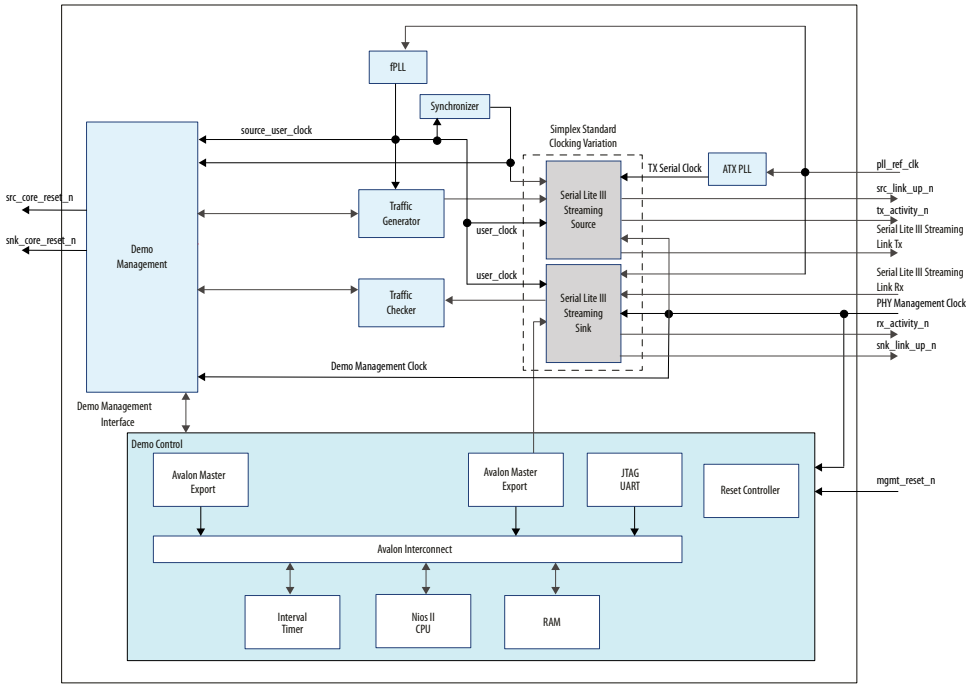
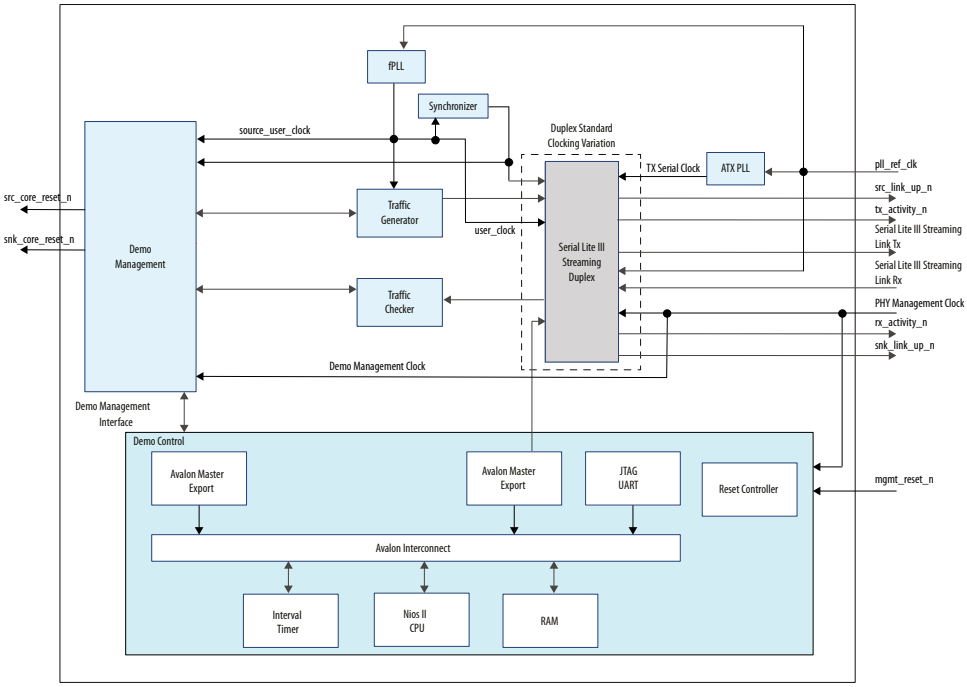


Figure 8. Design Example for Duplex Core in Standard Clocking Mode



2.3.1. Design Example Components

The design example consists of the following components:

- Serial Lite III Streaming IP core variation
- Source and sink user clock—fPLL
- ATX PLL
- Traffic generator
- Traffic checker
- Demo control
- Demo management

2.3.1.1. Serial Lite III Streaming IP Core

The Serial Lite III Streaming IP core variation accepts data from the traffic generator and formats the data for transmission. It also receives data from the link, strips the headers, and presents it to the traffic checker for analysis. The core is generated using the parameter editor in the Intel Quartus Prime software.

2.3.1.2. User Clock

The fPLL generates a user clock for sourcing and sinking data into the Serial Lite III Streaming IP core.

2.3.1.3. Traffic Generator

The traffic generator generates traffic in a deterministic format to verify that data is transmitted correctly across the link. Traffic consists of sets of sample words, one for each lane on the link, that are presented to the source user interface.

Figure 9. Traffic Generator Sample Word Format

This figure shows the format of the sample words generated for each lane.

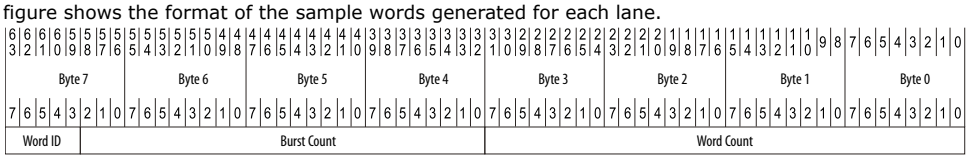


Table 5. Traffic Generator Sample Word Fields

Field	Bits	Description
Word ID	63–59	Contains a static value to distinguish which 64-bit word on the user interface that this sample was presented on. The Word ID value ranges from 0 to (lanes – 1).
Burst Count	58–32	Tracks the number of bursts used to transfer the sample data. This field value starts with one after reset and is incremented each time the `start_of_burst` signal is asserted on the source user interface.
Word Count	31–0	Tracks the number of valid sample words that have been transferred, across all bursts, to the source user interface.

2.3.1.4. Traffic Checker

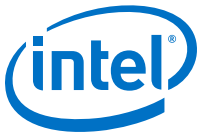
The traffic checker performs the following inspections to verify that the received data conforms to the expected format:

- Checks each sample word to verify that the expected word ID was received.
- Checks each sample word to verify that the word count value is higher than the word count value from the last valid sample word.
- Verifies that lane de-skew has been properly performed by validating that the word count and burst count values from the sample word are the same as the values received from the adjacent lane.
- If the `start_of_burst` signal is asserted on the user interface, verifies that the burst count value in the current sample word is higher than the burst count value from the last valid sample word. Otherwise, it verifies that the burst count value has not changed.

2.3.1.5. Demo Control

The demo control module is a Nios II processor system, generated in Platform Designer (Standard), to control the demo hardware.

Demo control module also consists of a timer to track interrupt occurrence, Avalon-MM interface to access demo management and the Serial Lite III Streaming Intel FPGA IP PHY interface, a reset controller, a UART interface, and an Avalon Streaming (Avalon-ST) interface.



2.3.1.6. Demo Management

The demo management module controls the user modules interaction with the Serial Lite III Streaming IP core such as enable and disable traffic generator and traffic checker, enable CRC error insertion, and provide user clock reset for Serial Lite III Streaming IP core. The module also implements CSRs to control and monitor the design operation. This includes CSRs to monitor and log errors that occur during the operation.

2.3.1.7. Nios II Processor Code

The Nios II processor controls the options exercised in the design example. The code also enables the configuration RAM (CRAM) bits for CRC-32 error injection support.

The design example sets the bit for channel 0 that connects to lane 0 in the design example. Therefore, CRC error injection is exercisable for lane 0 only. Refer to the Nios II processor source code (`demo_control.c`) for information on setting bits for other channels.

The `demo_control.c` program Intel Stratix 10 H-tile and L-tile devices uses the control registers to dynamically toggle the `rx_seriallpbken` port on the Transceiver PHY block to change the TX to RX loopback from internal to external.

2.3.2. Reset Scheme

The `mgmt_reset_n` reset signal controls the overall reset structure for the design example. This is an asynchronous and active-low signal. Asserting this signal resets the demo control module and the Serial Lite III Streaming IP core. The traffic generator and traffic checker modules get reset through the demo management and the reset synchronizer.

The following diagrams show the reset scheme implemented in the design example.

Figure 10. Reset Scheme for Intel Stratix 10 H-tile and L-tile Serial Lite III Streaming Simplex Core in Standard Clocking Mode

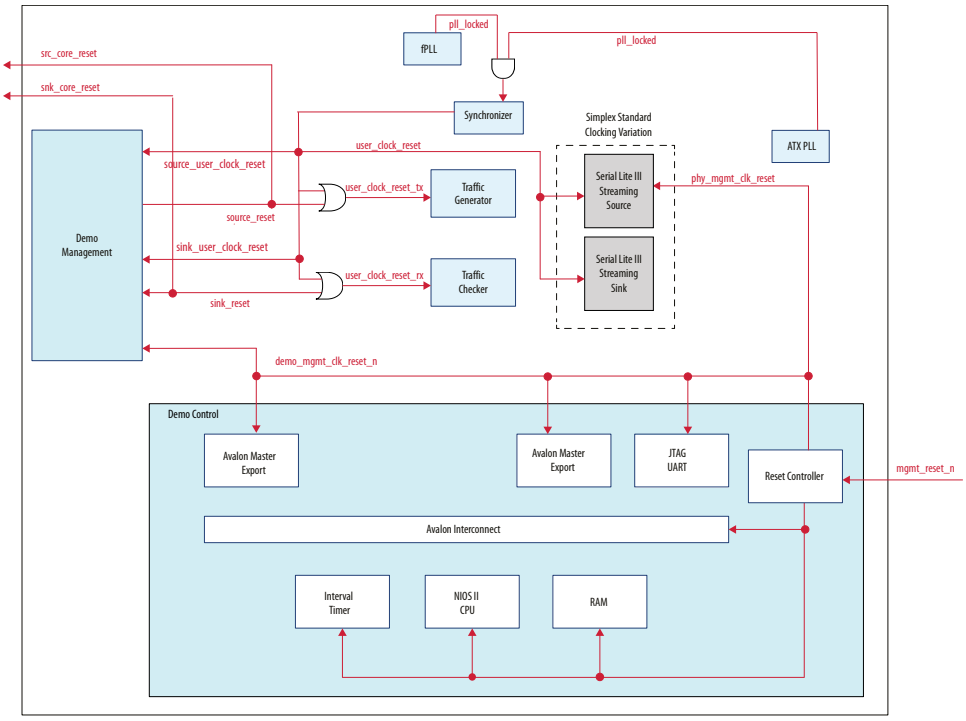
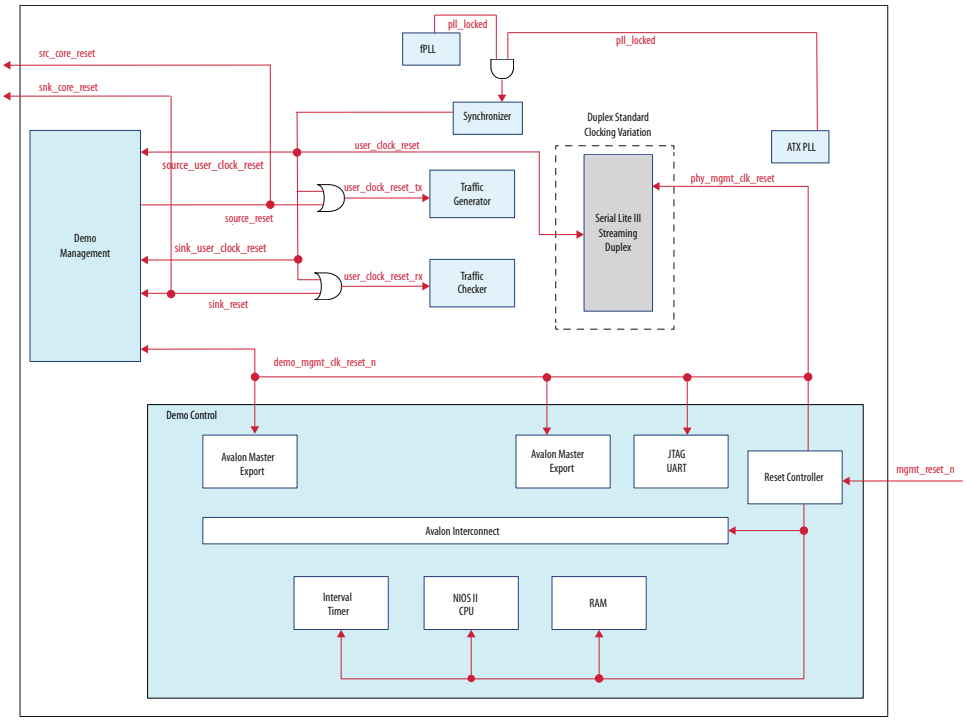


Figure 11. Reset Scheme for Intel Stratix 10 H-tile and L-tile Serial Lite III Streaming Duplex Core in Standard Clocking Mode



2.3.3. Clocking Scheme

The following diagrams show the clocking scheme for the design example.

Figure 12. Clocking Scheme for Intel Stratix 10 H-tile and L-tile Serial Lite III Streaming Simplex Core in Standard Clocking Mode

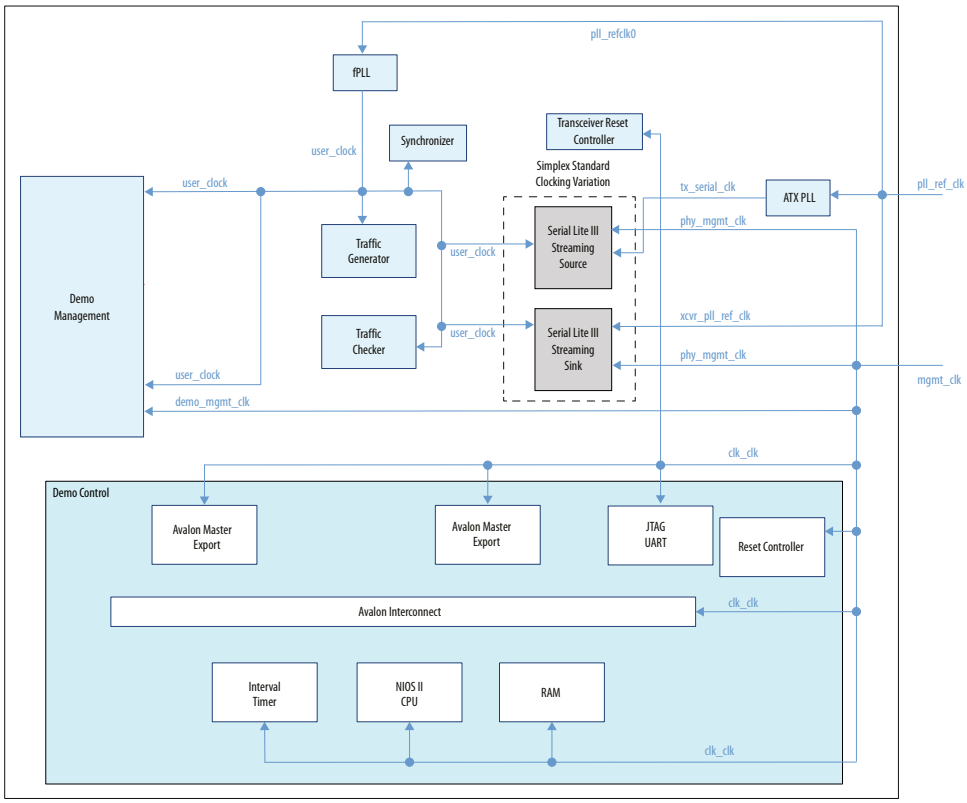
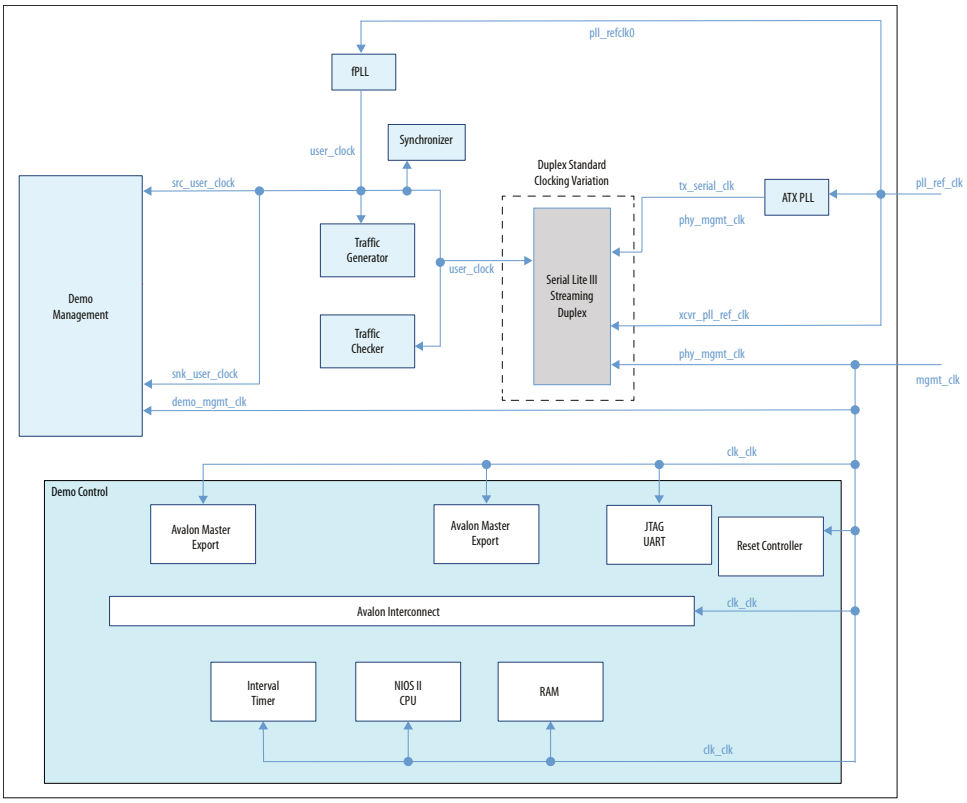


Figure 13. Clocking Scheme for Intel Stratix 10 H-tile and L-tile Serial Lite III Streaming Duplex Core in Standard Clocking Mode



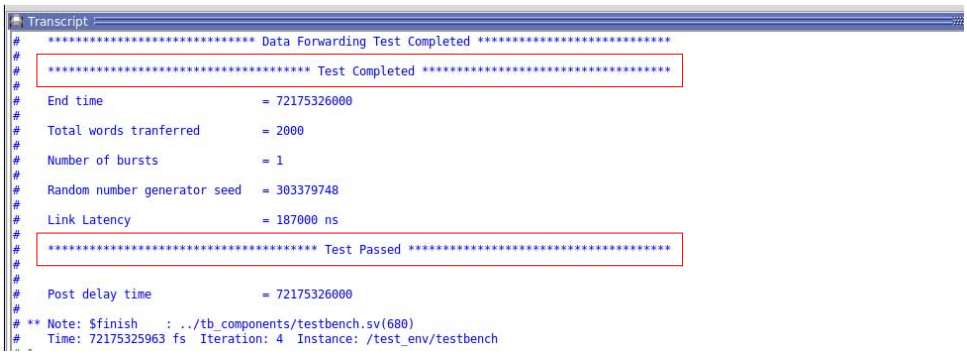
2.4. Simulation

The simulation test cases demonstrate continuous streaming of 2000 sample data from the traffic generator to the Serial Lite III Streaming source core and externally loopback to the sink core in standard clocking mode.

The simulation test case performs the following steps:

1. Initialize and configures Serial Lite III Streaming IP core, traffic generator and traffic checker.
2. Traffic generator generates data and starts data transmission.
3. Logs and display link up status and burst information.
4. Traffic checker verifies received data and stop transmission.
5. Testbench logs and displays test result and test information.

Figure 14. Sample of Successful Simulation



2.4.1. Testbench

The generated example testbench is dynamic and has the same configuration as the IP. An external transceiver ATX PLL will be generated for both duplex and simplex directions.

Note: The Intel Stratix 10 example testbench includes the external transceiver PLL; the IP core does not include the transceiver PLL for these devices.

Figure 15. Serial Lite III Streaming Example Testbench (Duplex) for Intel Stratix 10 H-tile and L-tile Standard Clocking Mode

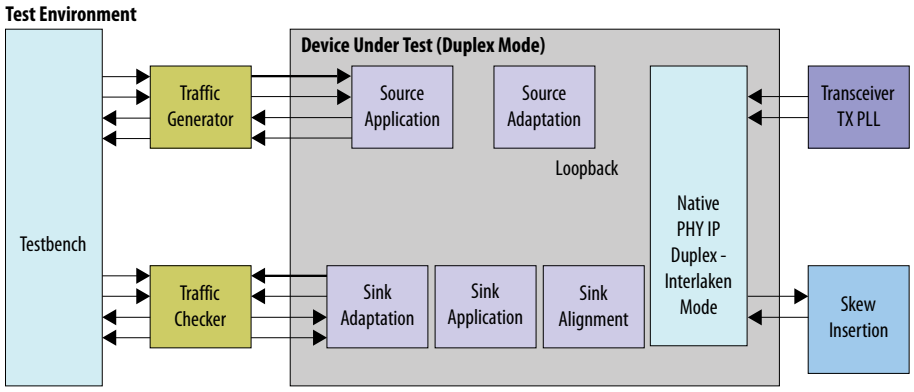


Figure 16. Serial Lite III Streaming Example Testbench (Simplex) for Intel Stratix 10 H-tile and L-tile Standard Clocking Mode

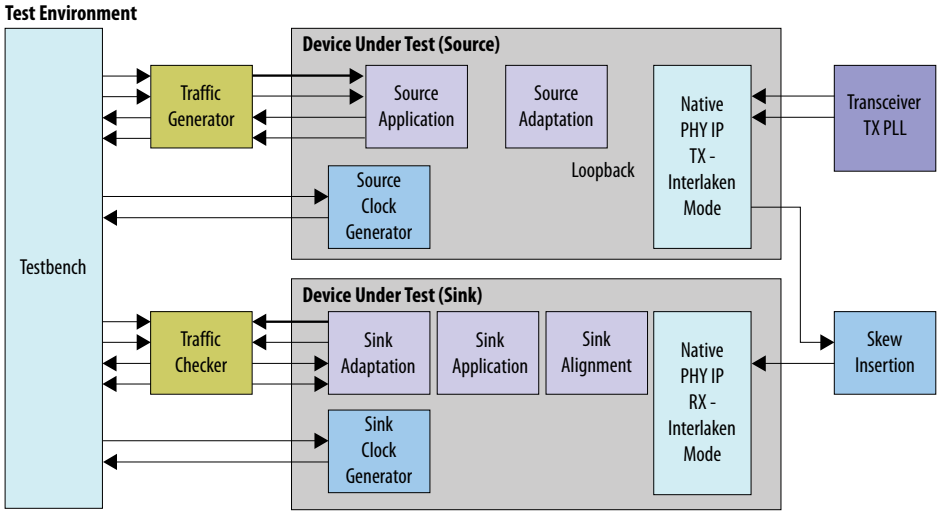
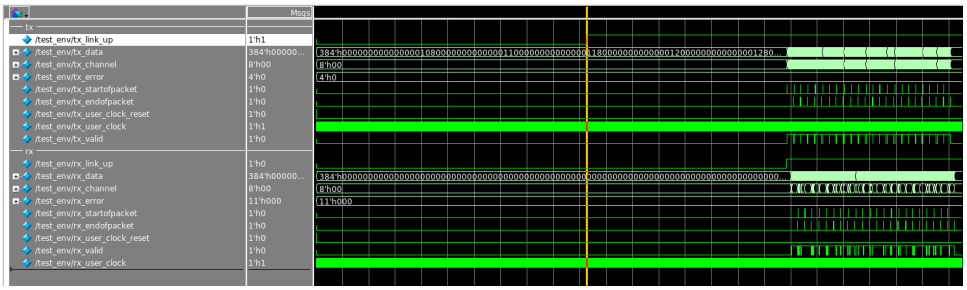


Figure 17. Simulation Waveform



2.5. Hardware Testing

After you download the design and the accompanying software into the FPGA, you can test the design through an interactive session. The interactive session provides helpful statistics, and enables you to control various aspects of the design.

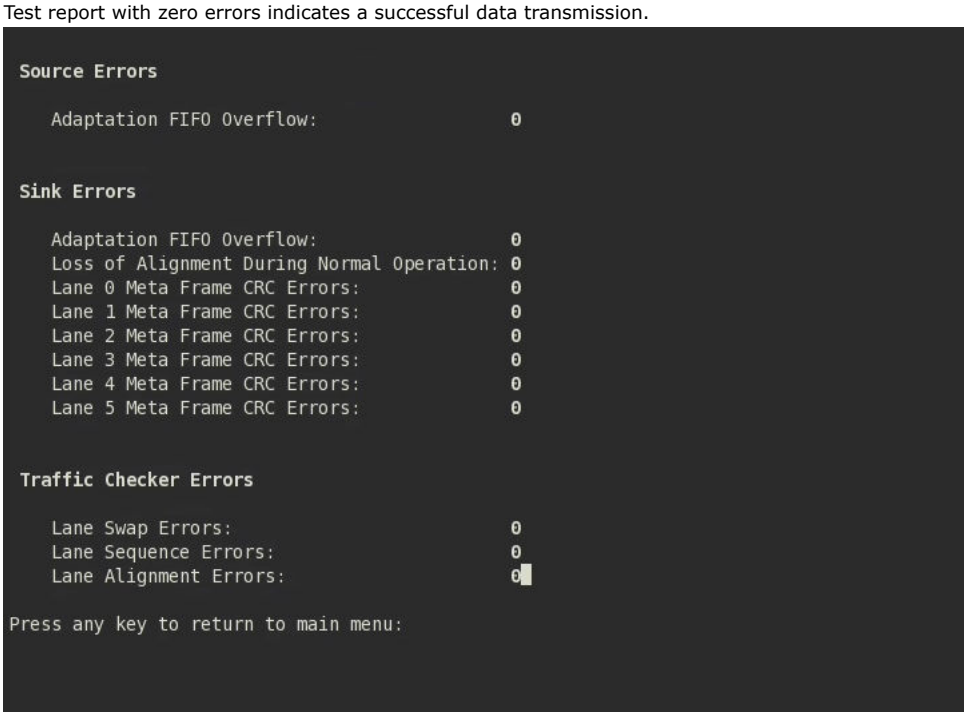
You can control the following operations by entering the option numbers listed below:

- **0) Toggle Loopback Mode** — Toggles TX to RX serial loopback path within the transceiver or external loopback mode. By default, the design example is set to external loopback mode. The loopback mode is specified in the interactive session. Disable the traffic generator/checker before switching loopback modes to avoid transmission error.
- **1) Enable Data Generator/Checker** — Enables the traffic generator and start sending out data.
- **2) Disable Data Generator/Checker** — Disables traffic generation.
- **3) Reset Source Core** — Resets the source core and traffic generator.
- **4) Reset Sink Core** — Resets the sink core and traffic checker.
- **5) Display Error Details** — Displays the error statistics.

- **6) Toggle Burst/Continuous Mode** — Resets the source and sink MACs and switches the traffic generator to generate a burst (multiple burst packet data) or continuous (single continuous data) traffic stream. By default, the design example is set to burst mode. When in continuous mode, the burst count will always show 1. Disable the data generator/checker before switching mode to avoid transmission error.
- **7) Toggle CRC Error Insertion** — Turns off or on CRC error injection (for all lanes). By default, the design example has the CRC error injection turned off.
- **8) Enable Slave Test Mode** — This option disables the traffic generator/checker and enables the traffic to flow from sink to source. This option is only available for hardware setup with master and slave configuration using two different development kits.
- **9) Disable Slave Test Mode** — This option disables data flow from sink to source. Select option 1 to enable the data generator and data checker.

Figure 18. Example of a Successful Hardware Test Report When Data Generator/ Checker is Enabled

Test report with zero errors indicates a successful data transmission.



2.5.1. Design Setup

The design example targets the Intel Stratix 10 GX Transceiver Signal Integrity Development Kit.

The design includes an SDC script as well as a QSF file with verified constraints in loopback mode. If you use the design example with another device or development board, you may need to update the device setting and constraints in the QSF file.

2.5.2. Error Details

These are the list of errors reported when you run the design example.

Table 6. Details of Errors Reported

Error	Description
Source Error:	
Adaptation FIFO Overflow	To indicate source adaptation FIFO overflow error.
Sink Errors:	
Loss of Alignment During Normal Operation	To indicate loss of alignment error (`error_rx[1]`).
Meta Frame CRC Errors	To indicate CRC errors.
Lane Swap Errors	To indicate lane swap errors in traffic checker.
Lane Sequence Errors	To indicate lane sequence error in traffic checker.
Lane Alignment Errors	To indicate lane alignment error in traffic checker.

2.6. Signals

Figure 19. Top-level Signals for Intel Stratix 10 H-tile and L-tile Serial Lite III Streaming Standard Clocking Mode Design Example

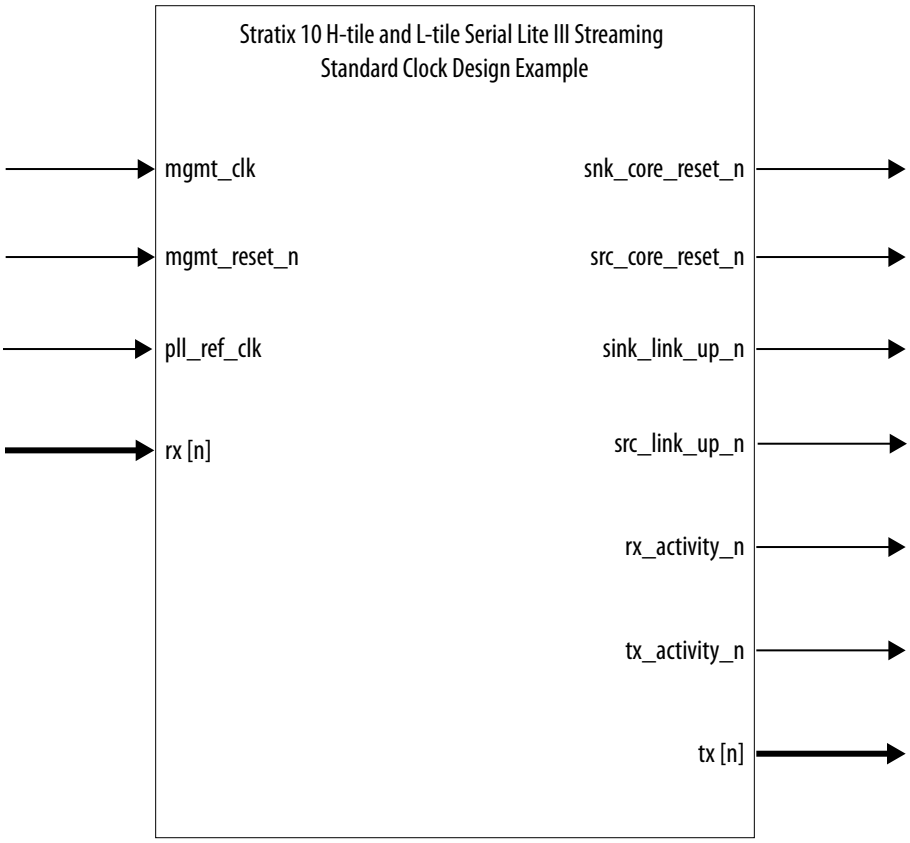


Table 7. Design Example Interface Signals

Signal	Direction	Width	Description
Clock and Reset Signal			
`mgmt_clk`	Input	1	Input clock for: • Avalon-MM PHY management interface for Serial Lite III Streaming IP core • Demo management module • Demo control module • Transceiver reset controller
`pll_ref_clk`	Input	1	This reference clock is used by the Clock Data Recovery (CDR) unit in the transceiver. It serves as a reference for the CDR to recover the clock from the serial line. The frequency of this clock must match the frequency you select in the IP parameter editor. It should also match the frequency of the tx_pll_ref_clk reference clock for the TX PLL at the Source variant.
`mgmt_reset_n`	Input	1	Design example asynchronous master reset. Assert this reset signal to reset the overall design example system. This is an active low signal.
`snk_core_reset_n`	Output	1	Demo management module asserts this signal to reset traffic checker module.
`src_core_reset_n`	Output	1	Demo management module asserts this signal to reset traffic generator module.
Data Signal			
`rx[n]`	Input	Based on **Number of Lanes** value	This vector carries the transmitted streaming data from the core. *n* represents the number of lanes.
`tx[n]`	Output	Based on **Number of Lanes** value	This vector carries the transmitted streaming data to the core. *n* represents the number of lanes.
Status Signal			
`rx_activity_n`	Output	1	This single bit signal indicates that the data is valid.
`tx_activity_n`	Output	1	This single bit signal indicates that the data is valid.
`snk_link_up_n`	Output	1	The core asserts this signal to indicate that the core initialization is complete and is ready to receive user data.
`src_link_up_n`	Output	1	The core asserts this signal to indicate that the core initialization is complete and is ready to transmit user data.

3. Detailed Description for Intel Stratix 10 H-tile and L-tile Serial Lite III Streaming Advanced Clocking Mode Design Example

This design example demonstrates the functionality of data streaming using advanced clocking mode.

To generate the design example, select any of the following presets:

- Advanced Clocking Mode 2x25.0G
- Advanced Clocking Mode 4x28.0G
- Advanced Clocking Mode 6x12.5G
- Advanced Clocking Mode 6x17.4G

Note: By default, the design examples are generated as duplex core. To generate the design examples in simplex core, select **Simplex** for the **Direction** parameter.

3.1. Features

Features for Advanced Clocking Mode design example includes:

- Support up to 16 lanes for 17.4 Gbps and 4 lanes for 28 Gbps transceiver data rate
- Support for simplex and duplex transmission modes
- Traffic checker for data verification and lane de-skew verification
- Support for CRC error injection using Nios II processor
- Slave test mode for master and slave testing

3.2. Hardware and Software Requirements

Intel uses the following hardware and software to test the example designs in a Linux system:

- Intel Quartus Prime software
- ModelSim, Riviera-PRO, Xcelium, NCSim (Verilog only), or VCS/VCS MX simulator
- Intel Stratix 10 GX Signal Integrity Development Kit (1SG280HU1F50E2VG) for hardware testing

3.3. Functional Description

The Intel Stratix 10 H-tile and L-tile design examples consist of various components. The following block diagrams show the design components and the top level connections of the design examples.

Figure 20. Design Example for Simplex Core in Advanced Clocking Mode

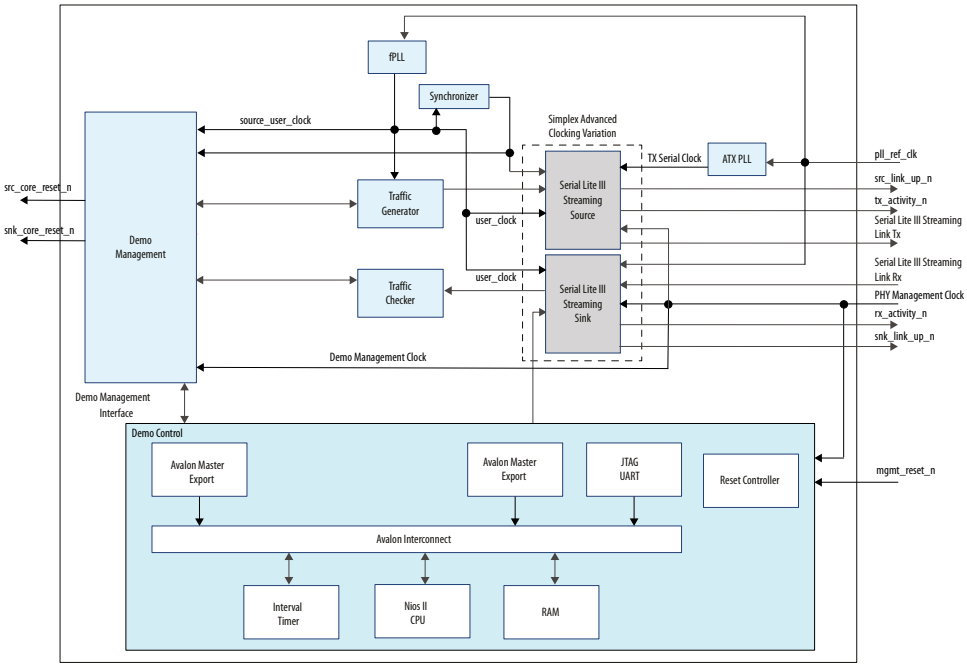
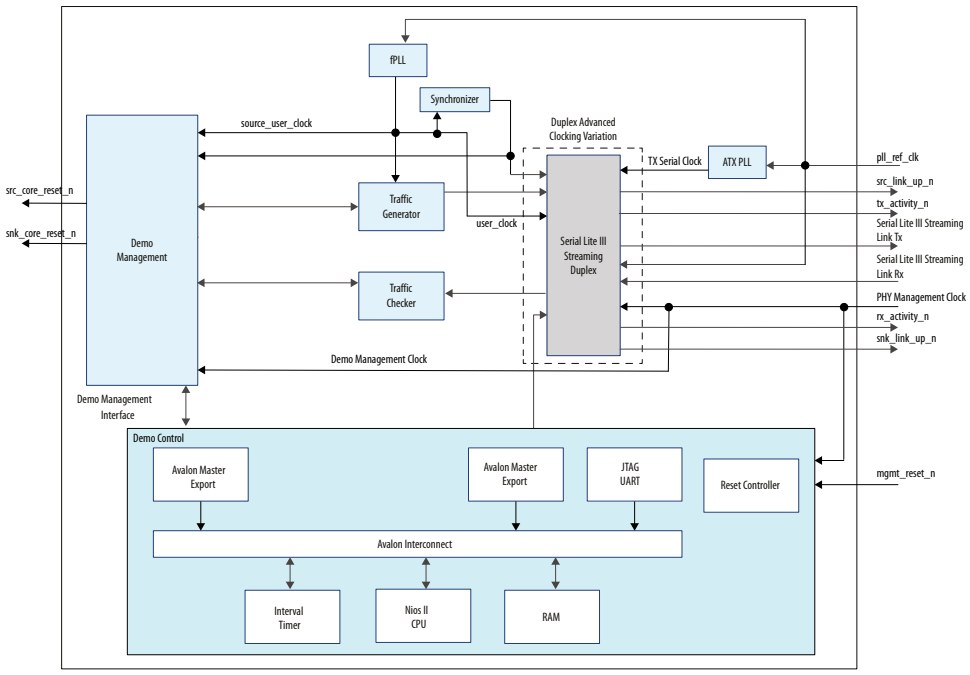


Figure 21. Design Example for Duplex Core in Advanced Clocking Mode



3.3.1. Design Example Components

The design example consists of the following components:

- Serial Lite III Streaming IP core variation
- Source and sink user clock—fPLL
- ATX PLL
- Traffic generator
- Traffic checker
- Demo control
- Demo management

3.3.1.1. Serial Lite III Streaming IP Core

The Serial Lite III Streaming IP core variation accepts data from the traffic generator and formats the data for transmission. It also receives data from the link, strips the headers, and presents it to the traffic checker for analysis. The core is generated using the parameter editor in the Intel Quartus Prime software.

3.3.1.2. User Clock

The fPLL generates a user clock for sourcing data into the Serial Lite III Streaming IP core.

3.3.1.3. Traffic Generator

The traffic generator generates traffic in a deterministic format to verify that data is transmitted correctly across the link. Traffic consists of sets of sample words, one for each lane on the link, that are presented to the source user interface.

Figure 22. Traffic Generator Sample Word Format

This figure shows the format of the sample words generated for each lane.

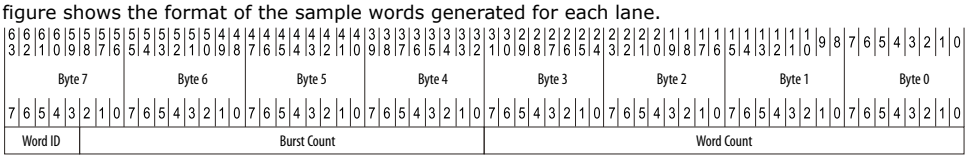


Table 8. Traffic Generator Sample Word Fields

Field	Bits	Description
Word ID	63–59	Contains a static value to distinguish which 64-bit word on the user interface that this sample was presented on. The Word ID value ranges from 0 to (lanes – 1).
Burst Count	58–32	Tracks the number of bursts used to transfer the sample data. This field value starts with one after reset and is incremented each time the `start_of_burst` signal is asserted on the source user interface.
Word Count	31–0	Tracks the number of valid sample words that have been transferred, across all bursts, to the source user interface.

3.3.1.4. Traffic Checker

The traffic checker performs the following inspections to verify that the received data conforms to the expected format:

- Checks each sample word to verify that the expected word ID was received.
- Checks each sample word to verify that the word count value is higher than the word count value from the last valid sample word.
- Verifies that lane de-skew has been properly performed by validating that the word count and burst count values from the sample word are the same as the values received from the adjacent lane.
- If the `start_of_burst` signal is asserted on the user interface, verifies that the burst count value in the current sample word is higher than the burst count value from the last valid sample word. Otherwise, it verifies that the burst count value has not changed.

3.3.1.5. Demo Control

The demo control module is a Nios II processor system, generated in Platform Designer (Standard), to control the demo hardware.

Demo control module also consists of a timer to track interrupt occurrence, Avalon-MM interface to access demo management and the Serial Lite III Streaming Intel FPGA IP PHY interface, a reset controller, a UART interface, and an Avalon Streaming (Avalon-ST) interface.

3.3.1.6. Demo Management

The demo management module controls the user modules interaction with the Serial Lite III Streaming IP core such as enable and disable traffic generator and traffic checker, enable CRC error insertion, and provide user clock reset for Serial Lite III Streaming IP core. The module also implements CSRs to control and monitor the design operation. This includes CSRs to monitor and log errors that occur during the operation.

3.3.1.7. Nios II Processor Code

The Nios II processor controls the options exercised in the design example. The code also enables the configuration RAM (CRAM) bits for CRC-32 error injection support.

The design example sets the bit for channel 0 that connects to lane 0 in the design example. Therefore, CRC error injection is exercisable for lane 0 only. Refer to the Nios II processor source code (`demo_control.c`) for information on setting bits for other channels.

The `demo_control.c` program Intel Stratix 10 H-tile and L-tile devices uses the control registers to dynamically toggle the `rx_seriallpbken` port on the Transceiver PHY block to change the TX to RX loopback from internal to external.

3.3.2. Reset Scheme

The `mgmt_reset_n` reset signal controls the overall reset structure for the design example. This is an asynchronous and active-low signal. Asserting this signal resets the demo control module and the Serial Lite III Streaming IP core. The traffic generator and traffic checker modules get reset through the demo management and the reset synchronizer.

The following diagrams show the reset scheme implemented in the design example.

Figure 23. Reset Scheme for Intel Stratix 10 H-tile and L-tile Serial Lite III Streaming Simplex Core in Advanced Clocking Mode

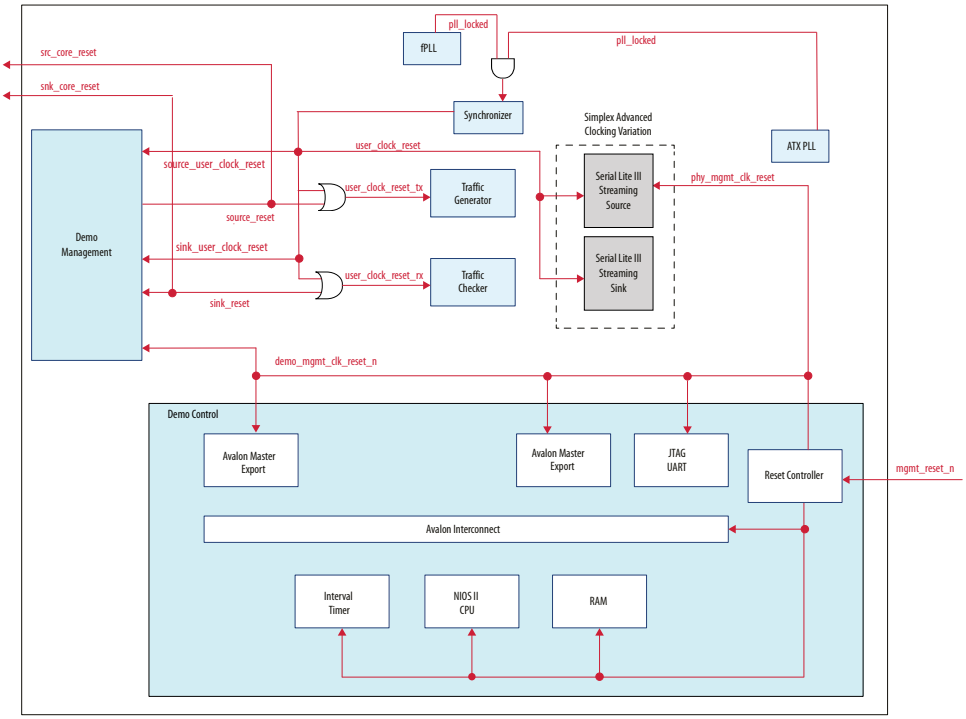
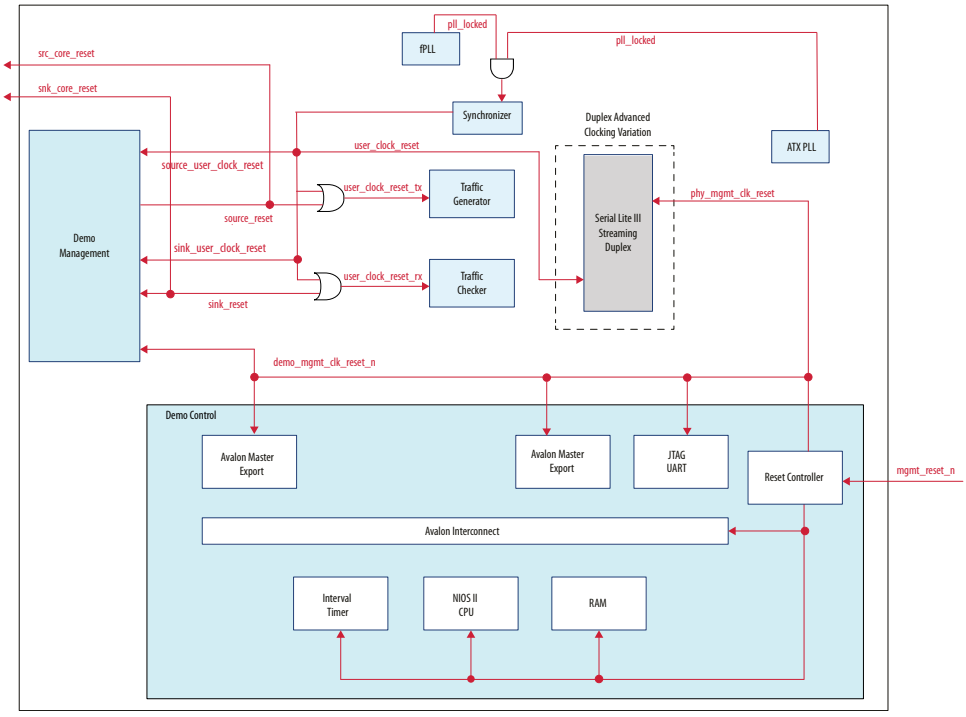


Figure 24. Reset Scheme for Intel Stratix 10 H-tile and L-tile Serial Lite III Streaming Duplex Core in Advanced Clocking Mode



3.3.3. Clocking Scheme

The following diagrams show the clocking scheme for the design example.

Figure 25. Clocking Scheme for Intel Stratix 10 H-tile and L-tile Serial Lite III Streaming Simplex Core in Advanced Clocking Mode

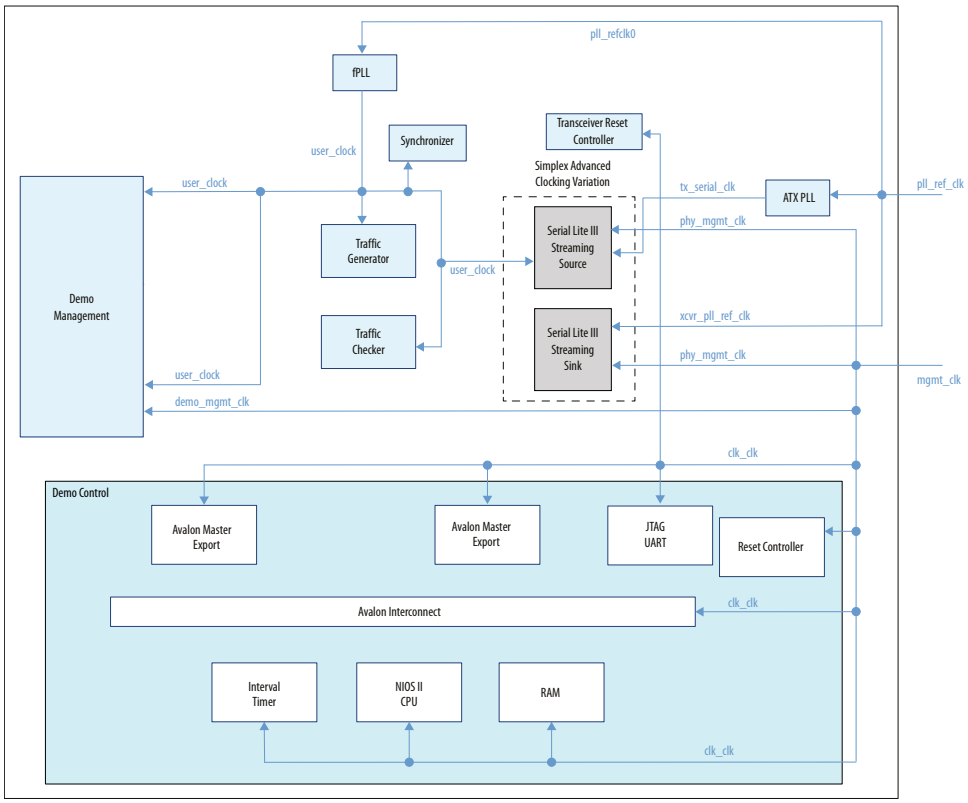
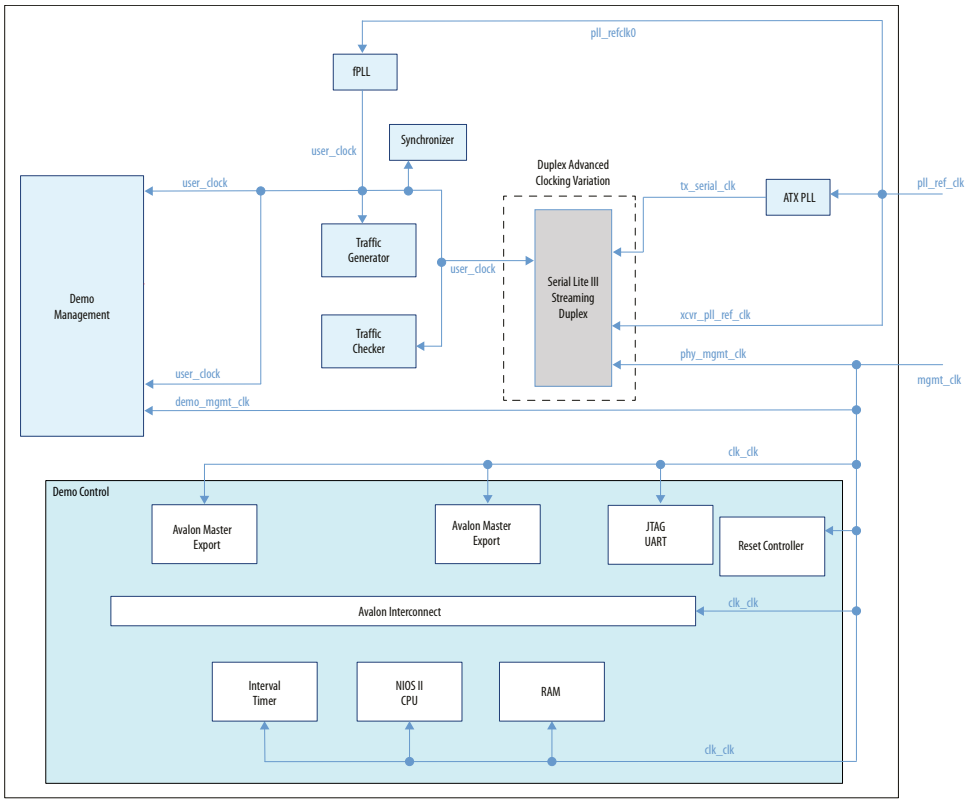


Figure 26. Clocking Scheme for Intel Stratix 10 H-tile and L-tile Serial Lite III Streaming Duplex Core in Advanced Clocking Mode



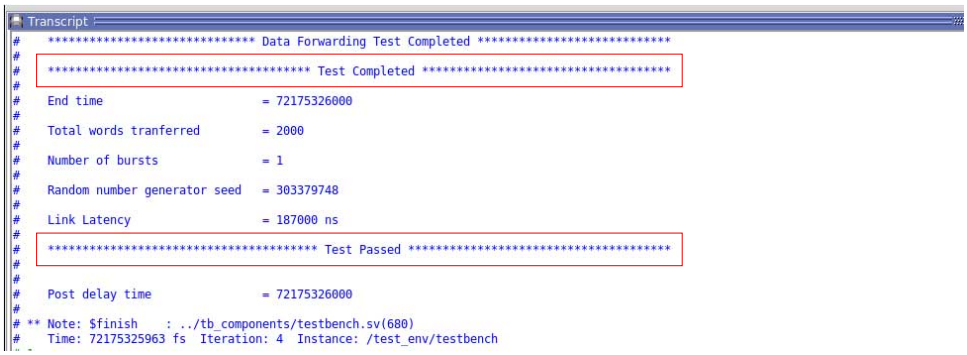
3.4. Simulation

The simulation test cases demonstrate continuous streaming of 2000 sample data from the traffic generator to the Serial Lite III Streaming source core and externally loopback to the sink core in advanced clocking mode.

The simulation test case performs the following steps:

1. Initialize and configures Serial Lite III Streaming IP core, traffic generator and traffic checker.
2. Traffic generator generates data and starts data transmission.
3. Logs and display link up status and burst information.
4. Traffic checker verifies received data and stop transmission.
5. Testbench logs and displays test result and test information.

Figure 27. Sample of Successful Simulation



3.4.1. Testbench

The generated example testbench is dynamic and has the same configuration as the IP. An external transceiver ATX PLL will be generated for both duplex and simplex directions.

Note: The Intel Stratix 10 example testbench includes the external transceiver PLL; the IP core does not include the transceiver PLL for these devices.

Figure 28. Serial Lite III Streaming Example Testbench (Duplex) for Intel Stratix 10 H-tile and L-tile Advanced Clocking Mode

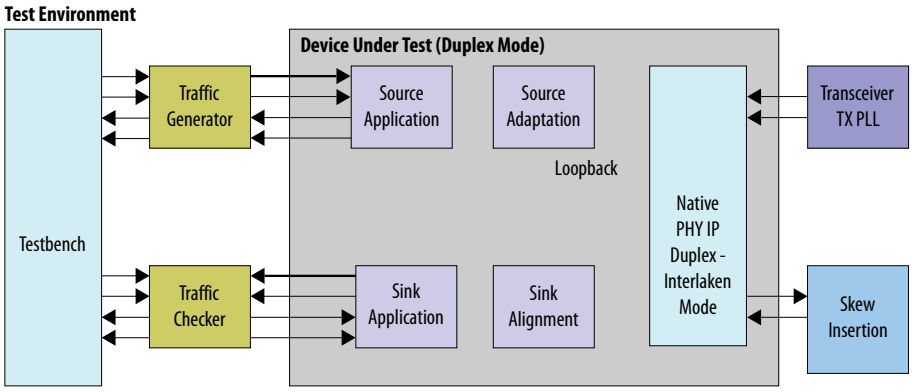
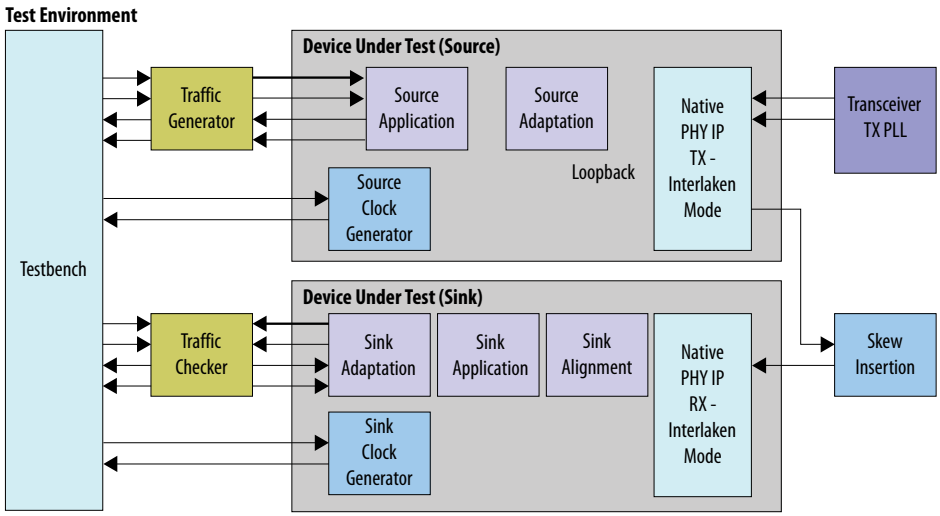


Figure 29. Serial Lite III Streaming Example Testbench (Simplex) for Intel Stratix 10 H-tile and L-tile Advanced Clocking Mode



3.5. Hardware Testing

After you download the design and the accompanying software into the FPGA, you can test the design through an interactive session. The interactive session provides helpful statistics, and enables you to control various aspects of the design.

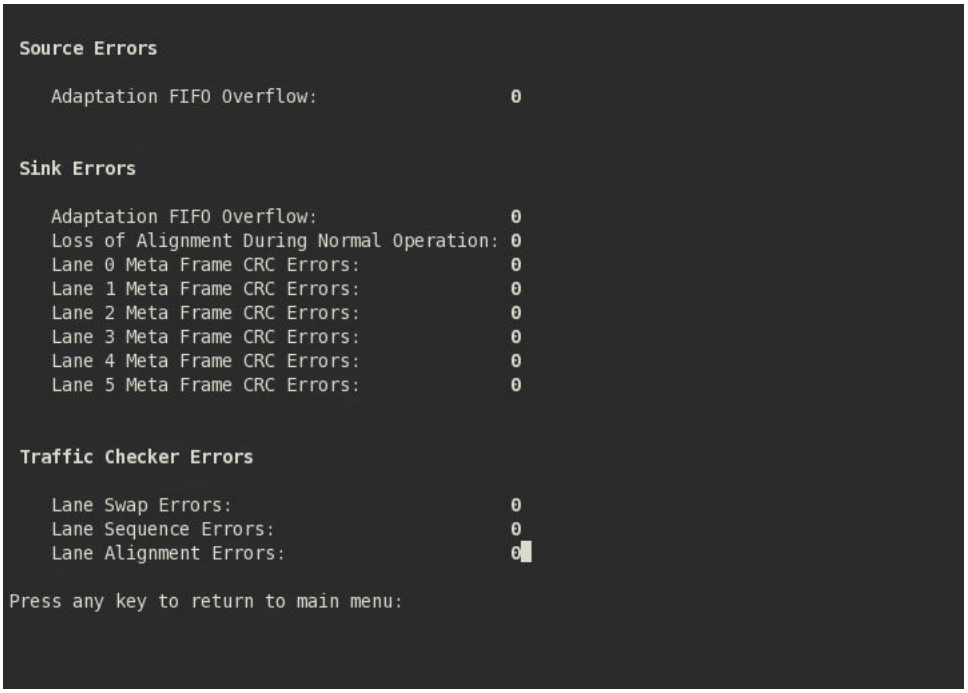
You can control the following operations by entering the numbers listed below:

- **0) Toggle Loopback Mode** - Toggles TX to RX serial loopback path within the transceiver or external loopback mode. The loopback mode is specified in the interactive session. Disable the traffic generator/checker before switching loopback modes to avoid transmission error.
- **1) Enable Data Generator/Checker** - Enables the traffic generator and start sending out data.
- **2) Disable Data Generator/Checker** - Disables traffic generation.
- **3) Reset Source Core** - Resets the source core and traffic generator.
- **4) Reset Sink Core** - Resets the sink core and traffic checker.
- **5) Display Error Details** - Displays the error statistics.
- **6) Toggle Burst/Continuous Mode** - Resets the source and sink MACs and switches the traffic generator to generate a burst (multiple burst packet data) or continuous (single continuous data) traffic stream. By default, the design example is set to burst mode. When in continuous mode, the burst count will always show 1. Disable the data generator/checker before switching mode to avoid transmission error.
- **7) Toggle CRC Error Insertion** - Turns CRC error injection off or on (for all lanes). By default, the design example has CRC error injection turned off.

Note: Options 8 and 9 applicable only in standard clocking mode.

Figure 30. Example of a Successful Hardware Test When Data Generator/Checker is Enabled

Test report with zero errors indicates a successful data transmission.



3.5.1. Design Setup

The design example targets the Intel Stratix 10 GX Transceiver Signal Integrity Development Kit.

The design includes an SDC script as well as a QSF file with verified constraints in loopback mode. If you use the design example with another device or development board, you may need to update the device setting and constraints in the QSF file.

3.5.2. Error Details

These are the list of errors reported when you run the design example.

Table 9. Details of Errors Reported

Error	Description
Source Error:	
Adaptation FIFO Overflow	To indicate source adaptation FIFO overflow error.
Sink Errors:	
Loss of Alignment During Normal Operation	To indicate loss of alignment error (`error_rx[1]`).
Meta Frame CRC Errors	To indicate CRC errors.

continued...

Error	Description
Lane Swap Errors	To indicate lane swap errors in traffic checker.
Lane Sequence Errors	To indicate lane sequence error in traffic checker.
Lane Alignment Errors	To indicate lane alignment error in traffic checker.

3.6. Signals

Figure 31. Top-level Signals for Intel Stratix 10 H-tile and L-tile Serial Lite III Streaming Advanced Clocking Mode Design Example

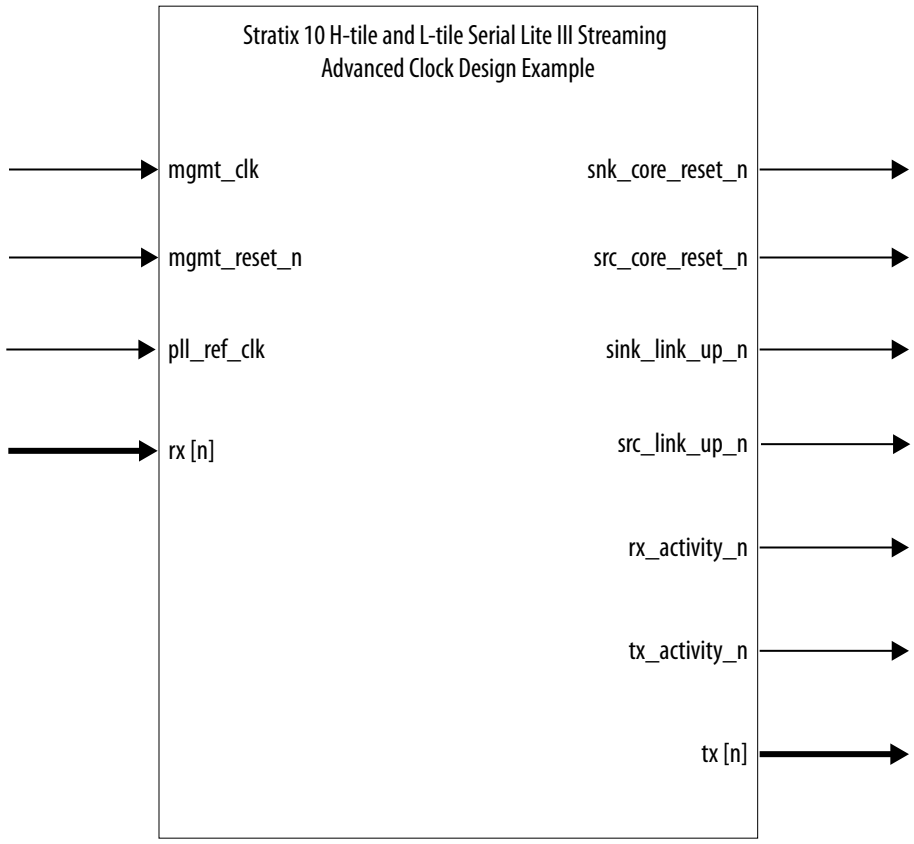


Table 10. Design Example Interface Signals

Signal	Direction	Width	Description
Clock and Reset Signal			
mgmt_clk	Input	1	Input clock for: • Avalon-MM PHY management interface for Serial Lite III Streaming IP core • Demo management module • Demo control module • Transceiver reset controller

continued...

Signal	Direction	Width	Description
pll_ref_clk	Input	1	This reference clock is used by the Clock Data Recovery (CDR) unit in the transceiver. It serves as a reference for the CDR to recover the clock from the serial line. The frequency of this clock must match the frequency you select in the IP parameter editor. It should also match the frequency of the tx_pll_ref_clk reference clock for the TX PLL at the Source variant.
mgmt_reset_n	Input	1	Design example asynchronous master reset. Assert this reset signal to reset the overall design example system. This is an active low signal.
snk_core_reset_n	Output	1	Demo management module asserts this signal to reset traffic checker module.
src_core_reset_n	Output	1	Demo management module asserts this signal to reset traffic generator module.
Data Signal			
rx[n]	Input	Based on **Number of Lanes** value	This vector carries the transmitted streaming data from the core. *n* represents the number of lanes.
tx[n]	Output	Based on **Number of Lanes** value	This vector carries the transmitted streaming data to the core. *n* represents the number of lanes.
Status Signal			
rx_activity_n	Output	1	This single bit signal indicates that the data is valid.
tx_activity_n	Output	1	This single bit signal indicates that the data is valid.
snk_link_up_n	Output	1	The core asserts this signal to indicate that the core initialization is complete and is ready to receive user data.
src_link_up_n	Output	1	The core asserts this signal to indicate that the core initialization is complete and is ready to transmit user data.

4. Detailed Description for Intel Stratix 10 E-tile Serial Lite III Streaming Standard Clocking Mode Design Example

This design example demonstrates the functionality of data streaming using standard clocking mode.

To generate the design example, select any of the following presets:

- Standard Clocking Mode 2x25.0G
- Standard Clocking Mode 4x28.0G
- Standard Clocking Mode 6x12.5G
- Standard Clocking Mode 6x17.4G

The design examples are available only in duplex mode.

Note: To target the Intel Stratix 10 E-tile device with the Intel Stratix 10 TX Signal Integrity development kit, make sure to select **E-Tile** for the **Transceiver Tile** parameter in the **IP** tab.

4.1. Features

Features for Standard Clocking Mode design example includes:

- Support for up to 12 lanes for 17.4 Gbps and 4 lanes for 28 Gbps transceiver data rate
- Support for duplex transmission mode
- Traffic checker for data verification and lane de-skew verification
- Support for CRC error injection using Nios II processor
- Slave test mode for master and slave testing

4.2. Hardware and Software Requirements

Intel uses the following hardware and software to test the example designs in a Linux system:

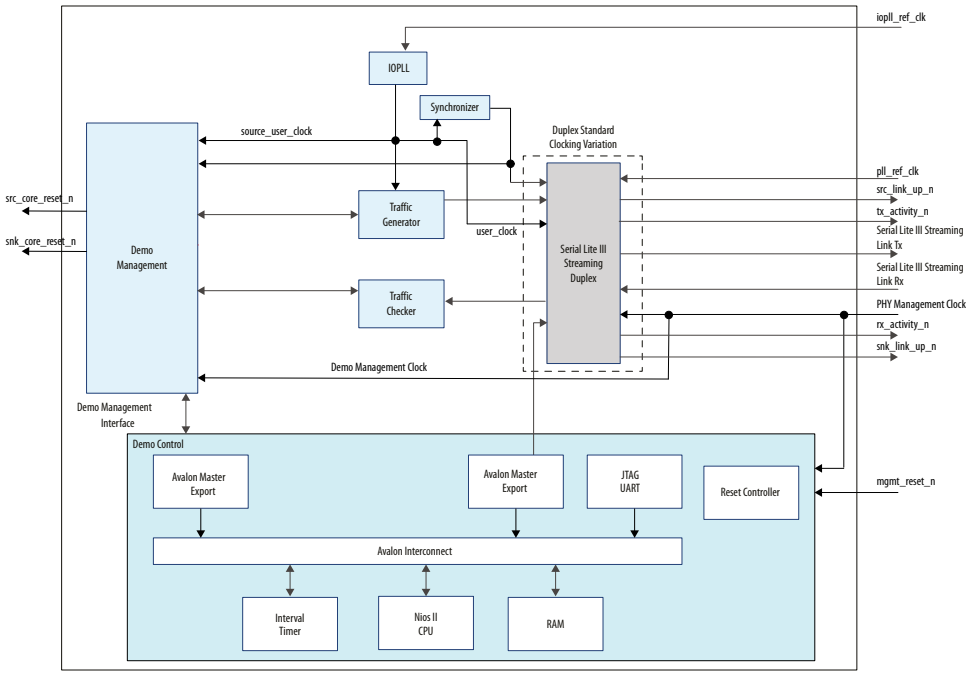
- Intel Quartus Prime software
- ModelSim, Xcelium, NCSim (Verilog only), or VCS/VCS MX simulator
- Intel Stratix 10 TX Signal Integrity Development Kit (1ST280EY1F55E1VGS1) for hardware testing

Note: To target the Intel Stratix 10 E-tile device with the Intel Stratix 10 TX Signal Integrity development kit, make sure to select **E-Tile** for the **Transceiver Tile** parameter in the **IP** tab.

4.3. Functional Description

The Intel Stratix 10 E-tile design examples consist of various components. The following block diagram shows the design components and the top level connections of the design examples.

Figure 32. Design Example for Duplex Core in Standard Clocking Mode



4.3.1. Design Example Components

The design example consists of the following components:

- Serial Lite III Streaming IP core variation
- Source user clock—IOPLL
- Traffic generator
- Traffic checker
- Demo control
- Demo management

4.3.1.1. Serial Lite III Streaming IP Core

The Serial Lite III Streaming IP core variation accepts data from the traffic generator and formats the data for transmission. It also receives data from the link, strips the headers, and presents it to the traffic checker for analysis. The core is generated using the parameter editor in the Intel Quartus Prime software.

4.3.1.2. User Clock

The IOPLL generates a user clock for sourcing and sinking data into the Serial Lite III Streaming IP core.

4.3.1.3. Traffic Generator

The traffic generator generates traffic in a deterministic format to verify that data is transmitted correctly across the link. Traffic consists of sets of sample words, one for each lane on the link, that are presented to the source user interface.

Figure 33. Traffic Generator Sample Word Format

This figure shows the format of the sample words generated for each lane.

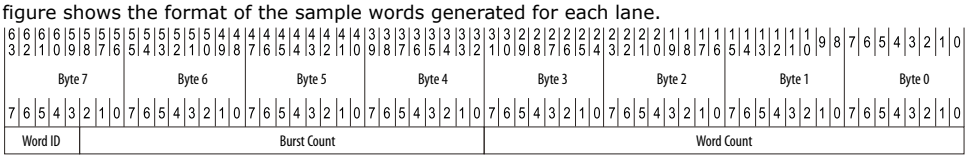


Table 11. Traffic Generator Sample Word Fields

Field	Bits	Description
Word ID	63–59	Contains a static value to distinguish which 64-bit word on the user interface that this sample was presented on. The Word ID value ranges from 0 to (lanes – 1).
Burst Count	58–32	Tracks the number of bursts used to transfer the sample data. This field value starts with one after reset and is incremented each time the `start_of_burst` signal is asserted on the source user interface.
Word Count	31–0	Tracks the number of valid sample words that have been transferred, across all bursts, to the source user interface.

4.3.1.4. Traffic Checker

The traffic checker performs the following inspections to verify that the received data conforms to the expected format:

- Checks each sample word to verify that the expected word ID was received.
- Checks each sample word to verify that the word count value is higher than the word count value from the last valid sample word.
- Verifies that lane de-skew has been properly performed by validating that the word count and burst count values from the sample word are the same as the values received from the adjacent lane.
- If the `start_of_burst` signal is asserted on the user interface, verifies that the burst count value in the current sample word is higher than the burst count value from the last valid sample word. Otherwise, it verifies that the burst count value has not changed.

4.3.1.5. Demo Control

The demo control module is a Nios II processor system, generated in Platform Designer (Standard), to control the demo hardware.

Demo control module also consists of a timer to track interrupt occurrence, Avalon-MM interface to access demo management and the Serial Lite III Streaming Intel FPGA IP PHY interface, a reset controller, a UART interface, and an Avalon Streaming (Avalon-ST) interface.

4.3.1.6. Demo Management

The demo management module controls the user modules interaction with the Serial Lite III Streaming IP core such as enable and disable traffic generator and traffic checker, enable CRC error insertion, and provide user clock reset for Serial Lite III Streaming IP core. The module also implements CSRs to control and monitor the design operation. This includes CSRs to monitor and log errors that occur during the operation.

4.3.1.7. Nios II Processor Code

The Nios II processor controls the options exercised in the design example. The code also enables CRAM bits for CRC-32 error injection support.

The design example sets the bit for channel 0 that connects to lane 0 in the design example. Therefore, CRC error injection is exercisable for lane 0 only. Refer to the Nios II processor source code (`demo_control.c`) for information on setting bits for other channels.

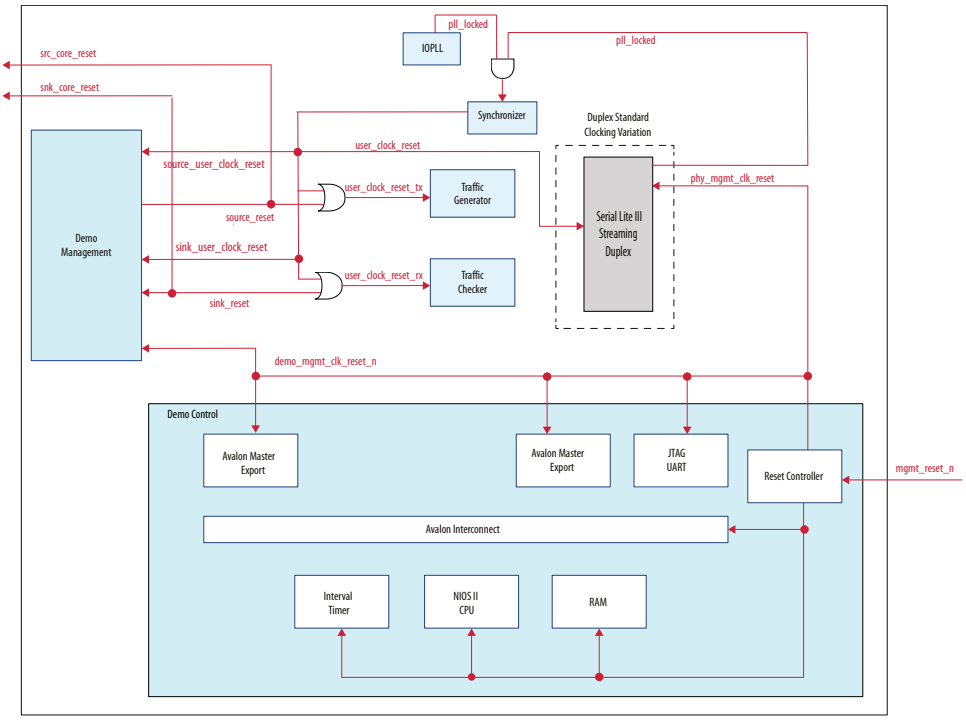
The `demo_control.c` program for Intel Stratix 10 E-tile devices uses the Transceiver PHY dynamic reconfiguration block to control registers to dynamically toggle the Transceiver PHY block `seriallpback` to change the TX to RX loopback from internal to external. The `demo_control` program also uses the Transceiver PHY dynamic reconfiguration to enable initial coarse adaptive equalization to reduce bit error during high data rate transmission.

4.3.2. Reset Scheme

The `mgmt_reset_n` reset signal controls the overall reset structure for the design example. This is an asynchronous and active-low signal. Asserting this signal resets the demo control module and the Serial Lite III Streaming IP core. The traffic generator and traffic checker modules get reset through the demo management and the reset synchronizer.

The following diagram shows the reset scheme implemented in the design example.

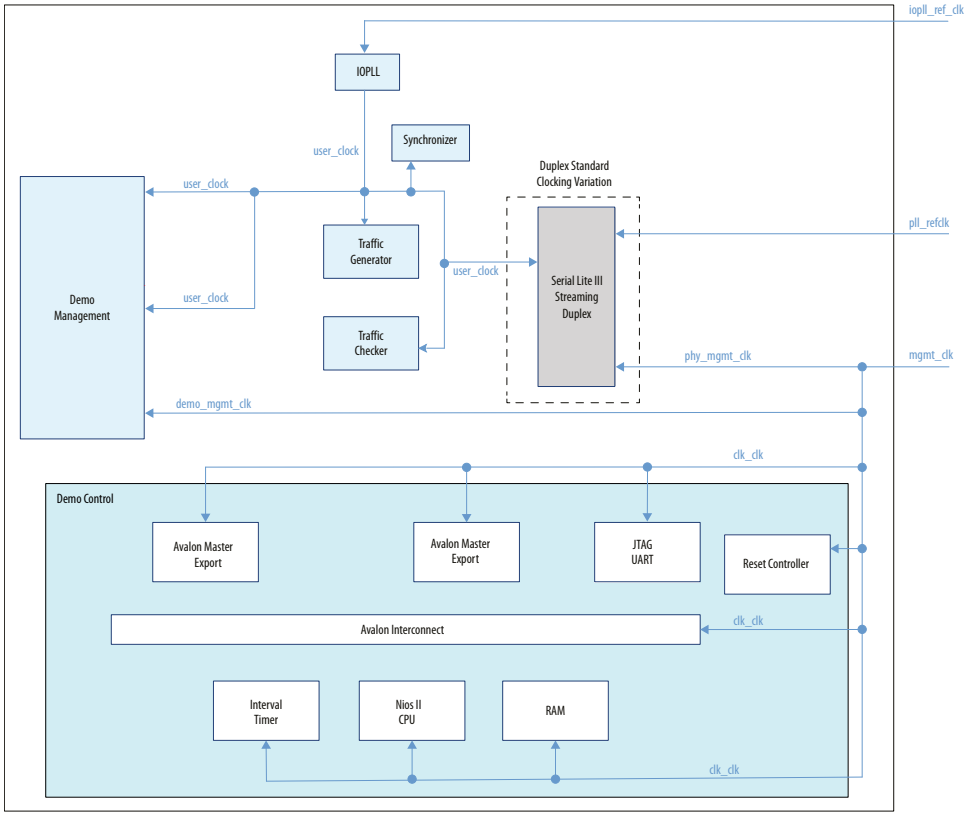
Figure 34. Reset Scheme for Intel Stratix 10 E-tile Serial Lite III Streaming Duplex Core in Standard Clocking Mode



4.3.3. Clocking Scheme

The following diagram shows the clocking scheme for the design example.

Figure 35. Clocking Scheme for Intel Stratix 10 E-tile Serial Lite III Streaming Duplex Core in Standard Clocking Mode



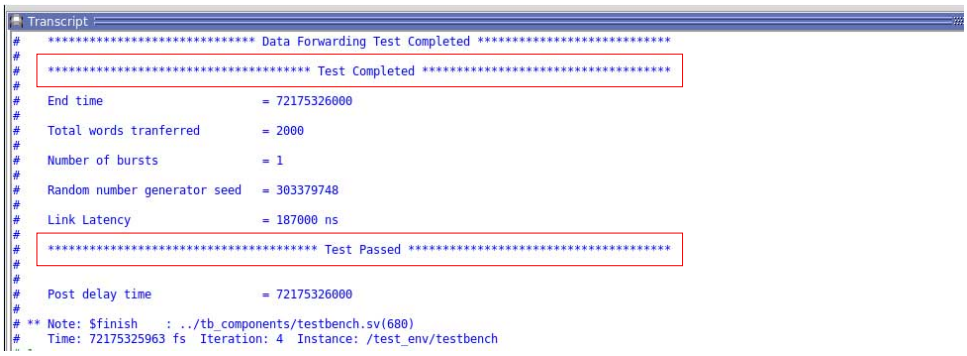
4.4. Simulation

The simulation test cases demonstrate continuous streaming of 2000 sample data from the traffic generator to the Serial Lite III Streaming source core and externally loopback to the sink core in standard clocking mode.

The simulation test case performs the following steps:

1. Initialize and configures Serial Lite III Streaming IP core, traffic generator and traffic checker.
2. Traffic generator generates data and starts data transmission.
3. Logs and display link up status and burst information.
4. Traffic checker verifies received data and stop transmission.
5. Testbench logs and displays test result and test information.

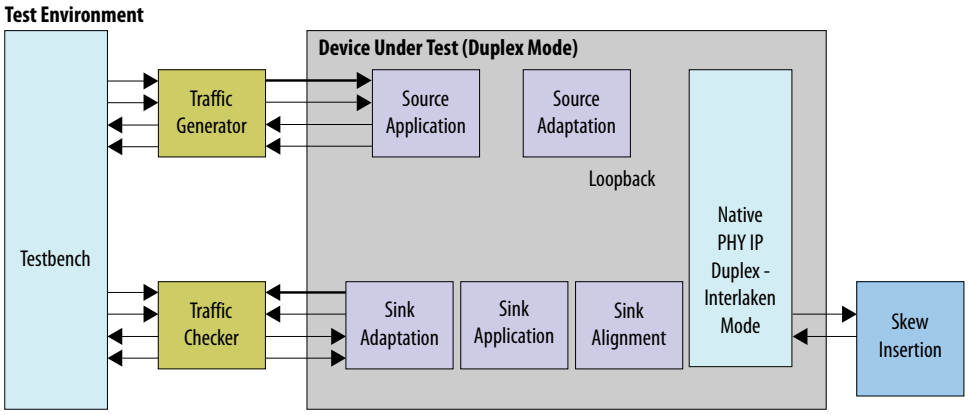
Figure 36. Sample of Successful Simulation



4.4.1. Testbench

The generated example testbench is dynamic and has the same configuration as the IP.

Figure 37. Serial Lite III Streaming Example Testbench (Duplex) for Intel Stratix 10 E-tile Standard Clocking Mode



4.5. Hardware Testing

After you download the design and the accompanying software into the FPGA, you can test the design through an interactive session. The interactive session provides helpful statistics, and enables you to control various aspects of the design.

You can control the following operations by entering the option numbers listed below:

- **0) Toggle Loopback Mode** — Toggles TX to RX serial loopback path within the transceiver or external loopback mode. By default, the design example is set to external loopback mode. The loopback mode is specified in the interactive session. Disable the traffic generator/checker before switching loopback modes to avoid transmission error.
- **1) Enable Data Generator/Checker** — Enables the traffic generator and start sending out data.
- **2) Disable Data Generator/Checker** — Disables traffic generation.

- **3) Reset Source Core** — Resets the source core and traffic generator.
- **4) Reset Sink Core** — Resets the sink core and traffic checker.
- **5) Display Error Details** — Displays the error statistics.
- **6) Toggle Burst/Continuous Mode** — Resets the source and sink MACs and switches the traffic generator to generate a burst (multiple burst packet data) or continuous (single continuous data) traffic stream. By default, the design example is set to burst mode. When in continuous mode, the burst count will always show 1. Disable the data generator/checker before switching mode to avoid transmission error.
- **7) Toggle CRC Error Insertion** — Turns off or on CRC error injection (for all lanes). By default, the design example has the CRC error injection turned off.
- **8) Enable Slave Test Mode** — This option disables the traffic generator/checker and enables the traffic to flow from sink to source. This option is only available for hardware setup with master and slave configuration using two different development kits.
- **9) Disable Slave Test Mode** — This option disables data flow from sink to source. Select option 1 to enable the data generator and data checker.

Figure 38. Example of a Successful Hardware Test Report When Data Generator/ Checker is Enabled

Test report with zero errors indicates a successful data transmission.

```
Source Errors

   Adaptation FIFO Overflow:                0


Sink Errors

   Adaptation FIFO Overflow:                0
   Loss of Alignment During Normal Operation: 0
   Lane 0 Meta Frame CRC Errors:            0
   Lane 1 Meta Frame CRC Errors:            0
   Lane 2 Meta Frame CRC Errors:            0
   Lane 3 Meta Frame CRC Errors:            0
   Lane 4 Meta Frame CRC Errors:            0
   Lane 5 Meta Frame CRC Errors:            0


Traffic Checker Errors

   Lane Swap Errors:                        0
   Lane Sequence Errors:                    0
   Lane Alignment Errors:                   0

Press any key to return to main menu:
```

4.5.1. Design Setup

The design example targets the Intel Stratix 10 TX Transceiver Signal Integrity Development Kit.

The design includes an SDC script as well as a QSF file with verified constraints in loopback mode. If you use the design example with another device or development board, you may need to update the device setting and constraints in the QSF file.

4.5.2. Error Details

These are the list of errors reported when you run the design example.

Table 12. Details of Errors Reported

Error	Description
Source Error:	
Adaptation FIFO Overflow	To indicate source adaptation FIFO overflow error.
Sink Errors:	
Loss of Alignment During Normal Operation	To indicate loss of alignment error (`error_rx[1]`).
Meta Frame CRC Errors	To indicate CRC errors.
Lane Swap Errors	To indicate lane swap errors in traffic checker.
Lane Sequence Errors	To indicate lane sequence error in traffic checker.
Lane Alignment Errors	To indicate lane alignment error in traffic checker.

4.6. Signals

Figure 39. Top-level Signals for Intel Stratix 10 E-tile Serial Lite III Streaming Standard Clocking Mode Design Example

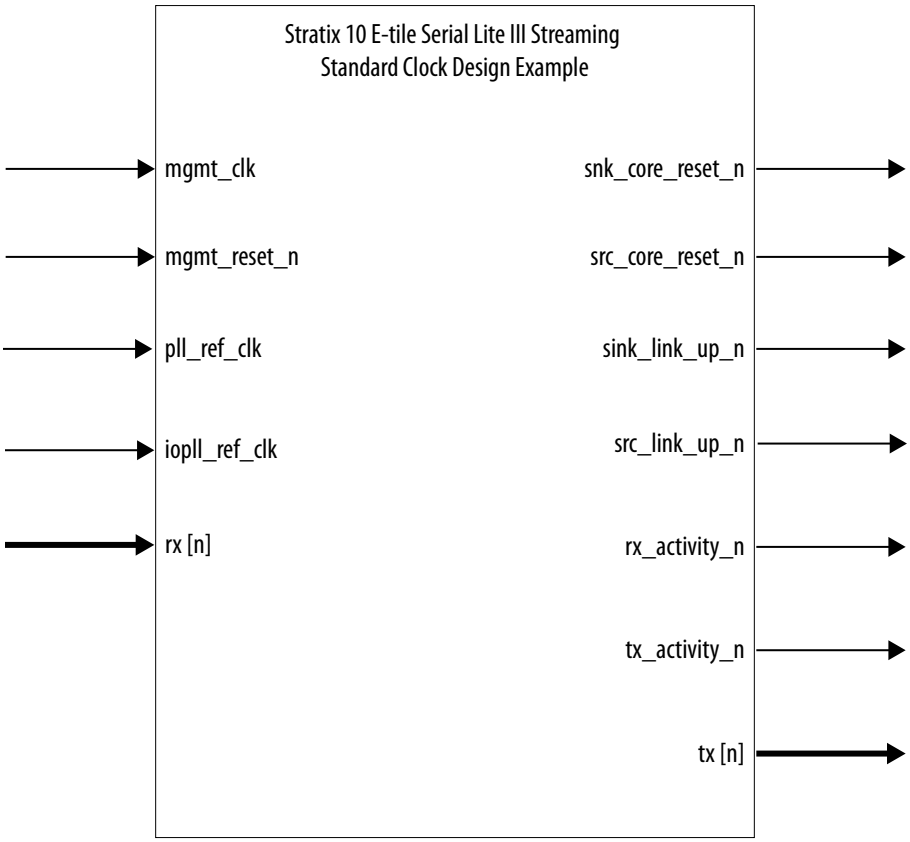


Table 13. Design Example Interface Signals

Signal	Direction	Width	Description
Clock and Reset Signal			
`mgmt_clk`	Input	1	Input clock for: • Avalon-MM PHY management interface for Serial Lite III Streaming IP core • Demo management module • Demo control module • Transceiver reset controller
`pll_ref_clk`	Input	1	This reference clock is used by the Clock Data Recovery (CDR) unit in the transceiver. It serves as a reference for the CDR to recover the clock from the serial line. The frequency of this clock must match the frequency you select in the IP parameter editor.
`iopll_ref_clk`	Input	1	This clock is used as a reference clock for the IOPLL user clock.

continued...

Signal	Direction	Width	Description
mgmt_reset_n	Input	1	Design example asynchronous master reset. Assert this reset signal to reset the overall design example system. This is an active low signal.
snk_core_reset_n	Output	1	Demo management module asserts this signal to reset traffic checker module.
src_core_reset_n	Output	1	Demo management module asserts this signal to reset traffic generator module.
Data Signal			
rx[n]	Input	Based on **Number of Lanes** value	This vector carries the transmitted streaming data from the core. *n* represents the number of lanes.
tx[n]	Output	Based on **Number of Lanes** value	This vector carries the transmitted streaming data to the core. *n* represents the number of lanes.
Status Signal			
rx_activity_n	Output	1	This single bit signal indicates that the data is valid.
tx_activity_n	Output	1	This single bit signal indicates that the data is valid.
snk_link_up_n	Output	1	The core asserts this signal to indicate that the core initialization is complete and is ready to receive user data.
src_link_up_n	Output	1	The core asserts this signal to indicate that the core initialization is complete and is ready to transmit user data.

5. Detailed Description for Intel Stratix 10 E-tile Serial Lite III Streaming Advanced Clocking Mode Design Example

This design example demonstrates the functionality of data streaming using advanced clocking mode.

To generate the design example, select any of the following presets:

- Advanced Clocking Mode 4x28.0G
- Advanced Clocking Mode 2x25.0G
- Advanced Clocking Mode 6x12.5G
- Advanced Clocking Mode 6x17.4G

The design examples are available only in duplex mode.

Note: To target the Intel Stratix 10 E-tile device with the Intel Stratix 10 TX Signal Integrity development kit, make sure to select **E-Tile** for the **Transceiver Tile** parameter in the **IP** tab.

5.1. Features

Features for Advanced Clocking Mode design example includes:

- Support up to 16 lanes for 17.4 Gbps and 4 lanes for 28 Gbps transceiver data rate
- Support for duplex transmission modes
- Traffic checker for data verification and lane de-skew verification
- Support for CRC error injection using Nios II processor
- Slave test mode for master and slave testing

5.2. Hardware and Software Requirements

Intel uses the following hardware and software to test the example designs in a Linux system:

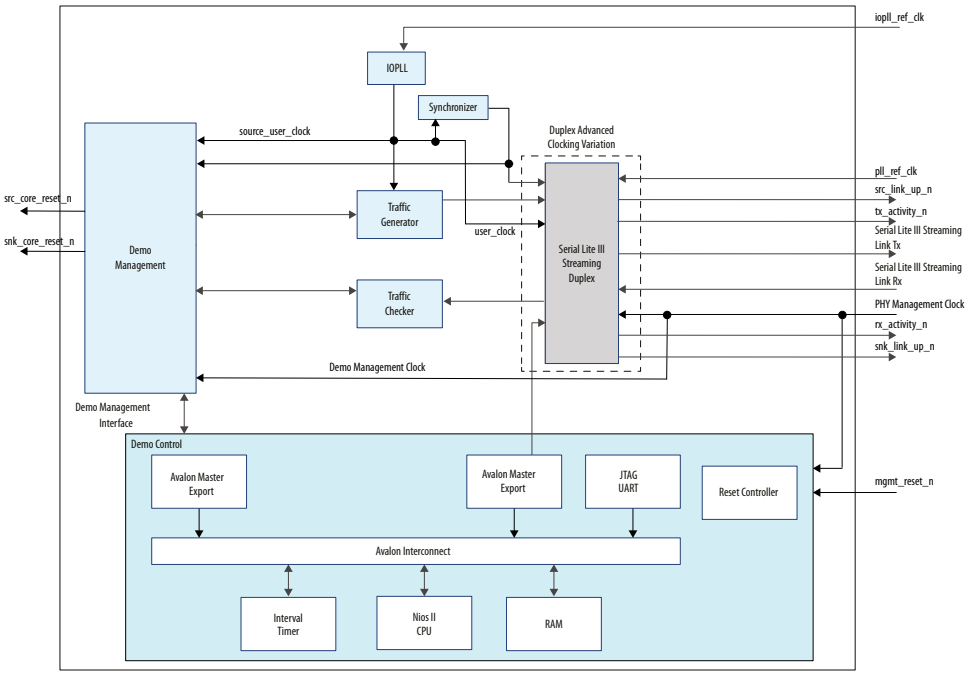
- Intel Quartus Prime software
- ModelSim, Xcelium, NCSim (Verilog only), or VCS/VCS MX simulator
- Intel Stratix 10 TX Signal Integrity Development Kit (1ST280EY1F55E1VGS1) for hardware testing

Note: To target the Intel Stratix 10 E-tile device with the Intel Stratix 10 TX Signal Integrity development kit, make sure to select **E-Tile** for the **Transceiver Tile** parameter in the **IP** tab.

5.3. Functional Description

The Intel Stratix 10 E-tile design examples consist of various components. The following block diagram shows the design components and the top level connections of the design examples.

Figure 40. Design Example for Duplex Core in Advanced Clocking Mode



5.3.1. Design Example Components

The design example consists of the following components:

- Serial Lite III Streaming IP core variation
- Source user clock—IOPLL
- Traffic generator
- Traffic checker
- Demo control
- Demo management

5.3.1.1. Serial Lite III Streaming IP Core

The Serial Lite III Streaming IP core variation accepts data from the traffic generator and formats the data for transmission. It also receives data from the link, strips the headers, and presents it to the traffic checker for analysis. The core is generated using the parameter editor in the Intel Quartus Prime software.

5.3.1.2. User Clock

The IOPLL generates a user clock for sourcing and sinking data into the Serial Lite III Streaming IP core.

5.3.1.3. Traffic Generator

The traffic generator generates traffic in a deterministic format to verify that data is transmitted correctly across the link. Traffic consists of sets of sample words, one for each lane on the link, that are presented to the source user interface.

Figure 41. Traffic Generator Sample Word Format

This figure shows the format of the sample words generated for each lane.

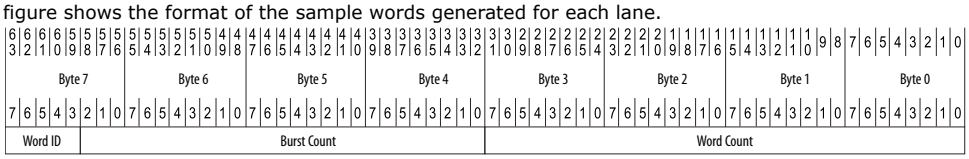


Table 14. Traffic Generator Sample Word Fields

Field	Bits	Description
Word ID	63–59	Contains a static value to distinguish which 64-bit word on the user interface that this sample was presented on. The Word ID value ranges from 0 to (lanes – 1).
Burst Count	58–32	Tracks the number of bursts used to transfer the sample data. This field value starts with one after reset and is incremented each time the `start_of_burst` signal is asserted on the source user interface.
Word Count	31–0	Tracks the number of valid sample words that have been transferred, across all bursts, to the source user interface.

5.3.1.4. Traffic Checker

The traffic checker performs the following inspections to verify that the received data conforms to the expected format:

- Checks each sample word to verify that the expected word ID was received.
- Checks each sample word to verify that the word count value is higher than the word count value from the last valid sample word.
- Verifies that lane de-skew has been properly performed by validating that the word count and burst count values from the sample word are the same as the values received from the adjacent lane.
- If the `start_of_burst` signal is asserted on the user interface, verifies that the burst count value in the current sample word is higher than the burst count value from the last valid sample word. Otherwise, it verifies that the burst count value has not changed.

5.3.1.5. Demo Control

The demo control module is a Nios II processor system, generated in Platform Designer (Standard), to control the demo hardware.

Demo control module also consists of a timer to track interrupt occurrence, Avalon-MM interface to access demo management and the Serial Lite III Streaming Intel FPGA IP PHY interface, a reset controller, a UART interface, and an Avalon Streaming (Avalon-ST) interface.

5.3.1.6. Demo Management

The demo management module controls the user modules interaction with the Serial Lite III Streaming IP core such as enable and disable traffic generator and traffic checker, enable CRC error insertion, and provide user clock reset for Serial Lite III Streaming IP core. The module also implements CSRs to control and monitor the design operation. This includes CSRs to monitor and log errors that occur during the operation.

5.3.1.7. Nios II Processor Code

The Nios II processor controls the options exercised in the design example. The code also enables CRAM bits for CRC-32 error injection support.

The design example sets the bit for channel 0 that connects to lane 0 in the design example. Therefore, CRC error injection is exercisable for lane 0 only. Refer to the Nios II processor source code (`demo_control.c`) for information on setting bits for other channels.

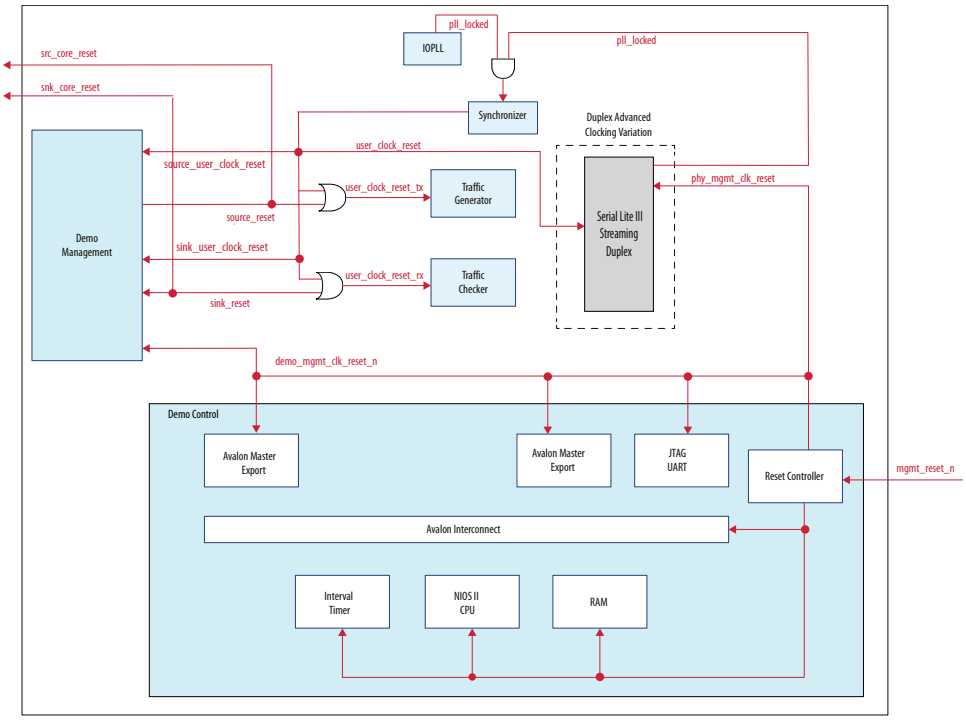
The `demo_control.c` program for Intel Stratix 10 E-tile devices uses the Transceiver PHY dynamic reconfiguration block to control registers to dynamically toggle the Transceiver PHY block `seriallpback` to change the TX to RX loopback from internal to external. The `demo_control` program also uses the Transceiver PHY dynamic reconfiguration to enable initial coarse adaptive equalization to reduce bit error during high data rate transmission.

5.3.2. Reset Scheme

The `mgmt_reset_n` reset signal controls the overall reset structure for the design example. This is an asynchronous and active-low signal. Asserting this signal resets the demo control module and the Serial Lite III Streaming IP core. The traffic generator and traffic checker modules get reset through the demo management and the reset synchronizer.

The following diagram shows the reset scheme implemented in the design example.

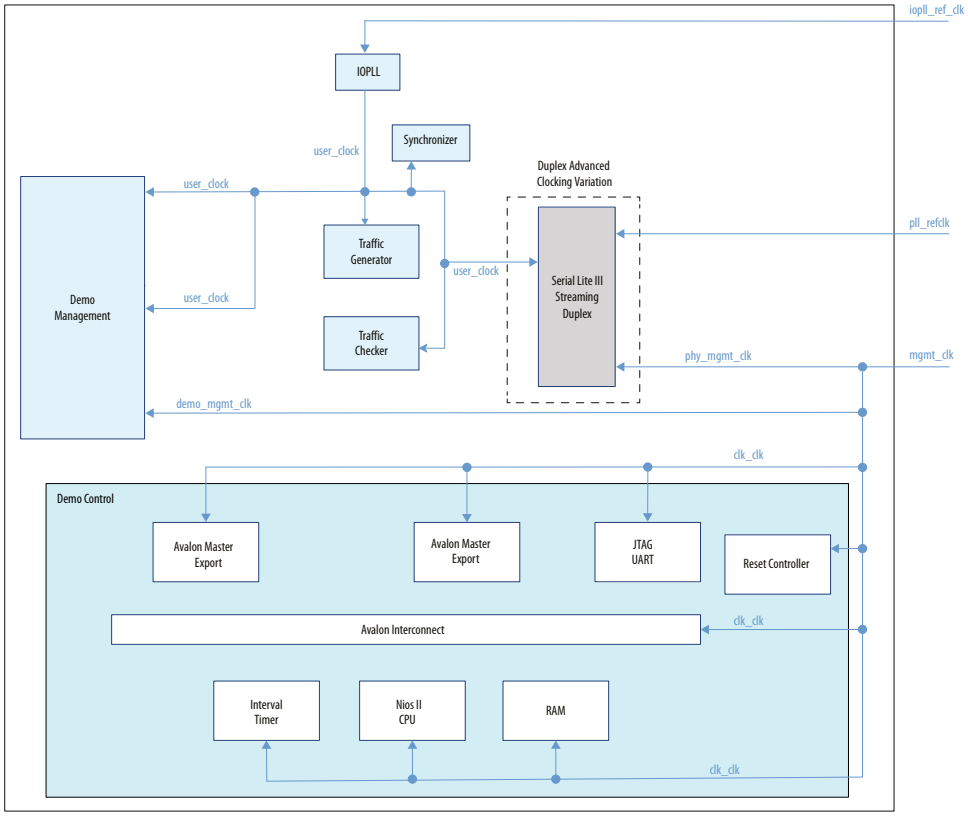
Figure 42. Reset Scheme for Intel Stratix 10 E-tile Serial Lite III Streaming Duplex Core in Advanced Clocking Mode



5.3.3. Clocking Scheme

The following diagram shows the clocking scheme for the design example.

Figure 43. Clocking Scheme for Intel Stratix 10 E-tile Serial Lite III Streaming Duplex Core in Advanced Clocking Mode



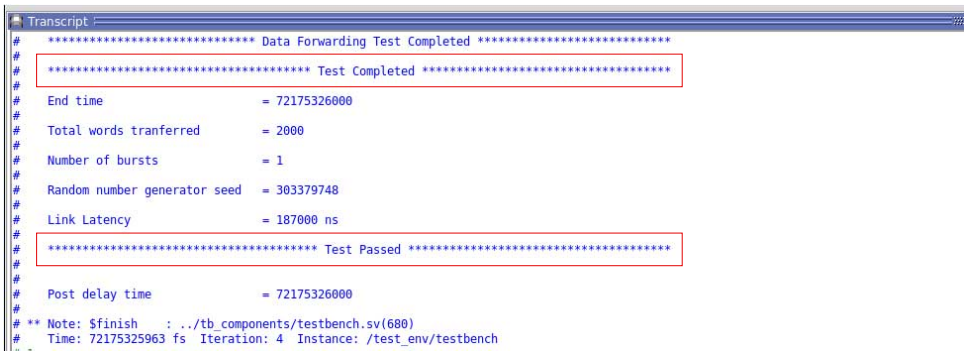
5.4. Simulation

The simulation test cases demonstrate continuous streaming of 2000 sample data from the traffic generator to the Serial Lite III Streaming source core and externally loopback to the sink core in advanced clocking mode.

The simulation test case performs the following steps:

1. Initialize and configures Serial Lite III Streaming IP core, traffic generator and traffic checker.
2. Traffic generator generates data and starts data transmission.
3. Logs and display link up status and burst information.
4. Traffic checker verifies received data and stop transmission.
5. Testbench logs and displays test result and test information.

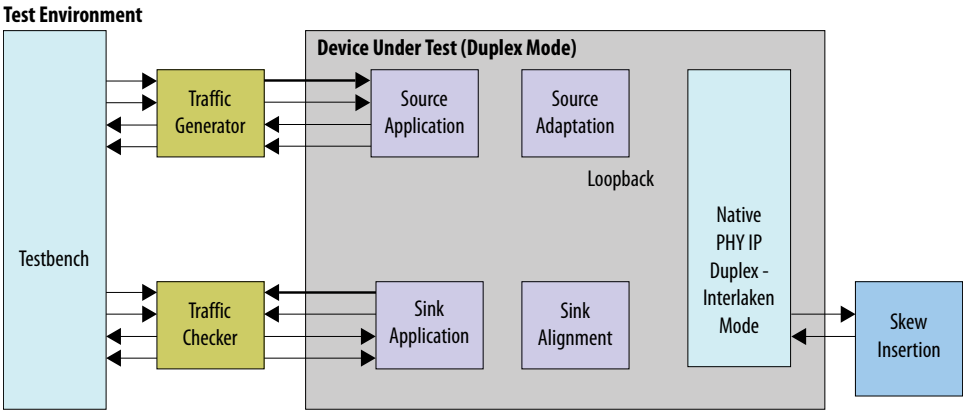
Figure 44. Sample of Successful Simulation



5.4.1. Testbench

The generated example testbench is dynamic and has the same configuration as the IP.

Figure 45. Serial Lite III Streaming Example Testbench (Duplex) for Intel Stratix 10 E-tile Advanced Clocking Mode



5.5. Hardware Testing

After you download the design and the accompanying software into the FPGA, you can test the design through an interactive session. The interactive session provides helpful statistics, and enables you to control various aspects of the design.

You can control the following operations by entering the numbers listed below:

- **0) Toggle Loopback Mode** - Toggles TX to RX serial loopback path within the transceiver or external loopback mode. The loopback mode is specified in the interactive session. Disable the traffic generator/checker before switching loopback modes to avoid transmission error.
- **1) Enable Data Generator/Checker** - Enables the traffic generator and start sending out data.
- **2) Disable Data Generator/Checker** - Disables traffic generation.
- **3) Reset Source Core** - Resets the source core and traffic generator.

- **4) Reset Sink Core** - Resets the sink core and traffic checker.
- **5) Display Error Details** - Displays the error statistics.
- **6) Toggle Burst/Continuous Mode** - Resets the source and sink MACs and switches the traffic generator to generate a burst (multiple burst packet data) or continuous (single continuous data) traffic stream. By default, the design example is set to burst mode. When in continuous mode, the burst count will always show 1. Disable the data generator/checker before switching mode to avoid transmission error.
- **7) Toggle CRC Error Insertion** - Turns CRC error injection off or on (for all lanes). By default, the design example has CRC error injection turned off.

Note: Options 8 and 9 applicable only in standard clocking mode.

Figure 46. Example of a Successful Hardware Test When Data Generator/Checker is Enabled

Test report with zero errors indicates a successful data transmission.

```
Source Errors

   Adaptation FIFO Overflow:                0


Sink Errors

   Adaptation FIFO Overflow:                0
   Loss of Alignment During Normal Operation: 0
   Lane 0 Meta Frame CRC Errors:            0
   Lane 1 Meta Frame CRC Errors:            0
   Lane 2 Meta Frame CRC Errors:            0
   Lane 3 Meta Frame CRC Errors:            0
   Lane 4 Meta Frame CRC Errors:            0
   Lane 5 Meta Frame CRC Errors:            0


Traffic Checker Errors

   Lane Swap Errors:                        0
   Lane Sequence Errors:                    0
   Lane Alignment Errors:                   0

Press any key to return to main menu:
```

5.5.1. Design Setup

The design example targets the Intel Stratix 10 TX Transceiver Signal Integrity Development Kit.

The design includes an SDC script as well as a QSF file with verified constraints in loopback mode. If you use the design example with another device or development board, you may need to update the device setting and constraints in the QSF file.

5.5.2. Error Details

These are the list of errors reported when you run the design example.

Table 15. Details of Errors Reported

Error	Description
Source Error:	
Adaptation FIFO Overflow	To indicate source adaptation FIFO overflow error.
Sink Errors:	
Loss of Alignment During Normal Operation	To indicate loss of alignment error (`error_rx[1]`).
Meta Frame CRC Errors	To indicate CRC errors.
Lane Swap Errors	To indicate lane swap errors in traffic checker.
Lane Sequence Errors	To indicate lane sequence error in traffic checker.
Lane Alignment Errors	To indicate lane alignment error in traffic checker.

5.6. Signals

Figure 47. Top-level Signals for Intel Stratix 10 E-tile Serial Lite III Streaming Advanced Clocking Mode Design Example

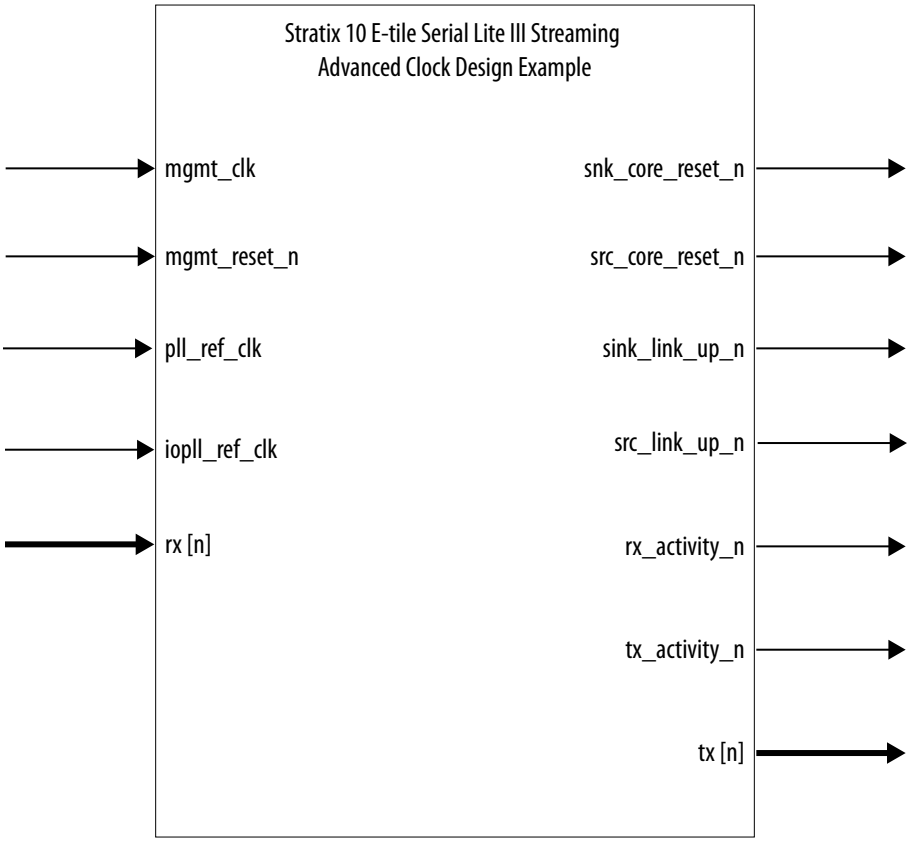


Table 16. Design Example Interface Signals

Signal	Direction	Width	Description
Clock and Reset Signal			
mgmt_clk	Input	1	Input clock for: • Avalon-MM PHY management interface for Serial Lite III Streaming IP core • Demo management module • Demo control module • Transceiver reset controller
pll_ref_clk	Input	1	This reference clock is used by the Clock Data Recovery (CDR) unit in the transceiver. It serves as a reference for the CDR to recover the clock from the serial line. The frequency of this clock must match the frequency you select in the IP parameter editor.
iopll_ref_clk	Input	1	This clock is used as a reference clock for the IOPLL user clock.
mgmt_reset_n	Input	1	Design example asynchronous master reset. Assert this reset signal to reset the overall design example system. This is an active low signal.
snk_core_reset_n	Output	1	Demo management module asserts this signal to reset traffic checker module.
src_core_reset_n	Output	1	Demo management module asserts this signal to reset traffic generator module.
Data Signal			
rx[n]	Input	Based on **Number of Lanes** value	This vector carries the transmitted streaming data from the core. *n* represents the number of lanes.
tx[n]	Output	Based on **Number of Lanes** value	This vector carries the transmitted streaming data to the core. *n* represents the number of lanes.
Status Signal			
rx_activity_n	Output	1	This single bit signal indicates that the data is valid.
tx_activity_n	Output	1	This single bit signal indicates that the data is valid.
snk_link_up_n	Output	1	The core asserts this signal to indicate that the core initialization is complete and is ready to receive user data.
src_link_up_n	Output	1	The core asserts this signal to indicate that the core initialization is complete and is ready to transmit user data.

6. Serial Lite III Streaming Intel Stratix 10 FPGA IP Design Example User Guide Archives

If an IP core version is not listed, the user guide for the previous IP core version applies.

IP Core Version	User Guide
17.1	SerialLite III Streaming IP Core Design Example User Guide for Intel Stratix 10 Devices

7. Document Revision History for Serial Lite III Streaming Intel Stratix 10 FPGA IP Design Example User Guide

Document Version	Intel Quartus Prime Version	Changes
2018.12.28	18.1	• Renamed the IP core to Serial Lite III Streaming Intel FPGA IP. • Renamed the document to *SerialLite III Streaming Intel Stratix 10 FPGA IP Design Example User Guide*. • Added design example presets for Intel Stratix 10 E-tile devices: — Standard and Advanced Clocking Mode 2x25.0G — Standard and Advanced Clocking Mode 4x28.0G — Standard and Advanced Clocking Mode 6x12.5G — Standard and Advanced Clocking Mode 6x17.4G • Added new sections for the Intel Stratix 10 E-tile Standard and Advanced Clocking Mode design examples. • Added new design example presets for Intel Stratix 10 H-tile and L-tile devices: — Standard and Advanced Clocking Mode 2x25.0G — Standard and Advanced Clocking Mode 4x28.0G • Added simplex mode support for Intel Stratix 10 H-tile and L-tile design examples. Intel Stratix 10 E-tile design examples support only duplex mode. • Added simplex mode block diagrams for the Intel Stratix 10 H-tile and L-tile design examples. • Added an example of a successful simulation in the *Simulation* sections and examples of successful tests in the *Hardware Testing* sections. • Updated the *Error Details* section to include source error about adaptation FIFO overflow. • Updated the *Parameter Settings for Intel Stratix 10 Design Example Standard and Advanced Clocking Presets* tables with E-tile information.

Date	Version	Changes
November 2017	2017.11.06	• Rebranded as Intel. • Renamed the document as *SerialLite III Streaming IP Core Design Example User Guide for Intel Stratix 10 Devices*. • Updated the "Parameters in the Example Design Tab" table: Updated the descriptions for **Select Board** parameter.
May 2017	2017.05.08	• Initial release.