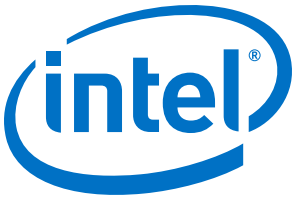

Intel® Stratix® 10 Low Latency 40G Ethernet Design Example User Guide

Updated for Intel® Quartus® Prime Design Suite: **19.1**

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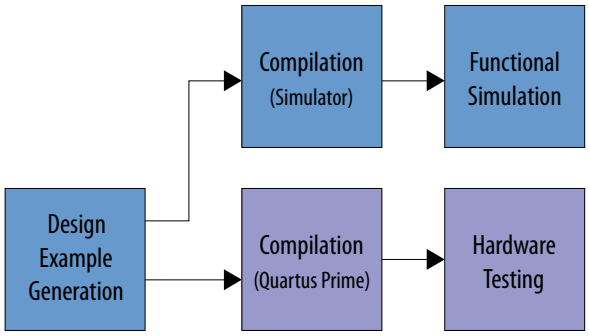
Contents

1. Quick Start Guide

The Intel Stratix® 10 Low Latency (LL) 40G Ethernet IP core provides a simulatable testbench and a hardware design example that supports compilation and hardware testing. When you generate the design example, the parameter editor automatically creates the files necessary to simulate, compile, and test the design in hardware. You can download the compiled hardware design to the Intel Stratix 10 GX Transceiver Signal Integrity Development Kit. The testbench and demonstration design example are available for a wide range of parameters. However, they do not cover all possible parameterizations of the Intel Stratix 10 LL 40GbE IP Core.

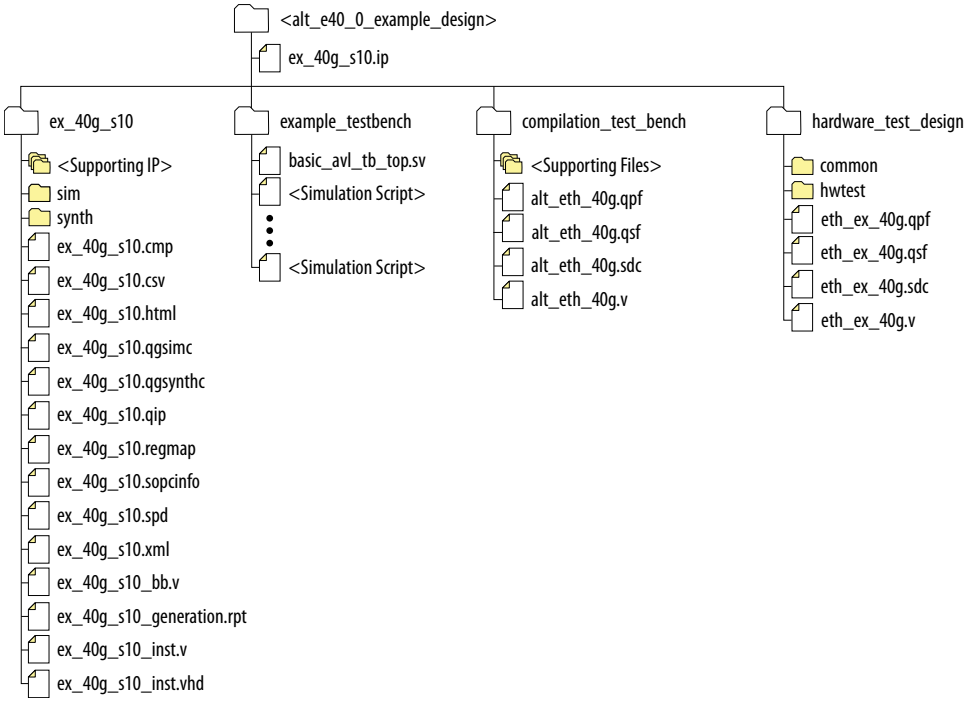
In addition, for most IP core variations, Intel provides a compilation-only example project that you can use to quickly estimate IP core area and timing.

Figure 1. Development Steps for the Design Example



1.1. Directory Structure

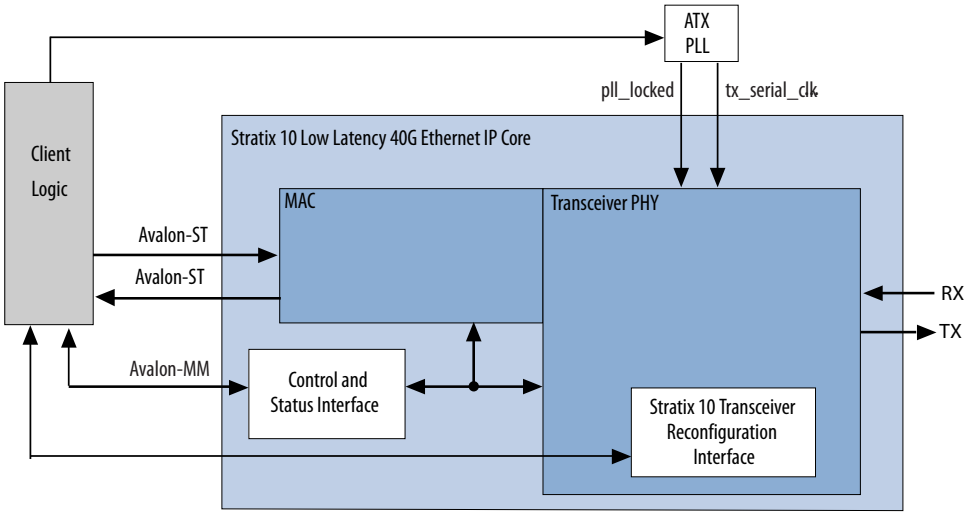
Figure 2. Directory Structure for the Generated Design Example



The hardware configuration and test files (the hardware design example) are located in *<design_example_dir>*/hardware_test_design. The simulation files (testbench for simulation only) are located in *<design_example_dir>*/example_testbench. The compilation-only example design is located in *<design_example_dir>*/compilation_test_design.

1.2. Simulation Design Example Components

Figure 3. Intel Stratix 10 LL 40GbE Design Example Block Diagram



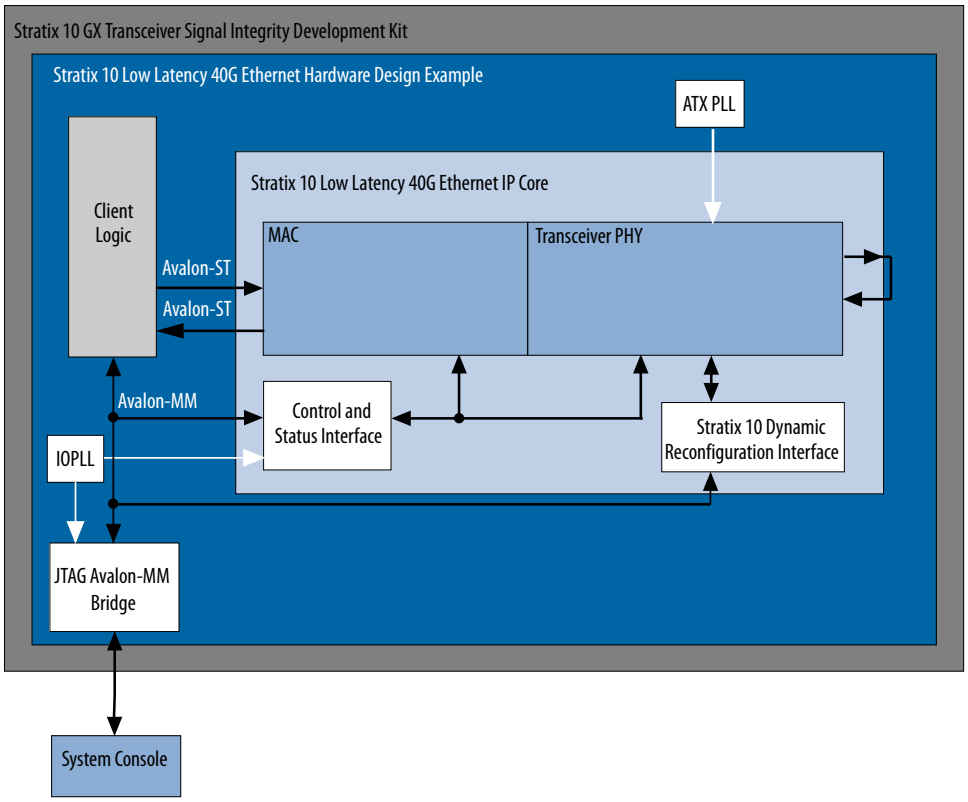
The simulation design example top-level test file is `basic_avl_tb_top.sv`. This file instantiates and connects an ATX PLL. It includes a task to send and receive 10 packets. The simulation design example for 40GBASE-KR4 variations also exercises auto-negotiation and link training, if enabled.

Table 1. Intel Stratix 10 LL 40GbE IP Core Testbench File Descriptions

File Names	Description
Testbench and Simulation Files	
`basic_avl_tb_top.sv`	Top-level testbench file. The testbench instantiates the DUT and runs Verilog HDL tasks to generate and accept packets. The testbench also implements auto-negotiation and link training if enabled in a 40GBASE-KR4/CR4 DUT.
Testbench Scripts	
`run_vsim.do`	The ModelSim script to run the testbench.
`run_vcs.sh`	The Synopsys VCS script to run the testbench.

1.3. Hardware Design Example Components

Figure 4. Intel Stratix 10 LL 40GbE Hardware Design Example High Level Block Diagram



The Intel Stratix 10 LL 40GbE hardware design example includes the following components:

- Intel Stratix 10 LL 40GbE IP core.
- Client logic that coordinates the programming of the IP core, and packet generation and checking.
- ATX PLL to drive the device transceiver channel clocks.
- IOPLL to generate a 100 MHz clock from a 50 MHz input clock to the hardware design example.
- JTAG controller that communicates with the Intel System Console. You communicate with the client logic through the System Console.

Table 2. Intel Stratix 10 LL 40GbE IP Core Hardware Design Example File Descriptions

File Names	Description
`eth_ex_40g.qpf`	Intel Quartus® Prime project file.
`eth_ex_40g.qsf`	Quartus project settings file.
`eth_ex_40g.sdc`	Synopsys Design Constraints file. You can copy and modify this file for your own Intel Stratix 10 LL 40GbE design.

continued...

File Names	Description
`eth_ex_40g.v`	Top-level Verilog HDL design example file.
`common/`	Hardware design example support files.
`hwtest/main.tcl`	Main file for accessing System Console.

1.4. Generating the Design Example

Figure 5. Procedure

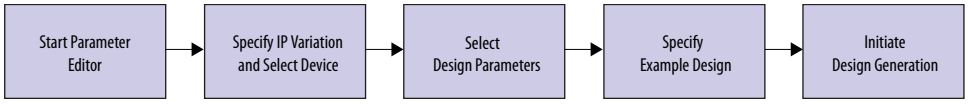
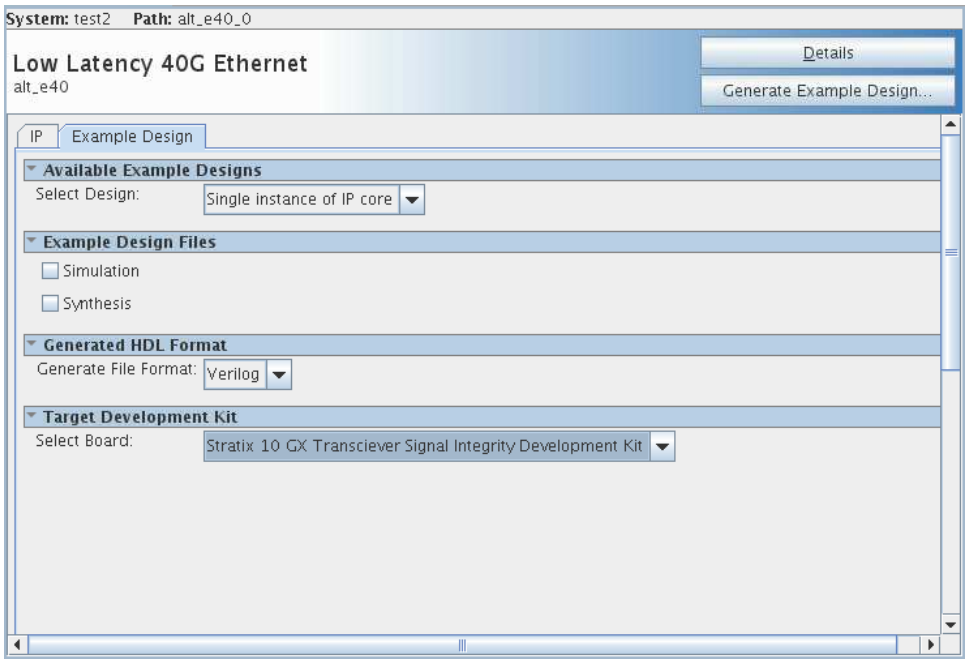


Figure 6. Example Design Tab in the Intel Stratix 10 LL 40GbE Parameter Editor



Follow these steps to generate the hardware design example and testbench:

1. In the Intel Quartus Prime Pro Edition, click **File ➤ New Project Wizard** to create a new Intel Quartus Prime project, or **File ➤ Open Project** to open an existing Intel Quartus Prime project. The wizard prompts you to specify a device family and device.

Note: The design example overwrites the selection with the device on the target board. You specify the target board from the menu of design example options in the Example Design tab (Step 8). At the time of publication (2017.05.08), only a single target board is available, the design example DUT if you select an H-tile device is 1SG280HU3F50E3VGS1, and the design example DUT if you select an L-tile device is 1SG280LU3F50E3VGS1.

2. In the IP Catalog, locate and select **Low Latency 40G Ethernet**. The **New IP Variation** window appears.
3. Specify a top-level name <*your_ip*> for your custom IP variation. The parameter editor saves the IP variation settings in a file named <*your_ip*>`.ip`.
4. Click **OK**. The parameter editor appears.
5. On the **IP** tab, specify the parameters for your IP core variation.

   Note: The Intel Stratix 10 LL 40GbE design example does not simulate correctly and does not function correctly in hardware for the following selections:

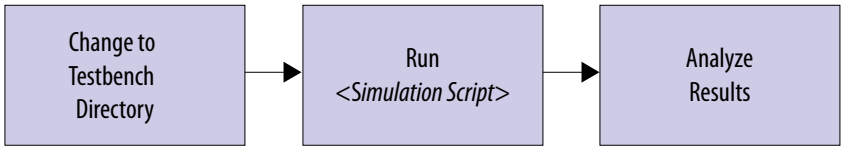
   - Use external TX MAC PLL
   - Enable preamble pass-through turned on
   - Ready latency set to the value of 3
   - Enable TX CRC insertion turned off
6. On the **Example Design** tab, under **Example Design Files**, select the **Simulation** option to generate the testbench, and select the **Synthesis** option to generate the compilation-only and hardware design examples.
7. On the **Example Design** tab, under **Generated HDL Format**, only Verilog HDL is available. This IP core does not support VHDL.
8. Under **Target Development Kit** select the **Stratix 10 GX Transceiver Signal Integrity Development Kit**. You must ensure your project targets the specific Stratix 10 device on the development board.
9. Click the **Generate Example Design** button. The **Select Example Design Directory** window appears.
10. If you wish to modify the design example directory path or name from the defaults displayed (`alt_e40_0_example_design`), browse to the new path and type the new design example directory name (<*design_example_dir*>).
11. Click **OK**.

Related Information

- IP Core Parameters
  Provides more information about customizing your IP core.
- Stratix 10 GX Signal Integrity Development Kit

1.5. Simulating the Intel Stratix 10 LL 40GbE Design Example Testbench

Figure 7. Procedure



Follow these steps to simulate the testbench:

1. Change to the testbench simulation directory *<design_example_dir>*/`example_testbench`.
2. Run the simulation script for the supported simulator of your choice. The script compiles and runs the testbench in the simulator. Refer to the table "Steps to Simulate the Testbench".
3. Analyze the results. The successful testbench sends ten packets, receives ten packets, and displays `"Testbench complete."`

   Note: The successful 40GBASE-KR4/CR4 testbench performs auto-negotiation (if enabled) and link training (if enabled) before performing these packet send and receive actions.

Table 3. Steps to Simulate the Testbench

Simulator	Instructions
ModelSim	In the command line, type `vsim -do run_vsim.do` If you prefer to simulate without bringing up the ModelSim GUI, type `vsim -c -do run_vsim.do` *Note:* The ModelSim* - Intel FPGA Edition simulator does not have the capacity to simulate this IP core. You must use another supported ModelSim simulator such as ModelSim SE.
VCS	In the command line, type `sh run_vcs.sh`

The successful test run displays output confirming the following behavior:

1. Waiting for RX clock to settle
2. Printing PHY status
3. Sending 10 packets
4. Receiving 10 packets
5. Displaying `"Testbench complete."`

The following sample output illustrates a successful simulation test run. For a 40GBASE-KR4/CR4 IP core variation, additional auto-negotiation and link training messages display if these features are enabled.

```
#Waiting for RX alignment
#RX deskew locked
#RX lane alignment locked
#TX enabled
#**Sending Packet    1...
#**Sending Packet    2...
#**Sending Packet    3...
#**Sending Packet    4...
```

```
#**Sending Packet    5...
#**Sending Packet    6...
#**Sending Packet    7...
#**Received Packet   1...
#**Sending Packet    8...
#**Received Packet   2...
#**Sending Packet    9...
#**Received Packet   3...
#**Sending Packet    10...
#**Received Packet   4...
#**Received Packet   5...
#**Received Packet   6...
#**Received Packet   7...
#**Received Packet   8...
#**Received Packet   9...
#**Received Packet   10...
#**
#** Testbench complete.
#**
#****************************************
```

1.6. Compiling and Configuring the Design Example in Hardware

To compile the hardware design example and configure it on your Stratix 10 device, follow these steps:

1. Ensure hardware design example generation is complete.
2. In the IntelIntel Quartus Prime Pro Edition software, open the Intel Quartus Prime project `<design_example_dir>/hardware_test_design/eth_ex_40g.qpf`.
3. On the Processing menu, click **Start Compilation**.
4. After successful compilation, a SRAM object file (`.sof`) is available for non-40GBASE-KR4 variations. Follow these steps to program the hardware design example on the Stratix 10 device:
   a. On the **Tools** menu, click **Programmer**.
   b. In the Programmer, click **Hardware Setup**.
   c. Select a programming device.
   d. Select and add the Stratix 10 GX Transceiver Signal Integrity Development Kit to which your Intel Quartus Prime session can connect.
   e. Ensure that **Mode** is set to **JTAG**.
   f. Select the Stratix 10 device and click **Add Device**. The Programmer displays a block diagram of the connections between the devices on your board.
   g. In the row with your `.sof`, check the box for the `.sof`.
   h. Check the box in the **Program/Configure** column.
   i. Click **Start**.

Related Information

- Incremental Compilation for Hierarchical and Team-Based Design
- Programming Intel FPGA Devices

1.7. Testing the Intel Stratix 10 LL 40GbE Hardware Design Example

After you compile the Intel Stratix 10 LL 40GbE IP core design example and configure it on your Stratix 10 device, you can use the Intel System Console to program the IP core and its embedded Native PHY IP core registers.

To turn on the System Console and test the hardware design example, follow these steps:

1. After the hardware design example is configured on the Stratix 10 device, in the Intel Quartus Prime Pro Edition software, on the **Tools** menu, click **System Debugging Tools ➤ System Console**.
2. In the Tcl Console pane, type `cd hwtest` to change directory to `<design_example_dir>/hardware_test_design/hwtest`.
3. Type `source main.tcl` to open a connection to the JTAG master.

You can program the IP core with the following design example commands:

- `chkphy_status`: Displays the clock frequencies and PHY lock status.
- `chkmac_stats`: Displays the values in the MAC statistics counters.
- `clear_all_stats`: Clears the IP core statistics counters.
- `start_pkt_gen`: Starts the packet generator.
- `stop_pkt_gen`: Stops the packet generator.
- `loop_on`: Turns on internal serial loopback
- `loop_off`: Turns off internal serial loopback.
- `reg_read <addr>`: Returns the IP core register value at <*addr*>.
- `reg_write <addr> <data>`: Writes <*data*> to the IP core register at address <*addr*>.

Related Information

- Intel Stratix 10 LL 40GbE Design Example Registers on page 13
  Register map for hardware design example.
- Analyzing and Debugging Designs with System Console

2. Design Example Description

The design example demonstrates the functions of the Intel Stratix 10 LL 40GbE core with transceiver interface compliant with the IEEE 802.3ba standard CAUI-4 specification. You can generate the design from the **Example Design** tab in the Intel Stratix 10 LL 40GbE parameter editor.

To generate the design example, you must first set the parameter values for the IP core variation you intend to generate in your end product. Generating the design example creates a copy of the IP core; the testbench and hardware design example use this variation as the DUT. If you do not set the parameter values for the DUT to match the parameter values in your end product, the design example you generate does not exercise the IP core variation you intend.

Note: The testbench demonstrates a basic test of the IP core. It is not intended to be a substitute for a full verification environment. You must perform more extensive verification of your own Intel Stratix 10 LL 40GbE design in simulation and in hardware.

Related Information

Intel Stratix 10 Low Latency 40-Gbps Ethernet IP Core User Guide

2.1. Design Example Behavior

The testbench sends traffic through the IP core, exercising the transmit side and receive side of the IP core. In the hardware design example, you can program the IP core in internal serial loopback mode and generate traffic on the transmit side that loops back through the receive side.

2.2. Design Example Interface Signals

The Intel Stratix 10 LL 40GbE testbench is self-contained and does not require you to drive any input signals.

Table 4. Intel Stratix 10 LL 40GbE Hardware Design Example Interface Signals

Signal	Direction	Comments
clk50	Input	Drive at 50 MHz. The intent is to drive this from a 50 Mhz oscillator on the board. The hardware design example routes this clock to the input of an IOPLL on the device and configures the IOPLL to drive a 100 MHz clock internally.
clk_ref	Input	Drive at 644.53125 MHz.

continued...

Signal	Direction	Comments
`cpu_resetn`	Input	Resets the IP core. Active low. Drives the global hard reset `csr_reset_n` to the IP core.
`tx_serial[3:0]`	Output	Transceiver PHY output serial data.
`rx_serial[3:0]`	Input	Transceiver PHY input serial data.
`user_led[7:0]`	Output	Status signals. The hardware design example connects these bits to drive LEDs on the target board. Individual bits reflect the following signal values and clock behavior: • [0]: Main reset signal to IP core • [1]: Divided version of `clk_ref` • [2]: Divided version of `clk50` • [3]: Divided version of 100 MHz status clock • [4]: `tx_lanes_stable` • [5]: `rx_block_lock` • [6]: `rx_am_lock` • [7]: `rx_pcs_ready`

Related Information

Interfaces and Signal Descriptions
Provides detailed descriptions of the Intel Stratix 10 LL 40GbE IP core signals and the interfaces to which they belong.

2.3. Intel Stratix 10 LL 40GbE Design Example Registers

Table 5. Intel Stratix 10 LL 40GbE Hardware Design Example Register Map

Lists the memory mapped register ranges for the hardware design example. You access these registers with the `reg_read` and `reg_write` functions in the Intel System Console.

Word Offset	Register Type
0xB0-0xFF	Intel Stratix 10 LL 40GBASE-KR4/CR4 registers
0x300-0x3FF	PHY registers
0x400-0x4FF	TX MAC registers
0x500-0x5FF	RX MAC registers
0x800-0x8FF	Statistics Counter registers - TX direction
0x900-0x9FF	Statistics Counter registers - RX direction
0x1000-1016	Packet Client registers

Table 6. Packet Client Registers

You can customize the Intel Stratix 10 LL 40GbE hardware design example by programming the packet client registers.

Addr	Name	Bit	Description	HW Reset Value	Access
0x1000	PKT_CL_SCRATCH	[31:0]	Scratch register available for testing.		RW
0x1001	PKT_CL_CLNT	[31:0]	Four characters of IP block identification string "CLNT"		RO
0x1008	Packet Size Configure	[29:0]	Specify the transmit packet size in bytes. These bits have dependencies to PKT_GEN_TX_CTRL register. • Bit [29:16]: Specify the upper limit of the packet size in bytes. This is only applicable to incremental mode. • Bit [13:0]: — For fixed mode, these bits specify the transmit packet size in bytes. — For incremental mode, these bits specify the incremental bytes for a packet.	0x25800040	RW
0x1009	Packet Number Control	[31:0]	Specify the number of packets to transmit from the packet generator.	0xA	RW
0x1010	PKT_GEN_TX_CTRL	[7:0]	• Bit [0]: Reserved. • Bit [1]: Packet generator disable bit. Set this bit to the value of 1 to turn off the packet generator, and reset it to the value of 0 to turn on the packet generator. • Bit [2]: Reserved. • Bit [3]: Has the value of 1 if the IP core is in MAC loopback mode; has the value of 0 if the packet client uses the packet generator. • Bit [5:4]: — 00: Random mode — 01: Fixed mode — 10: Incremental mode • Bit [6]: Set this bit to 1 to use 0x1009 register to turn off packet generator based on a fixed number of packets to transmit. Otherwise, bit [1] of PKT_GEN_TX_CTRL register is used to turn off the packet generator. • Bit [7]: — 1: For transmission without gap in between packets. — 0: For transmission with random gap in between packets.	0x6	RW
0x1011	Destination address lower 32 bits	[31:0]	Destination address (lower 32 bits)	0x56780ADD	RW
0x1012	Destination address upper 16 bits	[15:0]	Destination address (upper 16 bits)	0x1234	RW

continued...

Addr	Name	Bit	Description	HW Reset Value	Access
0x1013	Source address lower 32 bits	[31:0]	Source address (lower 32 bits)	0x43210ADD	RW
0x1014	Source address upper 16 bits	[15:0]	Source address (upper 16 bits)	0x8765	RW
0x1016	PKT_CL_LOOPBACK_RESET	[0]	MAC loopback reset. Set to the value of 1 to reset the design example MAC loopback.	1'b0	RW

Related Information

- Testing the Intel Stratix 10 LL 40GbE Hardware Design Example on page 11
  System Console commands to access the IP core and Native PHY registers.
- Intel Stratix 10 LL 40GbE Control and Status Register Descriptions
  Describes the Intel Stratix 10 LL 40GbE IP core registers.

A. Document Revision History for Intel Stratix 10 Low Latency 40G Ethernet Design Example User Guide

Document Version	Intel Quartus Prime Version	Changes
2019.05.15	19.1	Changed "lower" to upper per HSD-ES bug 1507179667.
2018.11.15	18.1	Added the Packet Client registers in section: *Intel Stratix 10 LL 40GbE Design Example Registers*.
2017.05.08	17.1 Intel Stratix 10 ES Editions	Initial release.