Early Power Estimator for Intel® Arria® 10 FPGAs User Guide

Updated for Intel® Quartus® Prime Design Suite: **18.0.1**

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Contents

1. Overview of the Early Power Estimator for Intel® Arria® 10

This user guide describes the Early Power Estimator (EPE) for Intel® Intel Arria® 10.

This user guide provides guidelines for using the EPE, and details about thermal analysis and the factors contributing to FPGA power consumption. You can calculate FPGA power consumption using the Microsoft* Excel-based EPE spreadsheet. For more accurate power estimation, use the Power Analyzer in the Intel Quartus® Prime software.

Intel recommends that you switch from the EPE spreadsheet to the Power Analyzer in theIntel Quartus Prime software once your design is available. The Power Analyzer produces more accurate results because it has more detailed information about your design, including routing and configuration information about each of the resources in your design.

Intel recommends using the EPE results as an estimation of dynamic power, not as a specification. You must verify the actual dynamic power consumption during device operation, because the information is sensitive to the actual device and design input signals. Static power is reported as a limit, and can be considered a specification when reporting with maximum power characteristics and accurate inputs. See the appendix *Measuring Static Power* for information on how to measure device static power in a way that correlates with the way that EPE reports static power.

The features of the EPE spreadsheet include:

- Ability to estimate the power consumption of your design before creating the design or during the design process
- Ability to import device resource information from the Intel Quartus Prime software into the EPE spreadsheet with the use of the Intel Quartus Prime-generated EPE file
- Ability to perform preliminary thermal analysis of your design

Related Information

- Power Analysis Chapter in Volume 3 of the Quartus Prime Handbook
- Arria 10 Core Fabric and General Purpose I/Os Handbook
- Early Power Estimators (EPE) and Power Analyzer

1.1. Power Model Status

The power models in the Early Power Estimator for Arria 10 can be in either preliminary or final status.

Preliminary power models are created based on simulation results, process data, and other known parameters; preliminary power models may change over time. Final power models are corelated to the production device with thousands of designs, and undergo no further changes. The power model status for the selected device is shown in the Main worksheet of the EPE spreadsheet.

The accuracy of the power model is determined on a per-power-rail basis for both the Power Analyzer and the Early Power Estimator. For most designs, the Power Analyzer and the EPE spreadsheet have the following accuracies, with final power models:

- Power Analyzer: Within 10% of silicon for the highest power rails, assuming accurate inputs and toggle rates.
- EPE spreadsheet: Within 20% of silicon for the highest power rails, assuming accurate inputs and toggle rates. Recommended margins are shown in the report tab (see Report tab section).

See Section 5 for information on factors impacting power estimation accuracy.

Related Information

Early Power Estimators (EPE) and Power Analyzer

2. Setting Up the Early Power Estimator for Intel Arria 10

2.1. System Requirements

The Early Power Estimator for Arria 10 requires the following software:

- Windows operating system
- Microsoft Excel 2003, Microsoft Excel 2007, or Microsoft Excel 2010
- Quartus Prime Pro software version 17.0 or later (if generating a file for importation)

Related Information

Operating System Support

2.2. Download and Install the Early Power Estimator

The Early Power Estimator for Arria 10 is available from the *Early Power Estimators (EPE) and Power Analyzer* page on the Intel website.

After you read the terms and conditions and click **I Agree**, you can download the Microsoft Excel (`.xls` or `.xlsx`) file.

By default, the macro security level in Microsoft Excel 2003, Microsoft Excel 2007, and Microsoft Excel 2010 is set to **High**. If the macro security level is set to **High**, macros are automatically disabled. For the features in the EPE spreadsheet to function properly, you must enable macros.

Related Information

Early Power Estimators (EPE) and Power Analyzer

2.2.1. Changing the Macro Security Level in Microsoft Excel* 2003

To change the macro security level in Microsoft Excel* 2003, follow these steps:

1. Click **Tools ➤ Options**.
2. Click **Security ➤ Macro Security**.
3. Select **Security Level ➤ Medium** in the **Security** dialog box then click **Ok**.
4. Click **Ok** in the **Options** window.
5. Close the Early Power Estimator spreadsheet and reopen it.
6. Click **Enable Macros** in the dialog box.

2.2.2. Changing the Macro Security Level in Microsoft Excel* 2007

To change the macro security level in Microsoft Excel* 2007, follow these steps:

1. Click the **Office** button in the upper left corner of the `.xlsx` file.
2. Click the **Excel Options** button at the bottom of the menu.
3. Click the **Trust Center** button on the left. Then, click the **Trust Center Settings** button.
4. Click the **Macro Settings** button in the **Trust Center** dialog box. Turn on the **Disable all macros with notification** option.
5. Close the Early Power Estimator spreadsheet and reopen it.
6. Click **Options** when a security warning appears beneath the Office ribbon.
7. Turn on **Enable this content** in the **Microsoft Office* Security Options** dialog box.

2.2.3. Changing the Macro Security Level in Microsoft Excel* 2010

To change the macro security level in Microsoft Excel 2010, follow these steps:

1. Click **File**
2. Click **Help ➤ Options**
3. Click **Trust Center ➤ Trust Center Settings**
4. Click the **Macro Settings** button in the **Trust Center** dialog box. Turn on the **Disable all macros with notification** option.
5. Close the Early Power Estimator spreadsheet and reopen it.
6. Click **Enable Content** when a security warning appears beneath the Office ribbon.

2.3. Estimating Power Consumption

With the Early Power Estimator, you can estimate power consumption at any point in your design cycle. You can use the EPE to estimate the power consumption when you have not yet begun your design, or if your design is partially complete. Although the EPE can provide a power estimate for your completed design, Intel recommends that you use the Power Analyzer in the Intel Quartus Prime software instead, for a more accurate estimate based on the exact placement and routing information of the completed design.

2.3.1. Estimating Power Consumption Before Starting the FPGA Design

Table 1. Advantage and Constraints of Power Estimation before Designing FPGA

Advantage	Constraint
• You can obtain power estimation before starting your FPGA design. • You can adjust design resources and parameters and see how those changes affect total power consumption.	• Accuracy depends on your inputs and your estimation of the device resources; where this information may change (during or after your design is complete), your power estimation results may be less accurate. • The EPE spreadsheet uses averages and not the actual design implementation details. The Power Analyzer has access to the full design details. For example, the EPE uses average values for ALM configuration, while the Power Analyzer specifies an exact configuration for each ALM..

To estimate power consumption with the EPE spreadsheet before starting your FPGA design, follow these steps:

1. On the Main worksheet of the EPE spreadsheet, select the target family, device, and package from the **Family**, **Device Grade**, **Package**, and **Transceiver Grade** drop-down lists.
2. Enter values for each worksheet in the EPE spreadsheet. Different worksheets in the EPE spreadsheet display different power sections, such as clocks and phase-locked loops (PLLs).
3. The calculator displays the total estimated power consumption in the **Total (W)** cell of the Main worksheet.

2.3.2. Estimating Power Consumption While Creating the FPGA Design

If your FPGA design is partially complete, you can import the EPE file (*<revision name>*`_early_pwr.csv`) generated by the Quartus Prime software to the EPE spreadsheet. After importing the information from the *<revision name>*`_early_pwr.csv` into the EPE spreadsheet, you can edit the EPE spreadsheet to reflect the device resource estimates for your final design.

Table 2. Advantages and Constraints of Power Estimation if your FPGA Design is Partially Complete

Advantage	Constraint
• You can perform power estimation early in the FPGA design cycle. • Provides the flexibility to automatically fill in the Early Power Estimator spreadsheet based on the Quartus Prime software compilation results. • You can adjust design resources and parameters and see how those changes affect total power consumption.	• Accuracy depends on your inputs and your estimation of the device resources; where this information may change (during or after your design is complete), your power estimation results may be less accurate. • The EPE spreadsheet uses averages and not the actual design implementation details. The Power Analyzer has access to the full design details. For example, the EPE uses values for ALM configuration, while the Power Analyzer specifies an exact configuration for each ALM.

Importing a File

To estimate power consumption with the EPE spreadsheet if your FPGA design is partially complete, you can import a file.

Importing a file saves you time and effort otherwise spent on manually entering information into the EPE. You can also manually change any of the values after importing a file.

Generating the EPE File

To generate the EPE file, follow these steps:

1. Compile the partial FPGA design in the Quartus Prime software.
2. On the Project menu, click **Generate Early Power Estimator File** to generate the *<revision name>*`_early_pwr.csv` in the Quartus Prime software.

Importing Data into the EPE Spreadsheet

You must import the EPE file into the EPE spreadsheet before modifying any information in the EPE spreadsheet. Also, you must verify all your information after importing a file.

Importing a file from the Quartus Prime software populates all input values that were specified in the Quartus Prime software. Alternatively, you can import values exported from an earlier version of the EPE spreadsheet.

Input values imported into the EPE spreadsheet are the values taken from the Quartus Prime software as per the design, or the values that were entered into an earlier version of the EPE spreadsheet. You can manually edit the values in the EPE spreadsheet to suit your changing design requirements.

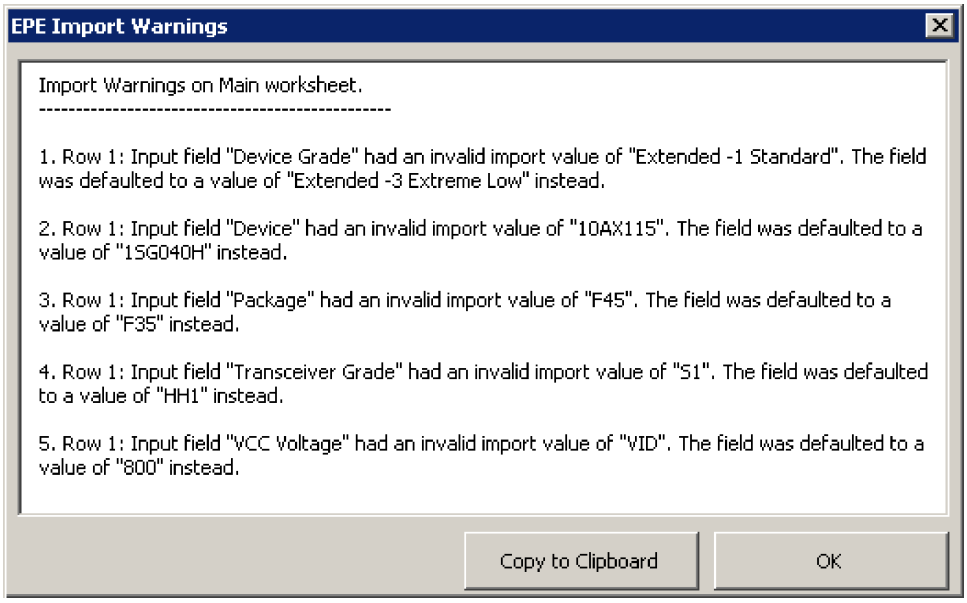
To import data into the EPE spreadsheet, follow these steps:

1. In the EPE spreadsheet, Click **Import CSV**.
2. Browse to a EPE file generated from the Quartus Prime software or an earlier version of the EPE spreadsheet and click **Open**. The file has a name of *<revision name>*`_early_pwr.csv`.
3. After the file is imported, the mouse cursor changes from busy to normal. If there are any warnings during the importation, the EPE produces the **EPE Import Warnings** dialog box. Analyze the warnings carefully to ensure that they are expected. If any of the warnings are unexpected, you must manually modify the

corresponding fields in the EPE after the importation is completed. You can copy all warning messages to the clipboard for future reference by clicking **Copy to Clipboard**. Click **OK** to dismiss the **EPE Import Warnings** dialog box.

The following figure shows example warnings that may occur when importing a design from the EPE spreadsheet for Stratix V devices. The first error message indicates that the board model specified in the earlier version of the EPE spreadsheet is not supported, and that the value was set to Typical instead. The second and third error messages indicate that device ordering codes have changed between the two families, so the previous values for Device and Package input fields could not be imported directly, but were set to their default values instead. Finally, the last two messages indicate that some required information was not found in the imported file, and that corresponding fields were set to their default values. This last message could indicate that the information was not present in the earlier version of the EPE spreadsheet, or that the import file is corrupted.

Figure 1. Example Warning Messages During Importation



Related Information

- Arria 10 EPE - Common Worksheet Elements on page 16
- Arria 10 EPE - Main Worksheet on page 17

2.3.3. Estimating Power Consumption After Completing the FPGA Design

If your design is complete, Intel strongly recommends using the Power Analyzer in the Quartus Prime software. The Power Analyzer provides the most accurate estimate of device power consumption. The Power Analyzer uses toggle rates from simulation, user assignments, and placement-and-routing information to provide accurate power estimates.

Related Information

Power Analysis Chapter in Volume 3 of the Quartus Prime Handbook

3. Early Power Estimator for Intel Arria 10 Graphical User Interface

The graphical user interface (GUI) of the Early Power Estimator for Arria 10 consists of input fields for data entry, output fields for display of results and messages, and buttons to trigger actions. Some fields can serve as both inputs and outputs, and are referred to as input/output fields.

Most input and output fields have tooltips that explain the field's purpose. Fields with tooltips have a red triangle in the top right corner of the field label. Hover your mouse over the label to display the tooltip.

3.1. Early Power Estimator Input Fields

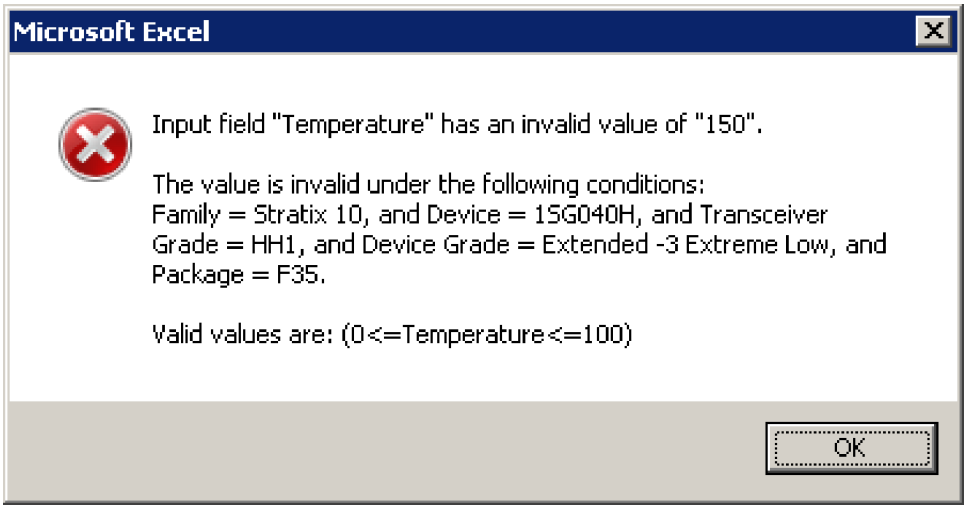
Input fields let you enter information about the device, board, and design for which you want to calculate power estimates. Some input fields let you type values directly, and others let you select from a list of values on a dropdown menu.

Direct Entry Input Fields

Some fields allow you to type values directly into the field. Such fields are often used for data that has a large range of possible values, such as clock frequencies or resource counts.

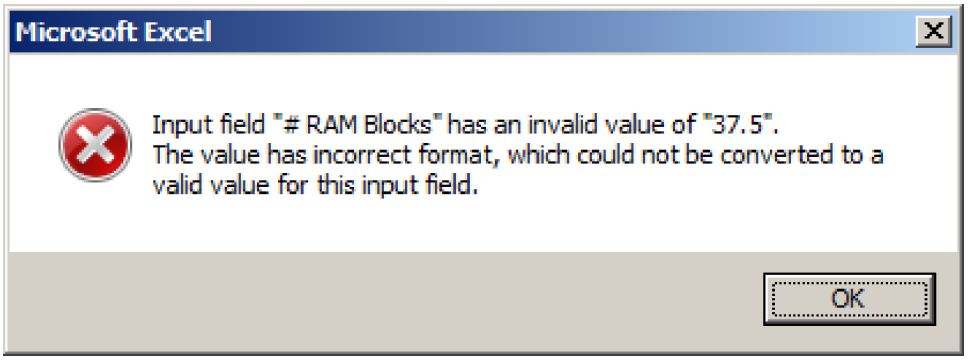
If the value you enter does not pass legality checks, or is inappropriate for the field, the system displays an error message. The error message may indicate the conditions under which a value is invalid, and specify a valid range of values. An example message is shown below. In this example the user has entered a temperature that is outside the allowed range for a selected family, device, transceiver grade, device grade and package combination. The error message also indicates the allowed range of 0 to 100. After the user clicks **OK**, the field value reverts to its previous value.

Figure 2. Example Error Message



If a specific type of numerical value is expected and you enter a text value or a wrong numerical type, the resulting error message indicates that the entered value cannot be converted to the expected data type. An example is shown in the figure below. In this instance, the user has entered a fractional value (37.5) in a field that expects an integer value representing the number of RAM blocks. After the user clicks **OK**, the field reverts to its previous value.

Figure 3. Invalid Value Error Message



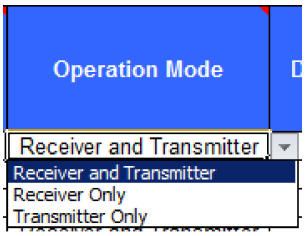
Many fields have restrictions based on the selected family and device. To better understand restrictions on field values, refer to the relevant field description in this user guide, to the tooltip in the appropriate EPE worksheet, or to the Arria 10 Device Handbook.

Note: Although the Early Power Estimator restricts many field values, the restrictions are not exhaustive. In order to provide power estimates at early design stages, when many details of the design are still unknown, the EPE uses a simplified device model that does not account for all possible restrictions. The EPE may accept as legal some values that might not be accepted as legal by the Quartus Prime software.

Dropdown Input Fields

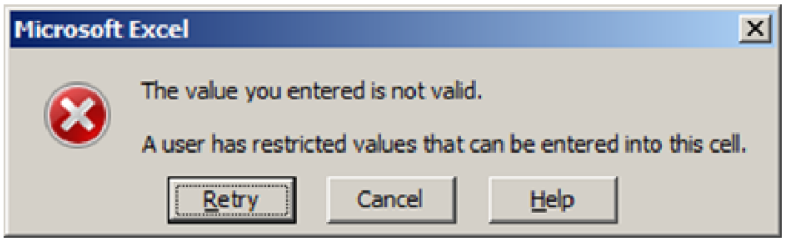
Input fields that have a limited number of valid values often employ a dropdown menu. A dropdown menu is denoted by a downward-pointing arrow that appears when you click in the field. Click in the field a second time to display the list of allowed values. Click the desired value to select it and populate the field. An example dropdown input field is shown in the following figure:

Figure 4. Dropdown Input Field



You can also type a value directly into an input field that has a dropdown menu. To directly enter a value, select the field and press F2, and then type the desired value. The value that you enter must be identical to one of the available values on the dropdown menu, otherwise you will receive an error message.

Figure 5. Value Entered is Not Valid



You can click **Retry** in the error dialog to enter a new value, or click **Cancel** to revert back to the last legal value. Clicking **Help** invokes the generic Excel help window.

3.2. Early Power Estimator Output Fields

Output fields display estimated values for power, current, temperature, or resource utilization for a design specification that you have entered into the Early Power Estimator.

Some output fields, such as thermal power estimates in the **Main** and **Report** worksheets, may display values in red to indicate an error in the design specification. If you encounter results displayed in red, review the relevant worksheet for errors or utilization values exceeding 100%. Correct any errors to obtain reliable power and temperature estimates.

3.3. Early Power Estimator Input/Output Fields

Certain fields may serve as input fields in some configurations, and output fields in others.

For example, you may enter a *Pin Clock Frequency* value manually for some I/O modes, while in other I/O modes *Pin Clock Frequency* is calculated automatically based on values of other input fields.

If you enter a value into an input/output field when it is serving as an output, there is no effect. The value reverts to the calculated value.

3.4. Early Power Estimator Field Shading

The Early Power Estimator for Arria 10 employs shading to distinguish between input and output fields, and to help identify fields with only one allowed value.

Figure 6. Input Fields with Shading

Input Parameters	
Family	Arria 10
Device	10AS016
Device Grade	Extended -1 Low
Package	F27
Transceiver Grade	E3
Power Characteristics	Typical
V_{CC} Voltage (mV)	900
Power Model Status	PRELIMINARY

Thermal Power (W)	
Logic	0.000
RAM	0.000
DSP	0.000
Clock	0.000
PLL	0.000
I/O	0.000
XCVR	0.000
HPS	0.018
P_{STATIC}	0.564
TOTAL (W)	0.582

Regular input fields, such as **Device**, **Device Grade** and **Package** have white shading. White shading also denotes input/output fields.

Input fields that currently have only one allowed value, such as **Transceiver Grade** in this example, have gray shading. In this example, there is only one supported transceiver grade for the selected combination of device, device grade and package. A different combination of device, device grade and package may support more than one transceiver grade, in which case the Transceiver Grade field shading would turn white.

Output fields, such as **Power Model Status**, or **P_{STATIC}** have pale blue shading. Some output fields, such as **TOTAL (W)**, employ a darker shade of blue for emphasis.

3.5. Early Power Estimator Input Field Dependencies

The value you specify for some input fields may affect the allowed values for other fields.

For example, the device package that you select may determine what transceiver grades are selectable. If you change the selected device package, and the currently selected transceiver grade is still legal for the new package, the **Transceiver Grade** value does not change. However, if the currently selected transceiver grade is not compatible with the selected device package, the **Transceiver Grade** value automatically change to one of the legal values.

Changes that you make in one worksheet may affect values on another worksheet, because of dependencies between input fields. For example, if you select a device that does not support the current I/O standard specified in the I/O worksheet, that I/O standard will automatically change to one that is supported by the new device.

In general, the Early Power Estimator for Arria 10 does not automatically change an input value unless it is necessary to preserve the legality of the input. Changes in one field have minimal impact on other fields, while ensuring that overall combination of field values are legal. However, this can sometimes lead to unanticipated results. Consider the following example:

Assume that **Dev1** is selected in the Main worksheet, and I/O standard **IO1** is selected in the I/O worksheet. Assume also that device **Dev1** supports I/O standards **IO1** and **IO2**. Suppose that you change the device selection to **Dev2**, which supports only one I/O standard, **IO2**. As a result of you changing the device selection, the I/O standard in the I/O worksheet will change to **IO2**. If you then reverted the device selection back to **Dev1**, the I/O standard would not change, because **IO2** is a legal I/O standard value for the device **Dev1**. The important point to note, is that the changing of device from **Dev1** to **Dev2** and back again, had the—potentially unintended—consequence of changing the I/O standard in the I/O worksheet.

Note: In most cases, field dependencies are limited to the same worksheet, and often even within the same row. However, device, device grade, package and transceiver grade selection can have a much wider impact, as illustrated above. A simple way to verify that no unintended changes resulted from changing a device is to use the **Export CSV** function to export the EPE state before and after the change in device selection. You can then compare the two CSV files using a third-party *diff* utility to identify any fields that have changed.

3.6. Early Power Estimator Buttons

The Early Power Estimator for Arria 10 provides buttons for resetting the EPE, for importing or exporting a comma-separated value (.csv) file, and for navigating between worksheets.

- The **Manage Power Rail Configuration** button opens the **Report** tab, where you can choose power rail configurations.
- The **Manage Power Regulators** button opens the **Enpirion** tab.

4. Early Power Estimator Worksheets for Intel Arria 10

The Early Power Estimator (EPE) for Arria 10 is an Excel-based spreadsheet that allows you to enter information into worksheets based on architectural features. The EPE then reports, in watts, subtotals of the power consumed by each architectural feature.

For more information about each architectural feature refer to the respective worksheets.

4.1. Arria 10 EPE - Common Worksheet Elements

The Early Power Estimator (EPE) for Arria 10 is divided into multiple worksheets, each allowing entry of a subset of FPGA resources. Some elements are common to more than one worksheet.

Total Thermal Power

The Total Thermal Power field estimates the total thermal power consumed by all FPGA resources in the specific worksheet. Some worksheets may also provide a breakdown of the components contributing to the Total Thermal Power.

Resource Utilization

Most worksheets contain one or more fields that provide an estimate of the percentage resource utilization for the modules in the specific worksheet. Such values are calculated based on the maximum available resources of a given type for a selected device. If resource utilization exceeds 100%, the value is highlighted in red to

alert you that the current device may not be able to support the resources entered into the worksheet. Additionally, the thermal power value displayed in the **Main** and **Report** worksheets is displayed in red for any worksheet whose utilization exceeds 100%.

Power Rail Current Consumption

Most worksheets include a table showing the dynamic current consumption (and standby current consumption, if applicable) for all power rails used by the FPGA resources in the specific worksheet. The same power rail may appear in multiple worksheets, and the total dynamic and standby current in the **Report** worksheet is the sum of all corresponding currents for a given rail at a given voltage in individual worksheets. The **Report** worksheet also includes static currents, which are not reported in individual worksheets.

Errors and Warnings

Error and warning fields are used to display error and warning messages alerting users to issues with the information entered into this or another related worksheet. If there are error messages in the current worksheet, the thermal power value displayed in the **Main** and **Report** worksheets corresponding to the current worksheet will be highlighted in red to indicate an error message. For accurate power estimates, all error messages should be resolved.

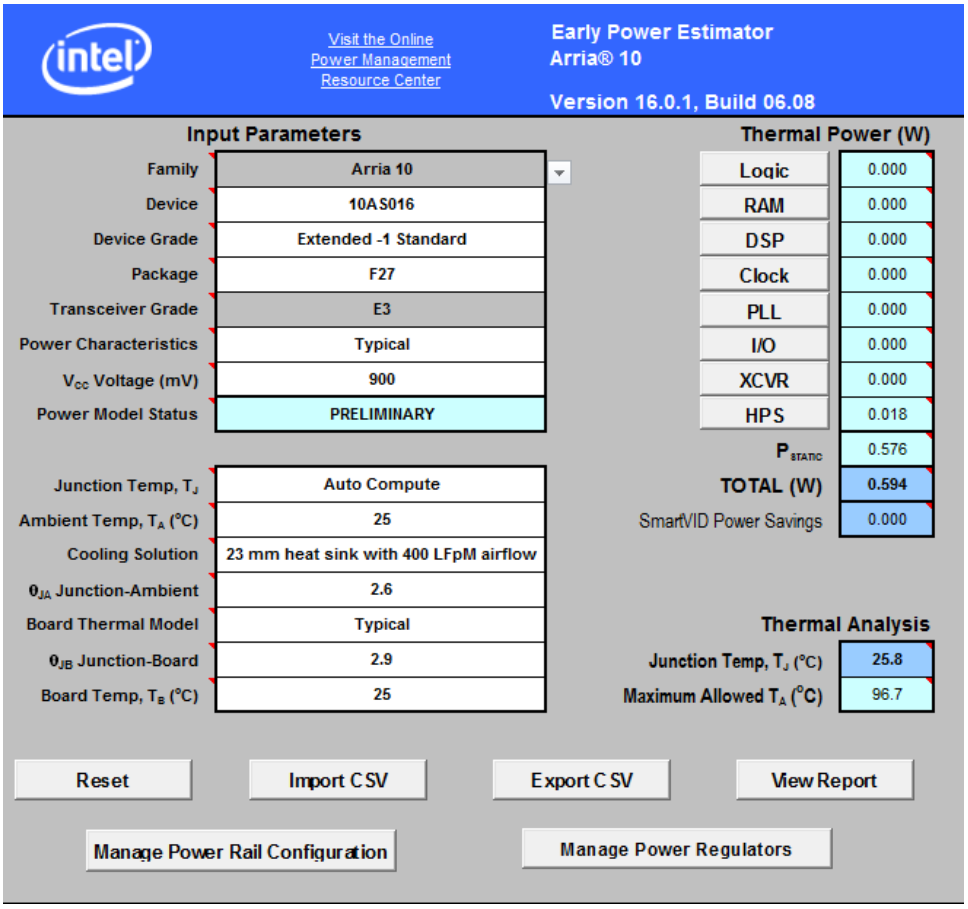
Related Information

- Arria 10 EPE - Main Worksheet on page 17
- Arria 10 EPE - Report Worksheet on page 46

4.2. Arria 10 EPE - Main Worksheet

The Main worksheet of the Early Power Estimator (EPE) for Arria 10 allows you to enter device, package, and cooling information, and displays thermal power and thermal analysis information.

Figure 7. Arria 10 EPE Main Worksheet



The required parameters depend on whether the junction temperature is manually entered or auto computed.

Table 3. Input Parameter Information

Parameter	Description
Family	Select the device family.
Device	Select your device. Larger devices consume more static power and have higher clock dynamic power. All other power components are unaffected by device selection.
Device Grade	Select the combination of Operating Temperature, Speed Grade, and Power Option used. • Operating Temperature: Extended (T_J = 0C to 100C), Industrial (T_J = -40C to 100C) • FPGA Core Fabric Speed Grade: 1 (fastest), 2 or 3. • Power Option: S (Standard), L (Low), or V (SmartVID)
Package	Select the device package. Larger packages provide a larger cooling surface and more contact points to the circuit board, thus they offer lower thermal resistance. Package selection does not affect dynamic power directly.

continued...

Parameter	Description
Transceiver Grade	Select the transceiver grade. *Note:* For information on transceiver grades, refer to *Arria 10 Device Variants and Packages*, in the *Arria 10 Device Overview*.
Power Characteristics	Select typical or theoretical worst-case silicon process. There is a process variation from die-to-die. This variation primarily affects static power consumption. If you choose **Typical** power characteristics, estimates are based on average power consumed by typical silicon. For FPGA board power supply design, choose **Maximum** for worst-case values. To enable the Enpirion device selection, you must set the Power Characteristics to **Maximum**.
V_{CC} Voltage (mV)	Select the voltage of the V_{CC} power rail, in mV.
Power Model Status	Indicates whether the power model for the device is in preliminary or final status. Assuming accurate inputs to the Early Power Estimator, the margins for calculated current values are as described below: • Effective with version 18.0.1, the recommended margin on Vcc is 20% or less for most designs (see the Report tab for the exact value for your design). • Recommended margin for transceiver rails (V_{cch_gxb}, V_{cct_gxb}, V_{ccr_gxb}) is 15% • Recommended margin for V_{cceram} is 5% • Recommended margin for all other rails is 25%
Junction Temp, T_J	Select whether Junction Temperature (T_J) should be computed automatically or provided by the user.
Ambient Temp, T_A (°C)/Junction Temp, T_J (°C)	Enter the temperature of the air that is cooling the device. This value can range from **–40°C** to **125°C**, depending on the device grade selected. If you turn on the **Auto Compute** junction temperature option, you can enter the ambient temperature in this field; otherwise, enter the actual junction temperature.
Cooling Solution	Select your cooling solution with associated airflow. (This field is not available when you enter the junction temperature directly.) Representative examples of heat sinks and airflows are provided; larger heat sinks provide lower thermal resistance, and thus lower junction temperature. If the heat sink and airflow is known, consult the data sheet, choose **Custom**, and in the **θ_{JA} Junction-Ambient** field, enter a junction to ambient value according to your system.
θ_{JA} Junction-Ambient	If you have specified a custom cooling solution, enter the Junction-Ambient value in °C/W. This value is used to compute the final junction temperature if you have selected **Auto Compute** (This field is not available when you enter the junction temperature directly.)
Board Thermal Model	This field is not applicable when no heat sink is used, or when you enter the junction temperature directly. Select the type of board model to be used in thermal analysis. Available values are: • **None (Conservative)**. If you select this model, the system assumes that no heat is dissipated through the board. This results in a pessimistic calculated junction temperature. • **Typical**. If you select this model, the system assumes the characteristics of a typical customer board stack, which is based on the selected device and package. • **Custom**. If you select this model, you must enter an appropriate value for θ_{JB} Junction-Board, in the field below.

continued...

Parameter	Description
	You should perform a detailed thermal simulation of your system to determine the final junction temperature. This two-resistor thermal model is for early estimation only.
θ_{JB} Junction-Board	If you specify a custom Board Thermal Model, enter the **θ_{JB} Junction-Board** value (in °C/W), in this field. (This field is not applicable when no heat sink is used, or when you enter the junction temperature directly.)
Board Temp, T_B (°C)	If you specified a custom or typical Board Thermal Model, enter the board temperature to be used in thermal calculations (in °C). (This field is not applicable when no heat sink is used, or when you enter the junction temperature directly.)

Thermal power is the power dissipated in the device. Total thermal power is the sum of the thermal power of all the resources used in the device, including the static, standby, and dynamic power. Total thermal power includes only the thermal component for the I/O worksheet and does not include external power dissipation, such as from voltage-referenced termination resistors.

The static power (P_{STATIC}) is the thermal power dissipated on the chip, independent of design activity. P_{STATIC} includes the static power from all FPGA functional blocks, except for I/O DC bias power and transceiver DC bias power, which are included in the standby power of the I/O and XCVR worksheets, respectively. P_{STATIC} is the only thermal power component that varies with junction temperature and power characteristics (process). P_{STATIC} is also the only thermal power component that varies significantly with selected device.

Table 4. Thermal Power (W) Information

Column Heading	Description
Logic	Displays the dynamic power consumed by adaptive logic modules (ALMs), flipflops (FFs) and associated routing. Click **Logic** to see details.
RAM	Displays the dynamic power consumed by RAMs and associated routing. Click **RAM** to see details.
DSP	Displays the dynamic power consumed by digital signal processing (DSP) blocks and associated routing. Click **DSP** to see details.
Clock	Displays the dynamic power consumed by clock networks. The clock dynamic power is affected by the selected device. Click **Clock** to see details.
PLL	Displays the dynamic power consumed by phase-locked loops (PLLs). Click **PLL** to see details.
I/O	Displays the thermal power consumed by I/O pins and I/O subsystems. Click **I/O** to see details.
XCVR	Displays the total power consumed by transceiver blocks. Click **XCVR** to see details.
HPS	Displays the total power consumed by the hard processor system (HPS). Click **HPS** to see details.
P_{static}	Displays the static power consumed regardless of clock frequency. This includes static power consumed by I/O and transceiver blocks, but does not include standby power. P_{static} is affected by junction temperature, selected device, power characteristics, and M20K, DSP and high speed LAB usage.

continued...

Column Heading	Description
	Note: For information on measuring the static power consumption of a specific device, refer to the appendix *Measuring Static Power*.
TOTAL (W)	Displays the total power dissipated as heat from the FPGA. This value includes power savings due to SmartVID. This value does not include power dissipated in off-chip termination resistors. Total power dissipation in the FPGA may differ from the sum of power on all rails due to several factors including, but not limited to, the power dissipated in off-chip termination resistors. Refer to the Report worksheet for power supply currents drawn from the FPGA supply rails.
SmartVID Power Savings	Displays the total power reduction (static and dynamic) resulting from the lower voltage that is made possible by SmartVID. This power reduction is dependent on the user design and device characteristics. The combination of these factors may result in different static and dynamic power savings, so the exact dynamic and static components are not identified separately, and the power reduction reported here is a worst-case result. This field is applicable only to devices that support the SmartVID feature, and only if the SmartVoltage ID setting is set to On. The **SmartVID Power Savings** value is provided for informational purposes only; the savings due to SmartVID are already included in the **TOTAL (W)** value.

Note: If any thermal power value is highlighted in red, it indicates an error in the design specification. Review the relevant worksheet for errors or utilization values exceeding 100%. Correct any errors to obtain reliable power and temperature estimates.

The Thermal Analysis section displays the junction temperature (T_J) and the maximum allowed ambient temperature (T_A) values.

Table 5. Thermal Analysis Information

Column Heading	Description
Junction Temp, T_J (°C)	If you specified a value for Junction Temp (T_J), the value in this field is equal to the value that you specified. If you specified Auto Compute for Junction Temp (T_J), this field displays the estimated device junction temperature based on the thermal parameters provided. The junction temperature is determined by dissipating the total thermal power through the top of the chip and through the board.
Maximum Allowed T_A (°C) / Maximum Allowed T_J (C)	If you specified a value for Junction Temp (T_J), the value in this field is the maximum allowable device junction temperature (in °C), based on the specified device grade. If you specified Auto Compute for Junction Temp (T_J), this field provides a guideline for the maximum ambient temperature (in °C) to which the device can be subjected, without exceeding the maximum allowable junction temperature, based on the specified cooling solution and device grade.

You can directly enter or automatically compute the junction temperature based on the information provided. To enter the junction temperature, select **User Entered** in the **Junction Temp** field in the **Input Parameters** section. To automatically compute the junction temperature, select **Auto Compute** in the same field.

When automatically computing the junction temperature, the ambient temperature, cooling solution, board thermal model, and board temperature of the device determine the junction temperature in °C. Junction temperature is the estimated operating junction temperature based on your device and thermal conditions.

You can consider the device as a heat source and the junction temperature is the temperature of the device. While the temperature typically varies across the device, to simplify the analysis, you can assume that the temperature of the device is constant regardless of where it is measured.

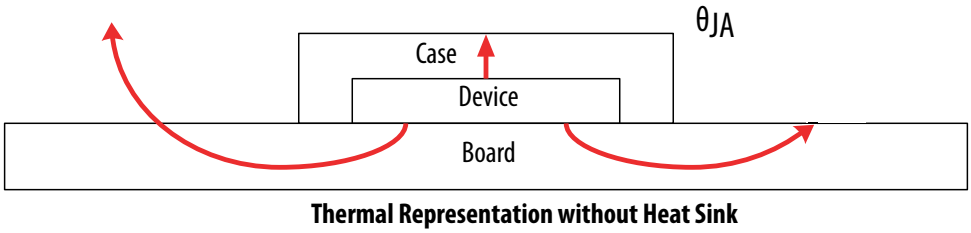
Power from the device can be dissipated through different paths. Different paths become significant depending on the thermal properties of the system. The significance of power dissipation paths vary depending on whether or not a heat sink is used for the device.

Not Using a Heatsink

When you do not use a heat sink, the major paths of power dissipation are from the device to the air. You can refer to this as a junction-to-ambient thermal resistance. In this case, there are two significant junction-to-ambient thermal resistance paths:

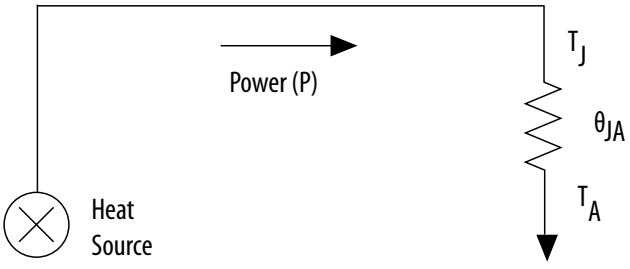
- From the device through the case to the air
- From the device to the board

Figure 8. Thermal Representation without a Heat Sink



In the model used in the EPE spreadsheet, power is dissipated through the case and board. The θ_{JA} values are calculated for differing air flow options accounting for the paths through the case and through the board.

Figure 9. Thermal Model in the EPE Spreadsheet without a Heat Sink



The ambient temperature does not change, but the junction temperature changes depending on the thermal properties and total power dissipation, which in turn is affected by junction temperature. The junction temperature calculation is an iterative process.

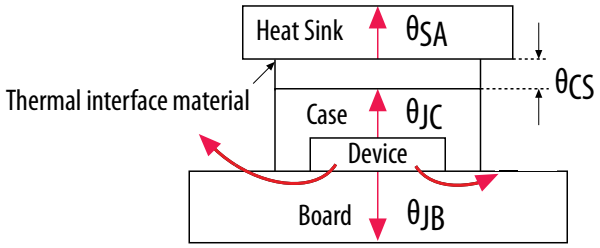
The following equation shows the total power calculated based on the total θ_{JA} value, ambient, and junction temperatures.

$$P = \frac{T_J - T_A}{\theta_{JA}}$$

Using a Heat Sink

When you use a heat sink, the major paths of power dissipation are from the device through the case, thermal interface material, and heat sink. There is also a path of power dissipation through the board. The path through the board has less impact than the path to air.

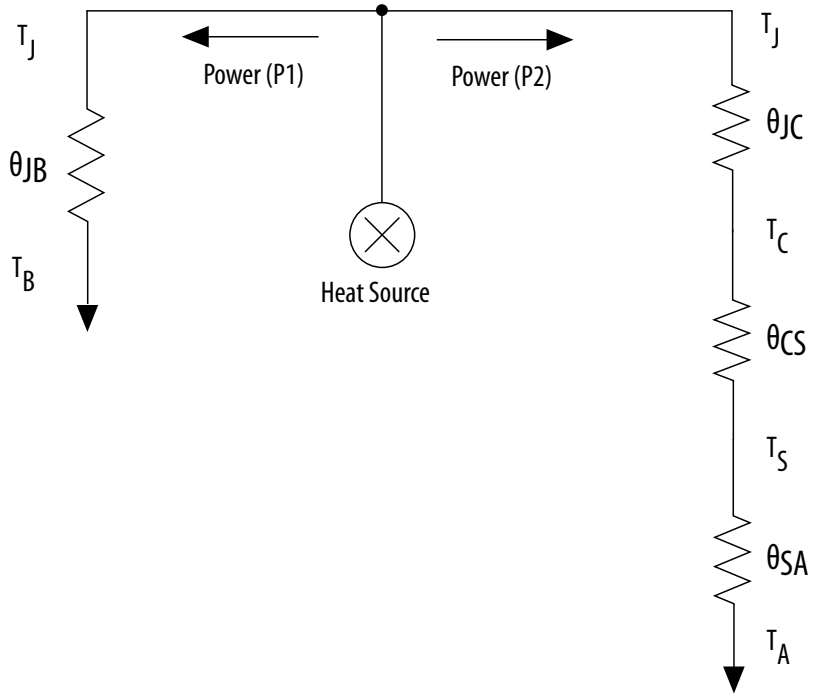
Figure 10. Thermal Representation with a Heat Sink



Thermal Representation with Heat Sink

In the model used in the EPE spreadsheet, power is dissipated through the board and through the case and heat sink. The junction-to-board thermal resistance (θ_{JB}) refers to the thermal resistance of the path through the board. Junction-to-ambient thermal resistance (θ_{JA}) refers to the thermal resistance of the path through the case, thermal interface material, and heat sink.

Figure 11. Thermal Model for the EPE Spreadsheet with a Heat Sink



If you want the EPE spreadsheet thermal model to take the θ_{JB} into consideration, set the Board Thermal Model parameter to either **Typical** or **Custom**. Otherwise, set the Board Thermal Model parameter to **None (conservative)**. In this case, the path through the board is not considered for power dissipation and a more conservative thermal power estimate is obtained.

The addition of the junction-to-case thermal resistance (θ_{JC}), the case-to-heat sink thermal resistance (θ_{CS}) and the heat sink-to-ambient thermal resistance (θ_{SA}) determines the θ_{JA}, as shown by the following equation.

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

Based on the device, package, airflow, and heat sink solution selected in the Input Parameters section, the EPE spreadsheet determines the θ_{JA}.

If you use a low, medium, or high profile heat sink, select the airflow from the values of **Still Air** and air flow rates of **100 lfm (0.5 m/s)**, **200 lfm (1.0 m/s)**, and **400 lfm (2.0 m/s)**. If you use a custom cooling solution, enter the custom θ_{JA} value. You must incorporate the airflow and junction to case resistance into the custom θ_{JA} value. You can obtain these values from the heat sink manufacturer.

The ambient temperature does not change, but the junction temperature changes depending on the thermal properties. Calculating the junction temperature is an iterative process because a change in junction temperature affects the thermal device properties, due to a change in power dissipation. Those thermal device properties are used to calculate junction temperature.

The total power is calculated based on the θ_{JA} and θ_{JB}values, and ambient board and junction temperatures with the following equation.

$$P = \frac{T_J - T_A}{\theta_{JA}} + \frac{T_J - T_B}{\theta_{JB}}$$

Table 6. Control Button Descriptions

Button Name	Description
Logic	Opens the Logic worksheet to display details of the dynamic power consumed by adaptive logic modules (ALMs), flipflops, and associated routing.
RAM	Opens the RAM worksheet to display details of the dynamic power consumed by RAMs and associated routing.
DSP	Opens the DSP worksheet to display details of the dynamic power consumed by digital signal processing blocks and associated routing.
Clock	Opens the Clock worksheet to display details of the dynamic power consumed by clock networks and associated routing.
PLL	Opens the PLL worksheet to display details of the dynamic power consumed by phase-locked loops and associated routing.
I/O	Opens the I/O worksheet to display details of the thermal power consumed by I/O pins and I/O subsystems.
XCVR	Opens the XCVR worksheet to display details of the total power consumed by transceiver blocks.
HPS	Opens the HPS worksheet to display details of the total power consumed by the hard processor system (HPS).
Reset	Resets the Early Power Estimator to default values; any parameters that you have specified are lost.
Import CSV	Allows you to import parameters from a comma-separated value file.
Export CSV	Allows you to export parameters to a comma-separated value file.
View Report	Displays the Report worksheet.
Manage Power Rail Configuration	Displays the Power Rail Configuration table, on the Report worksheet.
Manage Power Regulators	Displays the Regulator Selection table, on the Enpirion worksheet.

Related Information

- Arria 10 Device Variants and Packages
- Early Power Estimator for Intel Arria 10 Graphical User Interface on page 11
- Arria 10 EPE - Common Worksheet Elements on page 16

4.3. Arria 10 EPE - Logic Worksheet

The Logic worksheet of the Early Power Estimator (EPE) for Arria 10 allows you to enter logic resources for all modules in your design.

Figure 12. Logic Worksheet of the Early Power Estimator

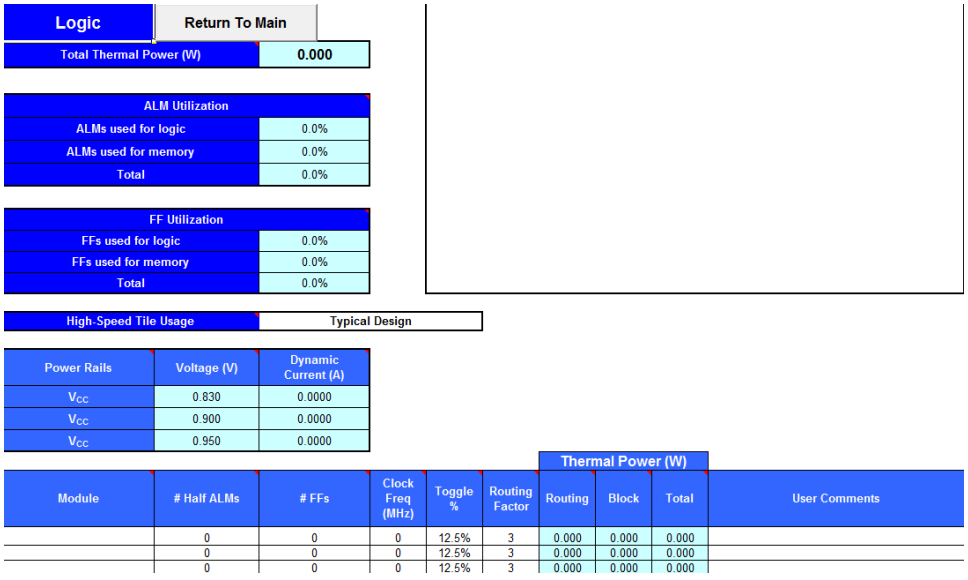


Table 7. General Settings in the Logic Worksheet

Input Parameter	Description
High-Speed Tile Usage	Select the High-Speed Tile Usage setting. This value can be Typical Design, Typical High-Performance Design, or Atypical High-Performance Design. • Typical Design represents a design with 10% or more timing margin. • Typical High-Performance Design represents an average design with no timing margin. These designs have a few near-critical timing paths. • Atypical High-Performance Design represents a 90th percentile design with no timing margin. These designs have many near-critical timing paths. This setting affects static power consumption (P_{STATIC}) found in the Main worksheet of the EPE spreadsheet. It also has a small impact on the dynamic power consumed by the logic resources entered in the Logic worksheet of the EPE spreadsheet. *Note:* When you import a design from the Intel Quartus Prime software, the Early Power Estimator imports a precise value for high-speed tile usage, and the value of this setting changes to **Imported.**

Table 8. Logic Worksheet Information

Input Parameter	Description
Module	Specify a name for each module of the design. This is an optional entry.
#Half ALMs	Enter twice the number of Adaptive Logic Modules (ALMs) used in your design.
# FFs	Enter the number of flipflops in the module.

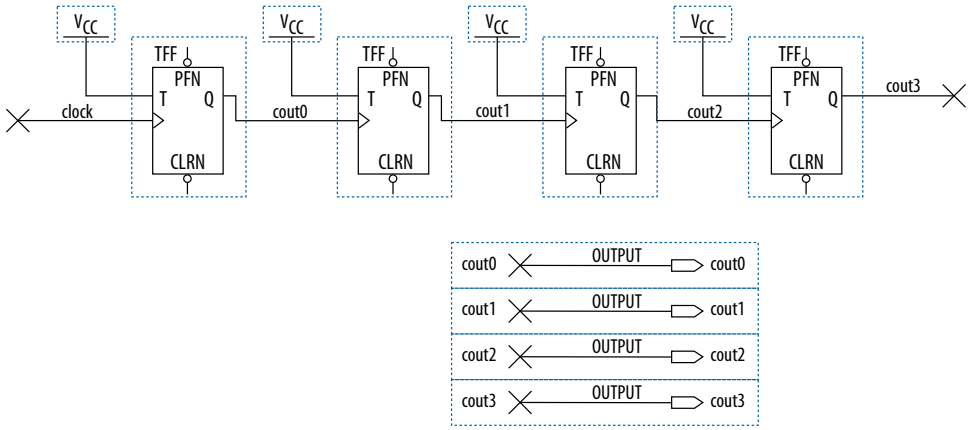
continued...

Input Parameter	Description
	Clock routing power associated with flipflops is calculated separately on the Clock worksheet of the EPE spreadsheet.
Clock Freq (MHz)	Enter a clock frequency (in MHz). This value is limited by the maximum frequency specification for the device family. *Note:* When you import a design from the Intel Quartus Prime software, some imported half ALMs and flipflops may have a clock frequency of 0 MHz; this can occur for one of two reasons: • The Intel Quartus Prime software did not have sufficient information to determine clock frequency due to incomplete clock constraints. • The Intel Quartus Prime software exported a comma-separated value (`.csv`) file containing half ALMs where only flipflops are used. Such ALMs are imported as ALMs with clock frequency of 0 MHz, while their flipflops are imported into a separate row with the correct clock frequency.
Toggle %	Enter the average percentage of clock cycles when the block output signals change values. Toggle percentage is multiplied by clock frequency to determine the number of transitions per second. For example, 100 MHz frequency with a 12.5% toggle rate, means that each LUT or flipflop output toggles 12.5 million times per second (100MHz × 12.5%). The toggle percentage ranges from 0 to 100%. Typically, the toggle percentage is 12.5%, which is the toggle percentage of a 16-bit counter. Most logic only toggles infrequently; therefore, toggle rates of less than 50% are more realistic. To ensure you do not underestimate the toggle percentage, use a realistic toggle percentage obtained through simulation. For example, a T flipflop (TFF) with its input tied to VCC has a toggle rate of 100% because its output is changing logic state on every clock cycle. Refer to the 4-Bit Counter Example below for a more detailed analysis. For any rows containing flip-flops, toggle percentage cannot exceed 100%. A small portion of ALMs in a design may experience glitching that results in toggle percentage exceeding 100% for such ALMs. Enter such ALMs into a separate row with # FFs set to 0.
Routing Factor	Indicates the extent of the routing power of the outputs. Characteristics that have a large power impact and are captured by this factor include the following: • the fanout of the outputs • the number of routing resources used • the relative power usage of the different types of routing resources used The default value for this field is typical; the actual value varies between blocks in your design, and depends on the placement of your design. For most accurate results, you should import this value from the Intel Quartus Prime software, because the Intel Quartus Prime software has access to detailed placement information. In the absence of a Intel Quartus Prime design, higher values generally correspond to signals that span large distances on the FPGA and fanout to many destinations, while lower values correspond to more localized signals. You can change this field from its default value to explore possible variations in power consumption depending on block placement. When changing this value, keep in mind that typical designs rarely use extreme values, and only for a small subset of the design.

continued...

Input Parameter	Description
Thermal Power (W) - Routing	Indicates the power dissipation due to estimated routing (in W). Routing power depends on placement and routing, which is a function of design complexity. The values shown are representative of routing power based on observed behavior across more than 100 real-world designs. Use the Intel Quartus Prime Power Analyzer for accurate analysis based on the exact routing used in your design.
Thermal Power (W) - Block	Indicates the power dissipation due to internal toggling of the ALMs (in W). Logic block power is a combination of the function implemented and the relative toggle rates of the various inputs. The EPE spreadsheet uses an estimate based on observed behavior across more than 100 real-world designs. Use the Intel Quartus Prime Power Analyzer for accurate analysis based on the exact synthesis of your design.
Thermal Power (W) - Total	Indicates the estimated power (in W), based on information entered into the EPE spreadsheet. It is equal to the sum of routing power and block power.
User Comments	Enter any comments. This is an optional entry.

Figure 13. 4-Bit Counter Example



The `cout0` output of the first TFF has a toggle percentage of 100% because the signal toggles on every clock cycle. The toggle percentage for the `cout1` output of the second TFF is 50% because the output toggles every two clock cycles. Similarly, the toggle percentage for the `cout2` and `cout3` outputs are 25% and 12.5%, respectively. Therefore, the average toggle percentage for this 4-bit counter is (100 + 50 + 25 + 12.5)/4 = 46.875%.

For more information about logic block configurations, refer to the *Logic Array Blocks and Adaptive Logic Modules* chapter of the Arria 10 Device Handbook.

Related Information

- Logic Array Blocks and Adaptive Logic Modules in Arria 10 Devices
- Early Power Estimator for Intel Arria 10 Graphical User Interface on page 11

- Arria 10 EPE - Common Worksheet Elements on page 16

4.4. Arria 10 EPE - RAM Worksheet

Each row in the RAM worksheet of the Early Power Estimator (EPE) for Arria 10 represents a design module with RAM blocks of the same type, same data width, same RAM depth (if applicable), same RAM mode, and the same port parameters.

Each row in the RAM worksheet of the EPE spreadsheet represents a logical RAM module that can be implemented using one or more physical RAM blocks. The EPE spreadsheet implements each logical RAM module with the minimum number of physical RAM blocks, in the most power-efficient way possible, based on the specified logical width and depth.

You must know how your RAM is implemented by the Quartus Prime Compiler when you are selecting the RAM block mode. For example, if a ROM is implemented with two ports, it is considered a true dual-port memory and not a ROM. Single-port and ROM implementations use only one port. Simple dual-port and true dual-port implementations use both Port A and Port B.

Note:

- The Early Power Estimator reports MLAB power in the RAM worksheet. However the Power Analyzer reports MLAB power as Combinational cell and Register cell block type in the *Thermal Power Dissipation by Block Type* section of the power report.
- The Power Analyzer reports LAB clock power as *Block Thermal Dynamic Power* under *Clock Network* block type in the *Thermal Power Dissipation by Block Type* section of the power report. The Early Power Estimator reports LAB clock power in either the Clock or RAM worksheet, depending on whether the LAB is used to implement logic or used as MLAB, respectively.

Figure 14. RAM Worksheet of the Early Power Estimator

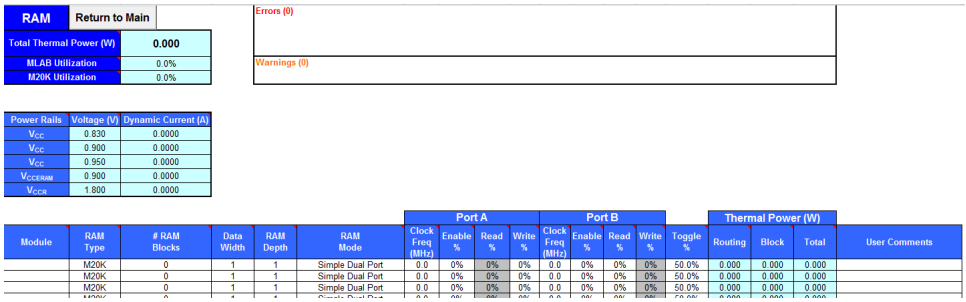


Table 9. RAM Worksheet Information

Column Heading	Description
Module	Enter a name for the RAM module in this row. This is an optional value.
RAM Type	Select the implemented RAM type.

continued...

Column Heading	Description
	You can find the RAM type in the *Type* column of the Quartus Prime Compilation Report. In the Compilation Report, select **Fitter** and click **Resource Section**. Click **Fitter RAM Summary**.
# RAM Blocks	Enter the number of RAM blocks in the module that use the same type and mode and have the same parameter for each port. The parameters for each port are as follows: • Clock frequency in MHz • Percentage of time the RAM is enabled • Percentage of time the port is writing as opposed to reading You can find the number of RAM blocks in either the *MLAB cells* or *M20K blocks* column of the Quartus Prime Compilation Report. In the Compilation Report, select **Fitter** and click **Resource Section**. Click **Fitter RAM Summary**.
Data Width	Enter the width of the data for the RAM block. This value is limited based on the RAM type. You can find the width of the RAM block in the *Port A Width* or the *Port B Width* column of the Quartus Prime Compilation Report. In the Compilation Report, select **Fitter** and click **Resource Section**. Click **Fitter RAM Summary**. For RAM blocks that have different widths for Port A and Port B, use the larger of the two widths.
RAM Depth	Enter the depth of the RAM block in number of words. You can find the depth of the RAM block in the *Port A Depth* or the *Port B Depth* column of the Quartus Prime Compilation Report. In the Compilation Report, select **Fitter** and click **Resource Section**. Click**Fitter RAM Summary**.
RAM Mode	Select from the following modes: • Single Port • Simple Dual Port • True Dual Port • Simple Dual Port with ECC • ROM The mode is based on how the Quartus Prime Compiler implements the RAM. If you are unsure how your memory module is implemented, Intel recommends compiling a test case in the required configuration in the Quartus Prime software. You can find the RAM mode in the *Mode* column of the Quartus Prime Compilation Report. In the Compilation Report, select **Fitter** and click **Resource Section**. Click **Fitter RAM Summary**. A single-port RAM has one port with a read and a write control signal. A simple dual-port RAM has one read port and one write port. A true dual-port RAM has two ports, each with a read and a write control signal. ROMs are read-only single-port RAMs.
Port A - Clock Freq (MHz)	Enter the clock frequency for Port A of the RAM blocks (in MHz). This value is limited by the maximum frequency specification for the RAM type and device family.
Port A - Enable %	The average percentage of time the Port A clock enable is active, regardless of activity on RAM data and address inputs. This number must be a percentage between 0% and 100%. RAM power is primarily consumed when a clock event occurs. Using a clock enable signal to disable a port when no read or write operation is occurring can result in significant power savings.

continued...

Column Heading	Description
Port A - Read %	Enter the percentage of time Port A of the RAM block is in read mode. This field is applicable only for single port and true dual port RAMs. This value must be a percentage number between 0 and 100%.
Port A - Write %	Enter the average percentage of time Port A of the RAM block is in write mode. This field is applicable only for single port, dual port and true dual port RAMs. This value must be a percentage number between 0 and 100%.
Port B - Clock Freq (MHz)	Enter the clock frequency for Port B of the RAM blocks (in MHz).
Port B - Enable %	Enter the average percentage of time the input clock enable for Port B is active, regardless of the activity on the RAM data and address inputs. The enable percentage ranges from 0 to 100%. RAM power is primarily consumed when a clock event occurs. Using a clock-enable signal to disable a port when no read or write operation is occurring can result in significant power savings.
Port B - Read %	Enter the percentage of time Port B of the RAM block is in read mode. This field is applicable only to dual port and true dual port RAMs and ROMs. This value must be a percentage number between 0 and 100%.
Port B - Write %	Enter the percentage of time Port B of the RAM block is in write mode. This field is only available for true dual-port mode. This value must be a percentage number between 0 and 100%.
Toggle %	The percentage of clock cycles when the block output signal changes value. This value is multiplied by the clock frequency and the enable percentage to determine the number of transitions per second. This value affects only routing power. 50% corresponds to a randomly changing signal, since half the time the signal will hold the same value and thus not transition. This is considered the highest meaningful toggle rate for a RAM block.
Thermal Power (W) - Routing	Indicates the power dissipation due to estimated routing (in W). Routing power depends on placement and routing, which is a function of design complexity. The values shown represent the routing power estimate based on observed behavior across more than 100 real-world designs. Use the Quartus Prime Power Analyzer for accurate analysis based on the exact routing used in your design.
Thermal Power (W) - Block	Indicates the power dissipation due to internal toggling of the RAM (in W). Use the Quartus Prime Power Analyzer for accurate analysis based on the exact RAM modes in your design.
Thermal Power (W) - Total	Indicates the estimated power (in W), based on information entered into the EPE spreadsheet. Total power is equal to the sum of routing power and block power.
User Comments	Enter any comments. This is an optional entry.

Related Information

- Embedded Memory Blocks in Arria 10 Devices
- Early Power Estimator for Intel Arria 10 Graphical User Interface on page 11
- Arria 10 EPE - Common Worksheet Elements on page 16

4.5. Arria 10 EPE - DSP Worksheet

Each row in the DSP worksheet of the Early Power Estimator (EPE) for Arria 10 represents a DSP design module where all instances have the same configuration, clock frequency, toggle percentage, and register usage.

Figure 15. DSP Worksheet of the Early Power Estimator

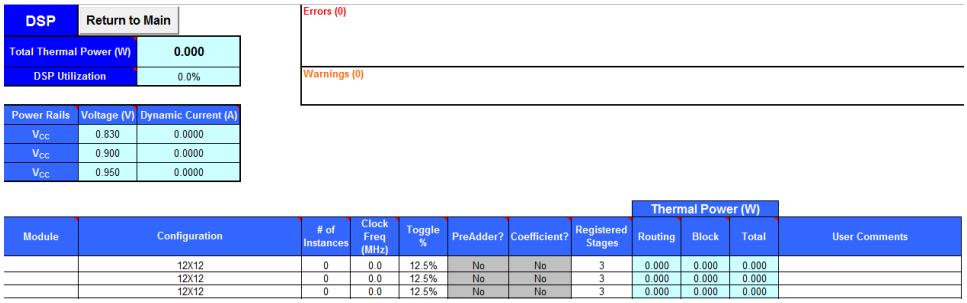


Table 10. DSP Worksheet Information

Column Heading	Description
Module	Enter a name for the DSP module in this column. This is an optional value.
Configuration	Select the DSP block configuration for the module.
# of Instances	Enter the number of DSP block instances that have the same configuration, clock frequency, toggle percentage, and register usage. This value is not necessarily equal to the number of dedicated DSP blocks you use. For example, it is possible to use two 18 × 18 simple multipliers that are implemented in the same DSP block in the FPGA devices. In this case, the number of instances would be two. To determine the maximum number of instances you can fit in the device for any particular mode, follow these steps: 1. Open the *Variable Precision DSP Blocks* chapter of the Arria 10 Device Handbook. 2. In the *Number of DSP Blocks* table, take the maximum number of DSP blocks available in the device for the mode of operation. 3. Divide the maximum number by the *# of Mults* for that mode of operation from the *DSP Block Operation Modes* table. The resulting value is the maximum number of instances supported by the device.
Clock Freq (MHz)	Enter the clock frequency for the module (in MHz). This value is limited by the maximum frequency specification for the device family.
Toggle %	Enter the average percentage of DSP data outputs toggling on each clock cycle. The toggle percentage ranges from 0 to 50%. The default value is 12.5%. For a more conservative power estimate, use a higher toggle percentage.

continued...

Column Heading	Description
	50% corresponds to a randomly changing signal, since half the time the signal will hold the same value and thus not transition. This is considered the highest meaningful toggle rate for a DSP block.
Preadder?	Select **Yes** if the PreAdder function of the DSP block is turned on.
Coefficient?	Select **Yes** if the Coefficient function of the DSP block is turned on.
Registered Stages	Select number of the registered stages. Having more stages registered increases DSP f_{MAX} and reduces power consumption at the cost of increased latency. • 0—None • 1—Input • 2—Input and Output • 3—Input, Output, and Multiplier • 4—Input, Output, Multiplier, and Floating-Point Adder
Thermal Power (W)–Routing	Indicates the power dissipation due to estimated routing (in W). Routing power depends on placement and routing, which is a function of design complexity. The values shown represent the routing power estimate based on observed behavior across more than 100 real-world designs.
Thermal Power (W)–Block	Indicates the estimated power consumed by the DSP blocks (in W).
Thermal Power (W)–Total	Indicates the estimated power (in W), based on information entered into the EPE spreadsheet. It is the total power consumed by the DSP blocks and is equal to the routing power and block power.
User Comments	Enter any comments. This is an optional entry.

Related Information

- Early Power Estimator for Intel Arria 10 Graphical User Interface on page 11
- Arria 10 EPE - Common Worksheet Elements on page 16

4.6. Arria 10 EPE - Clock Worksheet

Each row in the Clock worksheet of the Early Power Estimator (EPE) for Arria 10 represents a clock network or a separate clock domain.

Arria 10 devices support global, regional, and periphery clock networks. The EPE spreadsheet does not distinguish between global or regional clocks because the difference in power is not significant.

Figure 16. Clock Worksheet of the Early Power Estimator

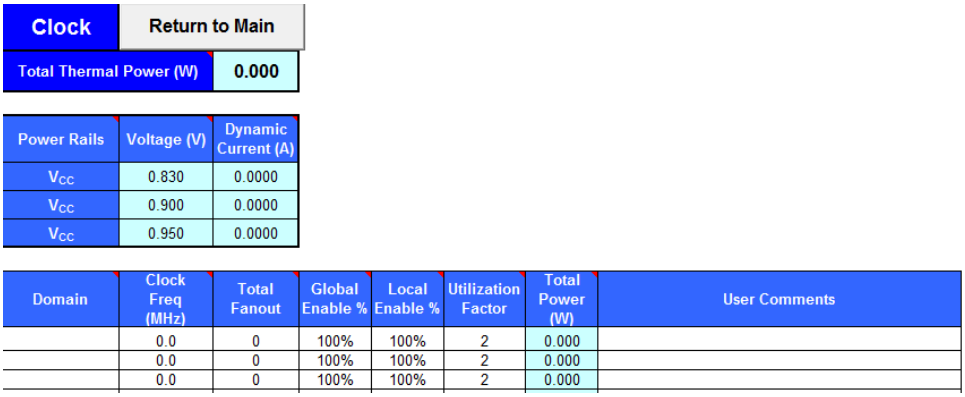


Table 11. Clock Worksheet Information

Column Heading	Description
Domain	Specify a name for the clock domain in this row. This is an optional value.
Clock Freq (MHz)	Enter the frequency of the clock domain. This value is limited by the maximum frequency specification for the device family. *Note:* When you import a design from the Quartus Prime software, some imported clocks may have a frequency of 0 MHz, due to either of the following reasons: • The Quartus Prime software did not have sufficient information to determine clock frequency due to incomplete clock constraints. • Clock resources were used to route a reset signal, which toggles infrequently, so its frequency is reported as 0 MHz.
Total Fanout	Enter the total number of flipflops, RAMs, digital signal processing (DSP) blocks, and I/O pins fed by this clock. Power consumed by MLAB clocks is accounted for in the RAM worksheet; therefore, clock fanout on this worksheet does not include any MLABs driven by this clock domain. The number of resources driven by every global clock and regional clock signal is reported in the *Fan-out* column of the Quartus Prime Compilation Report. In the Compilation Report, select **Fitter** and click **Resources Section**. Select **Global & Other Fast Signals Summary** and observe the *Fan-out* value.
Global Enable %	Enter the average percentage of time that the entire clock tree is enabled. Each global clock buffer has an enable signal that you can use to dynamically shut down the entire clock tree.
Local Enable %	Enter the average percentage of time that clock enable is high for destination flipflops. Local clock enables for flipflops in ALMs are promoted to LAB-wide signals. When a given flipflop is disabled, the LAB-wide clock is disabled, cutting clock power and the power for down-stream logic. This worksheet models only the impact on clock tree power.
Utilization Factor	Represents the impact of the clock network configuration on power.

continued...

Column Heading	Description
	Characteristics that have a large impact on power and are captured by this factor include the following: • whether the network is widely spread out • whether the fanout is small or large • the clock settings within each LAB The default value for this field is typical; the actual value varies between clocks in your design, and depends on the placement of your design. For most accurate results, you should import this value from the Quartus Prime software, because the Quartus Prime software has access to detailed placement information. In the absence of a Quartus Prime design, higher values generally correspond to signals that span large distances on the FPGA and fanout to many destinations, while lower values correspond to more localized signals. You can change this field from its default value to explore possible variations in power consumption depending on block placement. When changing this value, keep in mind that typical designs rarely use extreme values, and only for a small subset of the design.
Total Power (W)	Indicates the total power dissipation due to clock distribution (in W).
User Comments	Enter any comments. This is an optional entry.

Note: The Power Analyzer reports LAB clock power as *Block Thermal Dynamic Power* under *Clock Network* block type in the *Thermal Power Dissipation by Block Type* section of the power report. The Early Power Estimator reports LAB clock power in either the Clock or RAM worksheet, depending on whether the LAB is used to implement logic or used as MLAB, respectively.

For more information about the clock networks of Arria 10 devices, refer to the *Clock Networks and PLLs* chapter of the *Arria 10 Device Handbook*.

Related Information

- Clock Networks and PLLs in Arria 10 Devices
- Early Power Estimator for Intel Arria 10 Graphical User Interface on page 11
- Arria 10 EPE - Common Worksheet Elements on page 16

4.7. Arria 10 EPE - PLL Worksheet

Each row in the PLL worksheet of the Early Power Estimator (EPE) for Arria 10 represents one or more PLLs in the device.

For Arria 10 devices, the supported PLL types are IOPLL, fPLL, ATX PLL, and CMU PLL.

Figure 17. PLL Worksheet of the Early Power Estimator

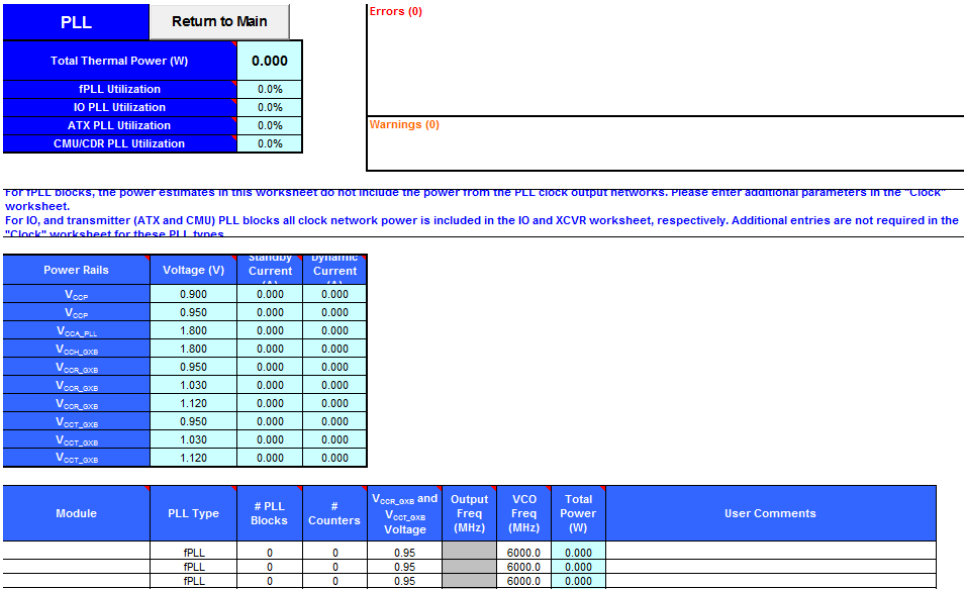


Table 12. PLL Worksheet Information

Column Heading	Description
Module	Specify a name for the PLL in this column. This is an optional value.
PLL Type	Select whether the PLL is an IOPLL, fPLL, ATX PLL, or CMU PLL.
# PLL Blocks	Enter the number of PLL blocks with the same combination of parameters.
# Counters	Enter the number of counters of the PLL. For fPLL, this includes C counter, L counter, and feedback. This field is not applicable for ATX PLLs and CMU PLLs.
V_{CCR_GXB} and V_{CCT_GXB} Voltage	Specify the voltage of the V_{CCR_GXB} and V_{CCT_GXB} rails. This field is not applicable for I/O PLLs.
Output Freq (MHz)	Specify the output frequency for CMU and ATX PLLs.
VCO Freq (MHz)	Specify the internal VCO operating frequency for fPLLs and I/O PLLs. When using an fPLL as a transmitter PLL for XCVR channels, the VCO frequency has to be such that the required fPLL output frequency can be achieved using a legal value of the counter used for HSSI clock output.
Total Power (W)	Shows the total estimated power for this row (in W).
User Comments	Enter any comments. This is an optional entry.

For more information about the PLLs available in Arria 10 devices, refer to the *Clock Networks and PLLs* chapter of the *Arria 10 Device Handbook*.

Related Information

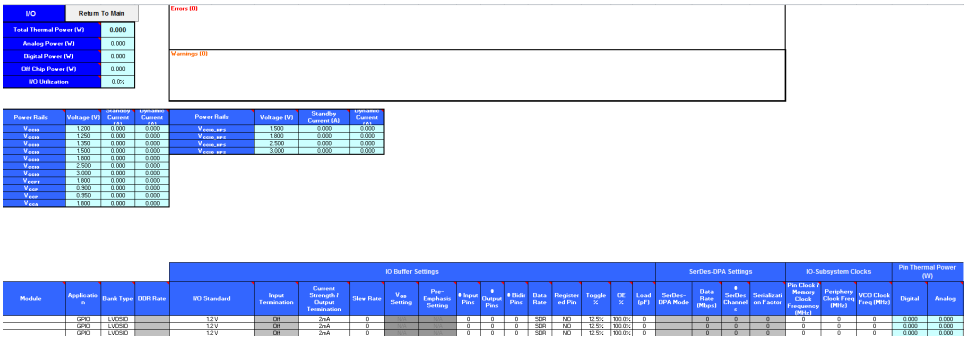
- Clock Networks and PLLs in Arria 10 Devices
- Early Power Estimator for Intel Arria 10 Graphical User Interface on page 11

- Arria 10 EPE - Common Worksheet Elements on page 16

4.8. Arria 10 EPE - I/O Worksheet

Each row in the I/O worksheet of the Early Power Estimator (EPE) for Arria 10 represents a design module where the I/O pins have the same I/O standard, input termination, current strength or output termination, data rate, clock frequency, output enable static probability, and capacitive load.

Figure 18. I/O Worksheet of the Early Power Estimator



When using the EPE spreadsheet, it is assumed you are using external termination resistors as recommended for SSTL and high-speed transceiver logic HSTL. If your design does not use external termination resistors, choose the LVTTL/ LVCMOS I/O standard with the same VCCIO and similar current strength as the terminated I/O standard. For example, if you are using the SSTL-2 Class II I/O standard with a 16 mA current strength, you must select 2.5 V as the I/O standard and 16 mA as the current strength in the EPE spreadsheet.

To use on-chip termination (OCT), select the **Current Strength/Output Termination** option in the EPE spreadsheet.

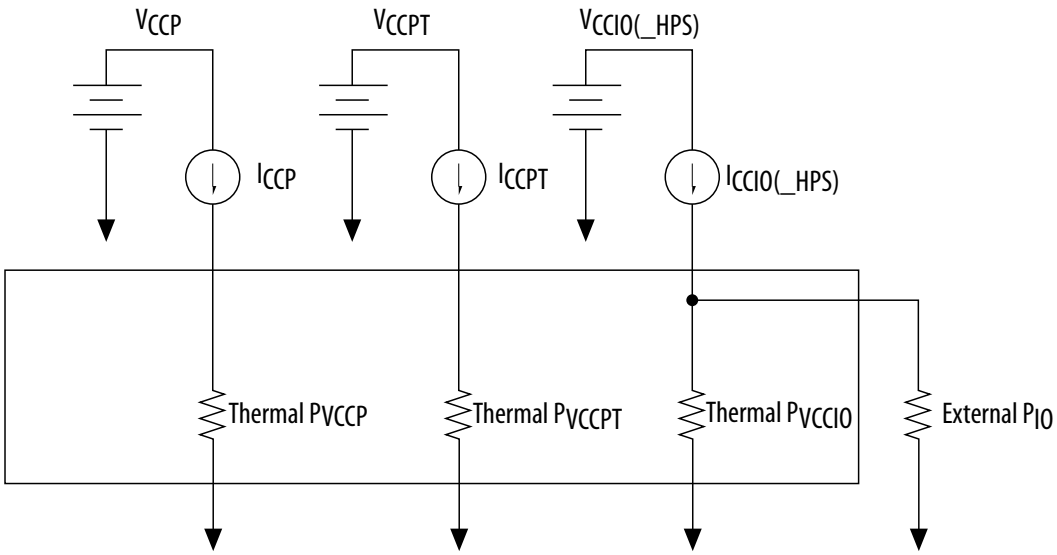
The power reported for the I/O signals includes thermal and external I/O power. The total thermal power is the sum of the thermal power consumed by the device from each power rail, as shown in the following equation.

Figure 19. Total Thermal Power

$$\text{thermal power} = \text{thermal } P_{VCCP} + \text{thermal } P_{VCCPT} + \text{thermal } P_{VCCIO(\_HPS)}$$

The following figure shows the I/O power consumption. The I_{CCIO} power rail includes both the thermal P_{IO} and the external P_{IO}.

Figure 20. I/O Power Representation



The VREF pins consume minimal current (typically less than 10 µA) and is negligible when compared with the current consumed by the general purpose I/O (GPIO) pins; therefore, the EPE spreadsheet does not include the current for VREF pins in the calculations.

Table 13. I/O Worksheet Information

Column Heading	Description
Module	Specify a name for the I/O in this column. This is an optional value.
Application	Specify the application for this I/O row. GPIO and SerDes interfaces can be instantiated using this field. Use the IP worksheet to instantiate EMIF interfaces.
Bank Type	Specifies the type of I/O bank for this row. An LVDSIO bank supports I/O standards up to 1.8V as well as LVDS I/O standards. 3V I/O banks support I/O standards up to 3.0V but not LVDS I/O standards.
DDR Rate	Specifies the clock rate of PHY logic. Determines the clock frequency of PHY logic in relation to the memory clock frequency. For example, if the memory clock sent from the FPGA to the memory device is toggling at 800MHz, a quarter rate interface means that the PHY logic in the FPGA runs at 200MHz.
I/O Buffer Settings - I/O Standard	Specifies the I/O standard used by the I/O pins in this module.
I/O Buffer Settings - Input Termination	Specifies the input termination setting for the input and bidirectional pins in this module.
I/O Buffer Settings - Current Strength/Output Termination	Specifies the current strength or output termination setting for the output and bidirectional pins in this module. Current strength and output termination are mutually exclusive.

continued...

Column Heading	Description
I/O Buffer Settings - Slew Rate	Specifies the slew rate setting for the output and bidirectional pins in this module. Using a lower slew rate setting helps reduce switching noise but may increase delay.
I/O Buffer Settings - V_{OD} Setting	Specifies the differential output voltage (V_{OD}) for the output and bidirectional pins in the module. A smaller number indicates a smaller VOD which reduces static power.
I/O Buffer Settings - Pre-Emphasis Setting	Specifies the pre-emphasis setting for the output and bidirectional pins in this module. A smaller number indicates a smaller pre-emphasis which reduces dynamic power.
I/O Buffer Settings - # Input Pins	Specifies the number of input-only I/O pins in this module. Differential pin pairs count as one pin.
I/O Buffer Settings - # Output Pins	Specifies the number of output-only I/O pins in this module. Differential pin pairs count as one pin.
I/O Buffer Settings - # Bidir Pins	Specifies the number of bidirectional I/O pins in this module. Differential pin pairs count as one pin. The I/O pin is treated as an output when its output enable signal is active and is treated as an input when the output enable signal is disabled. An I/O pin configured as a bidirectional pin, but used only as an output, consumes more power than if it were configured as an output-only pin, due to the toggling of the input buffer every time the output buffer toggles (they share a common pin).
I/O Buffer Settings - Data Rate	Indicates whether I/O value will change once (Single-Data Rate) or twice (Double-Data Rate) per cycle.
I/O Buffer Settings - Registered Pin	Indicates whether the pin is registered or not.
I/O Buffer Settings - Toggle %	Percentage of clock cycles when the I/O signal changes value. This value is multiplied by clock frequency to determine the number of transitions per second. If DDR is selected, the toggle rate is multiplied by an additional factor of two.
I/O Buffer Settings - OE %	For modules with Input Termination set to **OFF**, enter the average percentage of time that: • Output I/O is enabled • Bidirectional I/O is an output and enabled During the remaining time: • Output I/O is tri-stated • Bidirectional I/O is an input Input Termination cannot be active while the Output I/O is enabled, so for modules with Input Termination not set to **OFF**, enter the average percentage of time that On-Chip Termination is inactive (that is, 1-percentage that the On-Chip Termination is active).This number must be a percentage between 0% and 100%.
I/O Buffer Settings - Load (pF)	Specifies pin loading external to the chip (in pF). Applies only to outputs and bidirectional pins. Pin and package capacitance is already included in the I/O model. Include only off-chip capacitance.
SerDes-DPA Settings - SerDes-DPA Mode	Selects the mode of SerDes-DPA block.
SerDes-DPA Settings - Data Rate (Mbps)	The maximum data rate of the SerDes channels in Mbps.
SerDes-DPA Settings - # SerDes Channels	The number of channels running at the data rate of this SerDes domain.
SerDes-DPA Settings - Serialization Factor	Number of parallel data bits for each serial data bit.

continued...

Column Heading	Description
I/O Subsystem Clocks - Pin Clock/Memory Clock Frequency (MHz)	Clock frequency (in MHz). 100 MHz with a 12.5% toggle percentage would mean that each I/O pin toggles 12.5 million times per second (100 MHz * 12.5%).
I/O Subsystem Clocks - Periphery Clock Freq (MHz)	The I/O subsystem internal PHY clock frequency. This is an output-only field. In SerDes applications, the PHY clock frequency is a function of the SerDes rate and serialization factor. In external memory interface (EMIF) applications, the PHY clock frequency is a function of the memory clock frequency and DDR rate of the EMIF IP.
I/O Subsystem Clocks - VCO Clock Freq (MHz)	The internal VCO operating frequency. This is an output-only field. In SerDes applications, VCO frequency is a function of SerDes Data rate. In external memory interface (EMIF) applications, the VCO frequency is a function of the memory clock frequency of the EMIF IP. The VCO frequency is not applicable in GPIO mode.
Pin Thermal Power (W) - Digital	Power dissipated in the digital domain of the I/O-subsystem including GPIO, EMIF controller and SerDes controller.
Pin Thermal Power (W) - Analog	Power dissipated in the analog domain of the I/O-subsystem, for example, I/O buffers.
User Comments	Enter any comments. This is an optional entry.

For more information about the I/O standard termination schemes, refer to *I/O and High Speed I/Os in Arria 10 Devices*.

Related Information

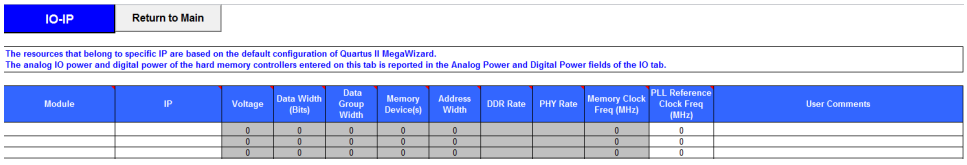
- I/O and High Speed I/O in Arria 10 Devices
- Early Power Estimator for Intel Arria 10 Graphical User Interface on page 11
- Arria 10 EPE - Common Worksheet Elements on page 16

4.9. Arria 10 EPE - I/O-IP Worksheet

Each row in the I/O-IP worksheet of the Early Power Estimator (EPE) for Arria 10 represents a design module.You use the I/O-IP worksheet to instantiate external memory interface and HPS IPs supported in Arria 10. The I/O-IP worksheet populates other EPE worksheets with resources used by a selected IP.

Analog I/O power and digital power of hard memory controllers and HPS IPs entered on this tab are reported in the Analog Power and Digital Power fields of the I/O worksheet. If the IP uses other resource types (for example Logic or PLL), the power is reported on the corresponding worksheet.

Figure 21. I/O-IP Worksheet of the Early Power Estimator



I/O-IP Worksheet Information

Column Heading	Description
Module	Specify a name for the IP in this column. The module name depends on the selected IP type. It helps to cross-reference each IP module and its corresponding auto-populated entries on other worksheets.
IP	Specifies the name of the IP in the design.
Voltage	Specifies the I/O voltage of the signaling between periphery device and interface.
Data Width (Bits)	Specifies the interface data width of the specific IP (in bits).
Data Group Width	Specifies the number of DQ pins per data group.
Memory Device(s)	Specifies the number of memory devices connected to the interface.
Address Width	Specifies the address width. This value is used to derive the total number of address pins required.
DDR Rate	Specifies the clock rate of user logic. Determines the clock frequency of user logic in relation to the memory clock frequency. For example, if the memory clock sent from the FPGA to the memory device is toggling at 800MHz, a "Quarter rate" interface means that the user logic in the FPGA runs at 200MHz.
PHY Rate	Specifies the clock rate of PHY logic. Determines the clock frequency of PHY logic in relation to the memory clock frequency. For example, if the memory clock sent from the FPGA to the memory device is toggling at 800MHz, a "Quarter rate" interface means that the PHY logic in the FPGA runs at 200MHz.
Memory Clock Freq (MHz)	Specifies the frequency of memory clock (in MHz).
PLL Reference Clock Freq (MHz)	Specifies the PLL Reference Clock Frequency (in MHz).
User Comments	Enter any comments. This is an optional entry.

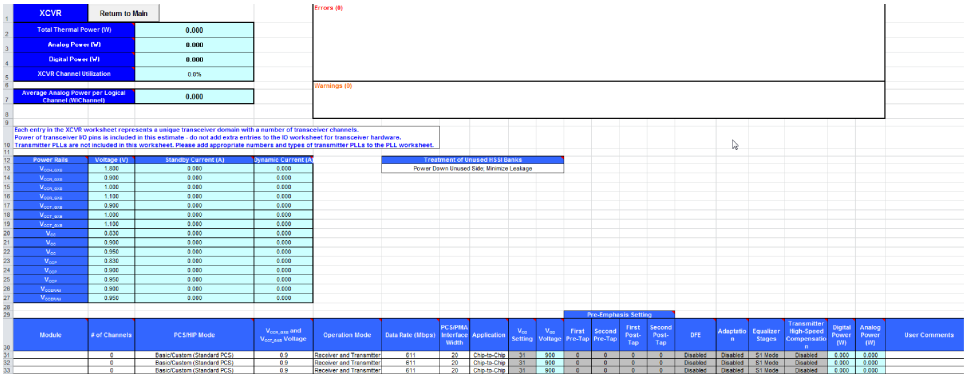
Related Information

- Early Power Estimator for Intel Arria 10 Graphical User Interface on page 11
- Arria 10 EPE - Common Worksheet Elements on page 16

4.10. Arria 10 EPE - XCVR Worksheet

The XCVR worksheet of the Early Power Estimator (EPE) for Arria 10 allows you to enter XCVR resources and their settings for all modules in your design. The power of transceiver I/O pins is included in this worksheet. Transmitters and receivers assume 100 Ω termination. The power of transmitter PLLs is not included in this worksheet, but is specified in the PLL worksheet instead.

Figure 22. XCVR Worksheet of the Early Power Estimator



The Early Power Estimator does not include power estimates for the On-Die Instrumentation (ODI) XCVR block. To estimate power for transceiver channels that include the ODI block, use the Quartus Prime Power Analyzer.

The Early Power Estimator makes the following simplifying assumptions about the transceiver clock network and the blocks used:

- x6 clock lines are used for all GX channels. GT channels use dedicated GT clock lines. (Refer to the Arria 10 Transceiver PHY User Guide for details on the clock line types.)
- For each duplex (both receiver and transmitter active) and transmitter-only row in the XCVR worksheet, there is one master CGB and one reference clock pin per 6 channels. Each row has at least one master CGB and at least one reference clock pin. Rows with receiver-only channels assume there is one reference clock pin per 6 channels, but no master CGBs. Each row has at least one reference clock pin.

  For example, a single-channel duplex design assumes one master CGB and one reference clock pin. The same is true if 6 channels are entered on one row. However, if 6 channels are entered into 6 rows (1 channel per row), each row assumes one master CGB and one reference clock pin, for a total of six master CGBs and six reference clock pins. Consequently, entering the same number of identical channels into individual rows results in a slightly different power estimate than if all channels are entered into one row.

Table 14. General Settings in the XCVR Worksheet

Input Parameter	Description
Treatment of Unused HSSI Banks	Specifies how transceiver banks not actively used by channels should be treated when calculating static power. You can select one of the following options: • Power Down Unused Side; Minimize Leakage • Power Down Unused Side; Minimize Number of Supply Voltages • Power Up Unused Side; Minimize Leakage • Power Up Unused Side; Minimize Number of Supply Voltages If all high-speed serial interface (HSSI) banks on one side are not used, they can all be powered down or remain powered up. You can select the voltage for unused-but-powered banks to minimize static power (that is, leakage), or to minimize the number of power supply voltages required.

Input Parameter	Description
	For example, if active transceiver channels use V_{CCR_GXB}=1.03V and 1.12V, selecting **Minimize Leakage** will assume the unused-but-powered banks use V_{CCR_GXB}=0.95V, which is the lowest supported voltage (assuming that the currently selected device supports this voltage). Selecting **Minimize Number of Supply Voltages** will assume the unused-but-powered banks use V_{CCR_GXB}=1.03V, which is the lowest voltage used by active channels, thus eliminating the need for the 0.95V power supply on V_{CCR_GXB}. If you select **Power Down Unused Side**, unused HSSI banks on the side that has active channels are still powered. This is because HSSI banks cannot be powered down individually; only the whole HSSI side can be powered down. For more details, refer to the *Arria 10 GX, GT, and SX Device Family Pin Connection Guidelines.* For devices with transceivers on both sides of the device, the Early Power Estimator determines whether one side or both sides should be powered, based on the number of transceiver channels and ATX PLLs, CMU PLLs, and fPLLs. If half or fewer of the available channels are used, the Early Power Estimator assumes that they can be placed on one side of the device. The Early Power Estimator assumes that both sides are in use if any of the following are true: • More than half of the channels are used. • More than half the available ATX PLLs, CMU PLLs, or fPLLs are used. • More than half the available PCIe HIP blocks are used. If channel placement in your design spans both sides of the device despite using fewer than half the resources, or if you want both sides of the device to be powered for future use, select one of the **Power Up Unused Side** settings, which cause the Early Power Estimator to asume that both sides are powered. *Note:* PLLs specified in the PLL worksheet, and their VCCR_GXB voltages, are also considered when determining how many HSSI banks are actively used. For example, if all active channels in the XCVR worksheet use VCCR_GXB=1.03V, but one PLL in the PLL worksheet uses VCCR_GXB=0.95V, there will be at least one HSSI bank operating at VCCR_GXB=0.95V.

Each row in the XCVR worksheet represents a separate transceiver domain. Enter the following parameters for each transceiver domain:

Table 15. XCVR Worksheet Information

Column Heading	Description
Module	Specifies a name for the module. This is an optional value.
# of Channels	Specifies the number of channels used in this transceiver domain. Each row represents one transceiver domain. These channels are grouped together in one transceiver bank, or two or more adjacent transceiver banks and clocked by one or more common transmitter PLLs. *Note:* For PCI Express protocols with Hard IP, the Hard IP block supports x1, x2, x4, and x8 modes. For each row, a minimum number of PCI Express Hard IP blocks are instantiated to support the number of channels entered. For example, if 5 channels are entered, 2 Hard IP blocks are instantiated (one in x4 and one in x1 mode).

continued...

Column Heading	Description
PCS/HIP Mode	Specifies the mode in which the PCS and HIP blocks operate. This mode depends on the communication protocol or standard that the channels on this row implement.
V_{CCR_GXB} and V_{CCT_GXB} Voltage	Specifies the voltage of the V_{CCR_GXB} and V_{CCT_GXB} rails. Allowed values depend on the selected device and selected data rate.
Operation Mode	Specifies whether the hardware is configured in full duplex transceiver mode (Receiver and Transmitter) or in Receiver Only or Transmitter Only mode. Allowed values depend on the selected PCS/HIP mode.
Data Rate (Mbps)	Specifies the data rate (in Mbps) for the transceiver. Allowed values depend on the selected protocol, selected device, and the V_{CCR_GXB} and V_{CCT_GXB} voltages.
PCS/PMA Interface Width	Specify the width of the parallel data bus between PCS and PMA.
Application	Select the application type from **Chip-to-Chip**, **Backplane**, or **Custom**. Select **Custom** to enable manual editing of advanced channel options for the current row.
V_{OD} Setting	The output differential voltage (V_{OD}) setting of the transmitter channel PMA. To enable this setting, select **Custom** in the **Application** column.
V_{OD} Voltage	The output differential voltage (V_{OD}) of the transmitter channel PMA (in mV). This voltage depends on the V_{OD} setting and the V_{CCT_GXB} voltage. For the purpose of power calculation, it is assumed that the transmitter uses a termination resistance of 100 Ohms.
Pre-Emphasis Setting–First Pre-Tap	Specifies the pre-emphasis setting used by the transmitter channel PMA. Allowed values for individual taps depend on selected V_{OD} setting and selected values of other pre-emphasis taps. Only positive values of tap settings are listed. Power consumption does not depend on the sign (positive or negative) of individual taps. To enable these settings, select **Custom** in the **Application** column.
Pre-Emphasis Setting–Second Pre-Tap	
Pre-Emphasis Setting–First Post-Tap	
Pre-Emphasis Setting–Second Post-Tap	
DFE	Specify mode of the decision feedback equalizer (DFE). Allowed values depend on the selected data rate. To enable this setting, select **Custom** in the **Application** column.
Adaptation	Specify if the adaptation feature is used. This option should be enabled if the channels use either CTLE adaptation or DFE adaptation. To enable this setting, select **Custom** in the **Application** column.
Equalizer Stages	Specify whether the continuous time linear equalizer (CTLE) uses high data rate mode (S1 Mode) or high gain mode (Non-S1 Mode). Allowed values depend on the selected data rate. To enable this setting, select **Custom** in the **Application** column.
Transmitter High-Speed Compensation	Specifies if the power distribution network (PDN) induced inter-symbol interference (ISI) compensation is enabled in the TX driver. To enable this setting, select **Custom** in the **Application** column.

continued...

Column Heading	Description
Digital Power (W)	The total power of the transmitter channel PCS, receiver channel PCS, and PCI Express Hard IP blocks used by all channels on this row (in W).
Analog Power (W)	The total power of all analog circuitry on this row (in W). This power excludes power of PCS and PCI Express Hard IP blocks, whose power is provided in the Digital Power column, and transmitter PLLs, whose power is provided in the PLL worksheet.
User Comments	Enter any comments. This is an optional entry.

For more information about the transceiver architecture of the supported device families, refer to the *Transceiver PHY User Guide* for Arria 10.

Related Information

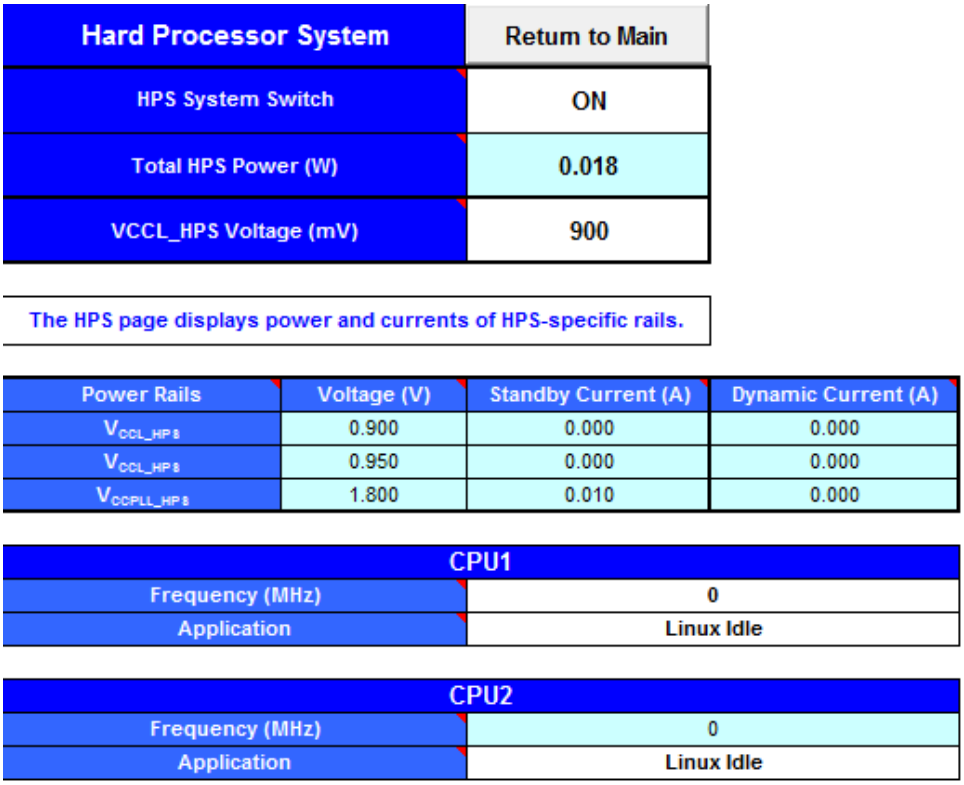
- Arria 10 Transceiver PHY User Guide
- Early Power Estimator for Intel Arria 10 Graphical User Interface on page 11
- Arria 10 EPE - Common Worksheet Elements on page 16

4.11. Arria 10 EPE - HPS Worksheet

The HPS worksheet of the Early Power Estimator (EPE) for Arria 10 applies to Arria 10 devices with HPS.

To enable parameter entry into the HPS worksheet, first turn **ON** the **HPS System Switch** in the HPS worksheet. For Arria 10 devices, select your peripheral modules in the I/O-IP worksheet. The power of the respective peripheral, except the corresponding I/O power, is shown in this HPS worksheet. To evaluate HPS I/O power, HPS peripherals should be instantiated using the I/O-IP worksheet.

Figure 23. HPS Worksheet of the Early Power Estimator



Hard Processor System	Return to Main
HPS System Switch	ON
Total HPS Power (W)	0.018
VCCL_HPS Voltage (mV)	900

The HPS page displays power and currents of HPS-specific rails.

Power Rails	Voltage (V)	Standby Current (A)	Dynamic Current (A)
V_{CCL_HPS}	0.900	0.000	0.000
V_{CCL_HPS}	0.950	0.000	0.000
V_{CCPLL_HPS}	1.800	0.010	0.000

CPU1	
Frequency (MHz)	0
Application	Linux Idle

CPU2	
Frequency (MHz)	0
Application	Linux Idle

Table 16. HPS Worksheet Information

Module	Parameters	Description
Hard Processor System	HPS System Switch	Turns the HPS system on and off. This selection affects the P_{STATIC} power.
	Total HPS Power (W)	Specifies the total power dissipated by the maximum available active processors (in W).
	VCCL_HPS Voltage (mV)	Specifies the core HPS voltage (in mV).
CPU1/2	Frequency	Specifies the operating frequency of the CPU.
	Application	Select a benchmark application representative of the application that will run on this CPU.

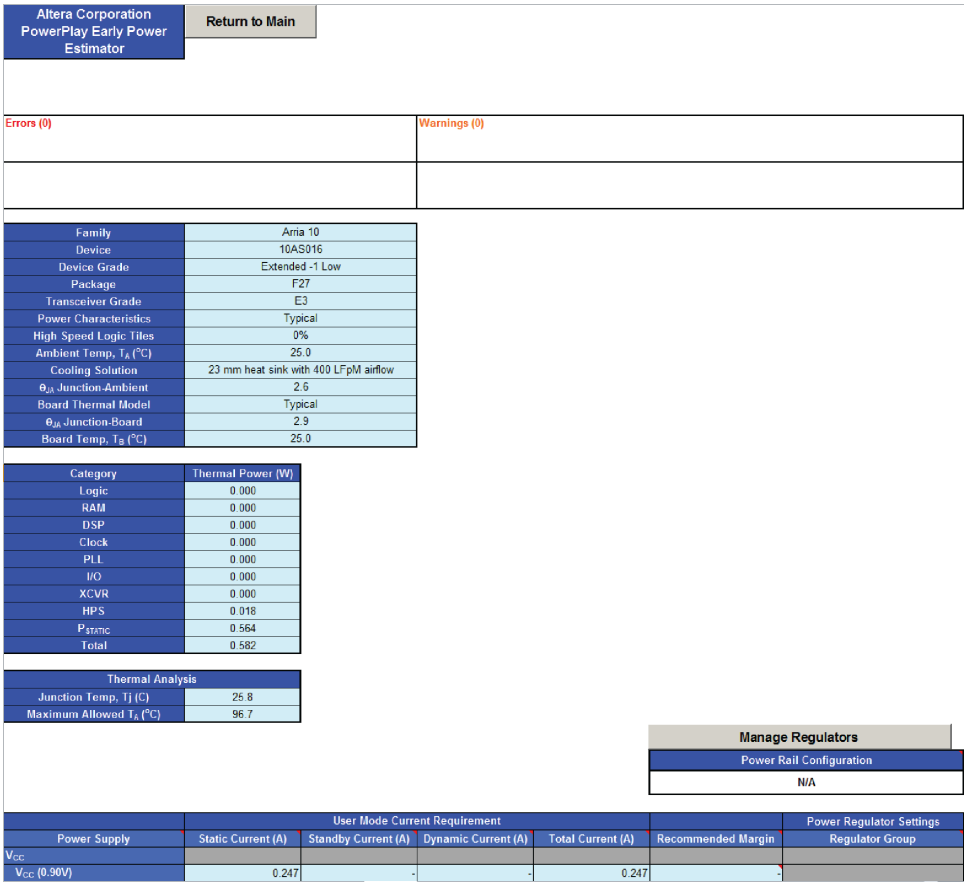
Related Information

- Early Power Estimator for Intel Arria 10 Graphical User Interface on page 11
- Arria 10 EPE - Common Worksheet Elements on page 16

4.12. Arria 10 EPE - Report Worksheet

The Report worksheet shows all the information and power estimation results from the Early Power Estimator (EPE) for Arria 10.

Figure 24. Report Worksheet of the Early Power Estimator



Altera Corporation PowerPlay Early Power Estimator | Return to Main

Errors (0)	Warnings (0)

Family	Arria 10
Device	10AS016
Device Grade	Extended -1 Low
Package	F27
Transceiver Grade	E3
Power Characteristics	Typical
High Speed Logic Tiles	0%
Ambient Temp, T_A (°C)	25.0
Cooling Solution	23 mm heat sink with 400 LFpM airflow
θ_{JA} Junction-Ambient	2.6
Board Thermal Model	Typical
θ_{JA} Junction-Board	2.9
Board Temp, T_B (°C)	25.0

Category	Thermal Power (W)
Logic	0.000
RAM	0.000
DSP	0.000
Clock	0.000
PLL	0.000
I/O	0.000
XCVR	0.000
HPS	0.018
P_{STATIC}	0.564
Total	0.582

Thermal Analysis	
Junction Temp, Tj (C)	25.8
Maximum Allowed T_A (°C)	96.7

Manage Regulators

Power Rail Configuration
N/A

	User Mode Current Requirement					Power Regulator Settings
Power Supply	Static Current (A)	Standby Current (A)	Dynamic Current (A)	Total Current (A)	Recommended Margin	Regulator Group
V_{CC}						
V_{CC} (0.90V)	0.247	-	-	0.247	-	

Table 17. Power Rail Configuration Settings in the Report Worksheet

Input Parameter	Description
Power Rail Configuration	Selects a power rail configuration for assignment of supply rails to regulator groups. This field is enabled regardless of the **Power Characteristics** setting in the Main worksheet. You will receive a warning message if you select a power rail configuration when the **Power Characteristics** setting is **Typical**. Choose **Custom** to manually enter regulator group selection, or to modify the results of automatic selection.

The Report worksheet provides current requirements for each voltage rail, expressed in terms of static current, standby current, dynamic current, and total current.

Table 18. Current and Power Regulator Requirements Per Voltage Rail

Module	Parameter	Description
User Mode Current Requirement	Power Supply	Indicates the power supply rail name and voltage applied to the specified rail (in V).
	Static Current (A)	Indicates the component of current consumed from the specified power rail whenever the power is applied to the rail, independent of circuit activity (in A). This current is dependent on device size, device grade, power characteristics and junction temperature.
	Standby Current (A)	Indicates the component of active current drawn from the specified power rail by all modules on all worksheets, independent of signal activity (in A). This current is independent of device grade, power characteristics and junction temperature. Standby current includes, but is not limited to, I/O and transceiver DC bias current. Device size has only a small impact on transceiver DC bias current.
	Dynamic Current (A)	Indicates the component of active current drawn from the specified power rail due to signal activity of all modules on all worksheets (in A). This current depends on device size, but is independent of device grade, power characteristics and junction temperature.
	Total Current (A)	Indicates the total current consumed from the specified power rail (in A). This value is the sum of static, standby and dynamic current.
	Recommended Margin	The recommended margin on Total Current estimates to use for regulator sizing due to possible inaccuracies in the power model. The Recommended Margin percentage represents a model accuracy such that >95% of designs fall within the Recommended Margin of silicon. To enable display of the recommended margin, **Power Characteristics** on the Main worksheet must be set to **Maximum**. Final power models are correlated with measured silicon results using thousands of designs. (Refer to the Main worksheet for the Power Model status for a given device).

continued...

Module	Parameter	Description
		For the V_{cc} rail, a design-specific margin is provided. This margin is calculated based on the ratio of static to dynamic power because static power is reported as a limit and only the dynamic power portion has recommended margin. For all other rails, the recommended margin is a static value.
Power Regulator Settings	Regulator Group	Indicates the number of the regulator group to which this supply rail is assigned. The regulator group numbers correspond to the group numbers shown in the Enpirion worksheet. If one of the automatic assignment modes is selected in the Power Rail Configuration field, the regulator group numbers also correspond to the group numbers in the pin connection guidelines. To manually edit fields in this column, select **Custom** under **Power Rail Configuration**. Manual edits may be necessary to correct grouping errors that may result from automatic assignment.

Related Information

- Early Power Estimator for Intel Arria 10 Graphical User Interface on page 11
- Arria 10 EPE - Common Worksheet Elements on page 16

4.13. Arria 10 EPE - Enpirion Worksheet

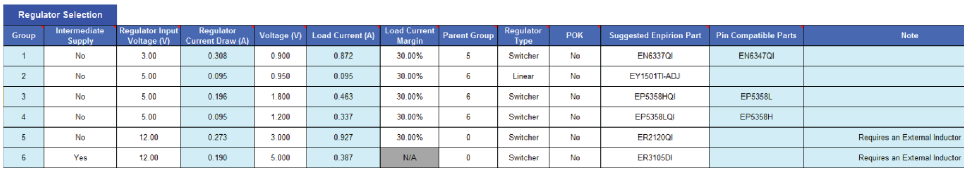
Each row in the Regulator Selection table of the Enpirion worksheet of the Early Power Estimator (EPE) for Arria 10 represents the power solution for a single regulator group.

Enpirion power devices are available that satisfy the power requirements for the power rails on Intel FPGA devices. Power devices are selected based on load current, input and output voltages, and power-delivery configuration.

Regulator groups are created by combining rails that can be allowably supplied from the same source. Enpirion device selection is enabled when **Power Characteristics** in the Main worksheet is set to **Maximum**, and the **Regulator Group** section of the Report worksheet is set up correctly with no grouping errors.

In the following figure, a 12-V off-line regulator supplies input power for Groups 5 and 6. The regulator for Group 6 is an intermediate supply, which does not directly power any of the FPGA supplies, but provides input power to regulators for Groups 2, 3, and 4. The 3-V regulator supplying Group 5 provides power for FPGA supplies, but also acts as an intermediate supply providing input power for Group 1.

Figure 25. Enpirion Worksheet of the EPE Spreadsheet for Arria 10



Regulator Selection												
Group	Intermediate Supply	Regulator Input Voltage (V)	Regulator Current Draw (A)	Voltage (V)	Load Current (A)	Load Current Margin	Parent Group	Regulator Type	POK	Suggested Enpirion Part	Pin Compatible Parts	Note
1	No	3.00	0.308	0.900	0.872	30.00%	5	Switcher	No	EN6337QI	EN6347QI	
2	No	5.00	0.095	0.950	0.095	30.00%	6	Linear	No	EY1501TI-ADJ		
3	No	5.00	0.196	1.800	0.463	30.00%	6	Switcher	No	EP5358HQI	EP5358L	
4	No	5.00	0.095	1.200	0.337	30.00%	6	Switcher	No	EP5358LQI	EP5358H	
5	No	12.00	0.273	3.000	0.927	30.00%	0	Switcher	No	ER2120QI		Requires an External Inductor
6	Yes	12.00	0.190	5.000	0.387	N/A	0	Switcher	No	ER3105DI		Requires an External Inductor

Table 19. Enpirion Worksheet Information

Column Heading	Description
Group	The regulator group number for this regulator. The regulator group numbers correspond to the group numbers shown in the Report worksheet.
Intermediate Supply	Indicate whether the supply is an intermediate supply. An intermediate supply is driven by a regulator that is not connected to any supply rails on the FPGA. Instead, such a regulator drives other regulators. If a regulator provides power to both the FPGA and other regulators, this field should be set to *No*.
Regulator Input Voltage (V)	Specifies the input voltage for the regulator. This field is filled automatically if you specify a non-zero Parent Group.
Regulator Current Draw (A)	Specifies the required input current to the regulator. It is assumed that all regulators have a current efficiency of 85%.
Voltage (V)	Specifies the output voltage for the regulator.
Load Current (A)	Specifies the load current required by the pins from the regulator.
Load Current Margin	Margin added to the load current to account for component variability. Recommended rail-specific margin values can be found in the Report worksheet in the **Recommended Margin** column.
Parent Group	Specifies the group number of the regulator that supplies input voltage to the regulator in the current row. This value is applicable only when the input voltage is provided by another regulator on this worksheet.
Regulator Type	In some cases, a linear regulator (LDO) may be a good choice to supply one of the group voltages. The efficiency of an LDO is the ratio of output voltage to input voltage. In the figure, Group 2 can be efficiently supplied by an LDO.
POK	Select **Yes** to select a regulator with a Power OK (**POK**) output to assist with sequencing.
Note	A note may be displayed here, depending on the chosen value under **Suggested Enpirion Part**.
Suggested Enpirion Part	Suggested Enpirion part is automatically populated with the part number of the device that most closely matches the **Load Current (A)**, **Regulator Type** and **POK** selections. The dropdown can be used to optionally select devices with equivalent or higher current capabilities. To finalize regulator selection, evaluate the V_{RM} voltage ripple specification and efficiency against the FPGA device requirement from the appropriate datasheets.

continued...

Column Heading	Description
	To enable this field, you must set the Power Characteristics setting in the Main worksheet to Maximum.
Pin Compatible Parts	Pin compatible parts are devices with equivalent or higher current capabilities that can be placed on the same PCB footprint as the **Suggested Enpirion Part**. Additional components or changes to component values may be required when using a pin compatible part. To enable this field, you must set the Power Characteristics setting in the Main worksheet to Maximum.

Related Information

- Arria 10 EPE - Report Worksheet on page 46
- Early Power Estimator for Intel Arria 10 Graphical User Interface on page 11
- Arria 10 EPE - Common Worksheet Elements on page 16

5. Factors Affecting the Accuracy of the Early Power Estimator for Intel Arria 10

Many factors can affect the estimated values displayed in the Early Power Estimator (EPE) for Arria 10 spreadsheet. In particular, the input parameters entered concerning toggle rates, airflow, temperature, and heat sinks must be accurate to ensure that the system is modeled correctly in the EPE spreadsheet.

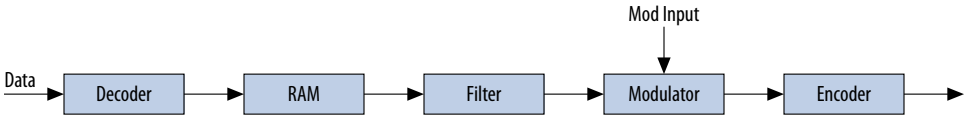
5.1. Toggle Rate

The toggle rates specified in the Early Power Estimator for Arria 10 spreadsheet can have a large impact on the dynamic power consumption displayed. To obtain an accurate estimate, you must input toggle rates that are realistic. Determining realistic toggle rates requires knowing what kind of input the FPGA is receiving and how often it toggles.

To get an accurate estimate if the design is not complete, isolate the separate modules in the design by function, and estimate the resource usage along with the toggle rates of the resources. The easiest way to accomplish this is to leverage previous designs to estimate the toggle rates for modules with similar function.

The input data in the following figure is encoded for data transmission and has a roughly 50% toggle rate.

Figure 26. Decoder and Encoder Block Diagram



In this case, you must estimate the following:

- Data toggle rate
- Mod input toggle rate
- Resource estimate for the Decoder, RAM, Filter, Modulator, and Encoder module
- Toggle rate for the Decoder, RAM, Filter, Modulator, and Encoder module

You can generate these estimates in many ways. If you used similar modules in the past with data inputs of roughly the same toggle rates, you can leverage that information. If MATLAB simulations are available for some blocks, you can obtain the toggle rate information from the simulations. If the HDL is available for some of the modules, you can simulate them to obtain toggle rates.

If the HDL is complete, the best way to determine toggle rates is to simulate the design. The accuracy of toggle rate estimates depends on the accuracy of the input vectors. Therefore, determining whether or not the simulation coverage is high gives you a good estimate of how accurate the toggle rate information is.

The Quartus Prime software can determine toggle rates of each resource used in the design if you provide information from simulation tools. Designs can be simulated in many different tools and the information provided to the Quartus Prime software through a Signal Activity File (`.saf`) or Value Change Dump File (`.vcd`). The Quartus Prime Power Analyzer provides the most accurate power estimate.

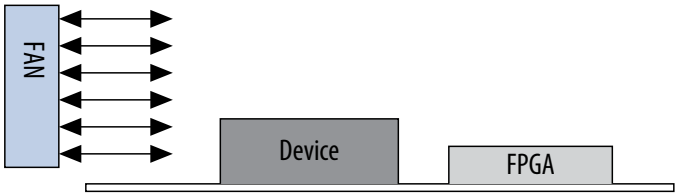
5.2. Airflow

It is often difficult to place the device adjacent to the fan providing the airflow. The path of the airflow might traverse a length on the board before reaching the device, thus diminishing the actual airflow the device receives. The following figure shows a fan that is placed at the end of the board. The airflow at the FPGA is weaker than the airflow at the fan.

Figure 27. Airflow and FPGA Position

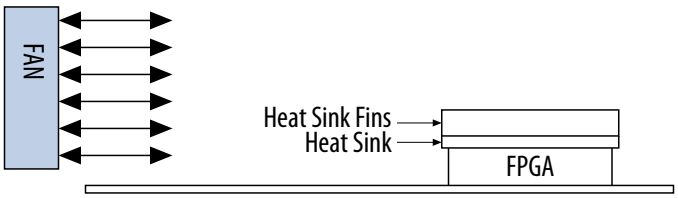
You must also consider blocked airflow. The following figure shows a device blocking the airflow from the FPGA, significantly reducing the airflow seen at the FPGA. The airflow from the fan also has to cool board components and other devices before reaching the FPGA.

Figure 28. Airflow with Component and FPGA Positions



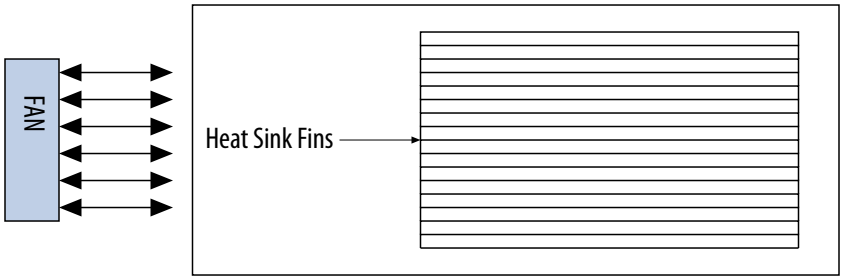
If you are using a custom heat sink, you do not need to enter the airflow directly into the EPE spreadsheet but it is required to enter the θ_{SA} value for the heat sink with the knowledge of what the airflow is at the device. Most heat sinks have fins located above the heat sink to facilitate airflow. The following figure shows the FPGA with a heat sink.

Figure 29. Airflow and Heat Sinks



When placing the heat sink on the FPGA, the direction of the fins must correspond with the direction of the airflow. A top view shows the correct orientation of the fins.

Figure 30. Heat Sink (Top View)



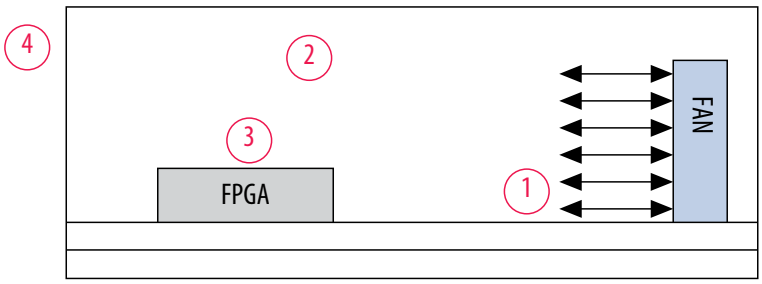
These considerations can influence the airflow at the device. When entering information into the EPE spreadsheet, you have to consider these implications to get an accurate airflow value at the FPGA.

5.3. Temperature

To calculate the thermal information of the device correctly, you must enter the ambient air temperature for the device in the Early Power Estimator (EPE) for Arria 10 spreadsheet. Ambient temperature refers to the temperature of the air around the device. The temperature of the air around the device is usually higher than the ambient temperature outside of the system. To get an accurate representation of ambient temperature for the device, you must measure the temperature as close to the device as possible with a thermocouple device.

Entering the incorrect ambient air temperature can drastically alter the power estimates in the EPE spreadsheet. The following figure shows a simple system with the FPGA housed in a box. In this case, the temperature is very different at each of the numbered locations.

Figure 31. Temperature Variances



For example, location 3 is where the ambient temperature pertaining to the device should be obtained for input into the EPE spreadsheet. Locations 1 and 2 are cooler than location 3 and location 4 is likely close to 25 °C if the ambient temperature outside the box is 25 °C. Temperatures close to devices in a system are often in the neighborhood of 50–60 °C but the values can vary significantly. To obtain accurate power estimates from the EPE spreadsheet, you must get a realistic estimate of the ambient temperature near the FPGA device.

5.4. Heat Sink

The following equations show how to determine power when using a heat sink.

Figure 32. Total Power

$$P = \frac{T_J - T_A}{\theta_{JA}}$$

Figure 33. Junction–to–Ambient Thermal Resistance

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

You can obtain the junction-to-case thermal resistance (θ_{JC}) value that is specific to the FPGA from the data sheet. The case-to-heat-sink thermal resistance (θ_{CS}) value refers to the material that binds the heat sink to the FPGA and is approximated to be 0.1 °C/W. You can obtain the heat sink-to-ambient thermal resistance (θ_{SA}) value from the manufacturer of the heat sink. Ensure that you obtain this value for the right conditions for the FPGA, which include analyzing the correct heat sink information at the appropriate airflow at the device.

6. Document Revision History

Document Version	Intel Quartus Prime Version	Changes
2021.06.04	18.0.1	• In the *Overview* chapter, modified the second bullet point in the *Power Model Status* topic. • In the *Worksheets* chapter, modified the *Recommended margin on Vcc* bullet point in the *Power Model Status* entry of the *Input Parameter Information* table.

Date	Version	Changes
March 2017	2017.03.13	Rebranded as Intel.
November 2016	2016.11.07	• Implemented editorial updates throughout. • Updated figures 3-1 and 3-3. • Updated parameter information throughout chapter 4. • Updated figures 4-1, 4-4, 4-5, 4-13, 4-14, 4-18, and 4-19. • Replaced *Additional Information for the PowerPlay Early Power Estimator for Arria 10 User Guide* section with *Document Revision History*. • Added example messages to *Estimating Power Consumption While Creating the FPGA Design* and *PowerPlay EPE Input Fields* topics. • Added appendix, *Measuring Static Power*.
March 2015	2015.03.02	Initial release.

A. Measuring Static Power

Follow these steps to measure static power in your design.

1. Verify that the device is properly configured and in user mode. (CONF_DONE, NSTATUS, NCONFIG, and TSTPOR values should be high.)
2. Wait until a stable junction temperature (thermal equilibrium) is reached.
   - Use of a thermally controlled chamber is recommended.
   - You can measure the junction temperature of the FPGA using the on-chip temperature sensing diode (TSD). Refer to your device documentation for details on using the TSD. You could also measure the junction temperature with the TADC, but with reduced accuracy.
   - If a thermally controlled chamber is not available, use temperature feedback from the on-chip TSD or TADC to control a heatsink fan to achieve a desired junction temperature.
   - You can also use a heat gun to achieve a desired temperature; however, this method offers less thermal control.
3. Keep all inputs constant and do not toggle any I/Os. Do not toggle any clock signals (except for the clock to the TADC, if you are using the TADC to measure temperature.)
4. Depending on the board design, you can measure static current in one of several ways:
   - Use a regulator with the ability to measure voltage drop across a shunt resistor, and query the power measurement through the power management bus (PMBus)/system management bus (SMBus) interface.
   - If a regulator with PMBus/SMBus support is not available, you can measure the voltage drop across the shunt resistor manually for each power supply and calculate the current from the voltage drop.
   - If you use an external power supply, query the current measurement from the power supply according to the manufacturer's specifications.
5. If you want to isolate and understand the static power component of your design's total power consumption, take several current measurements across a range of temperatures and record the junction temperature of each measurement. Refer to the junction temperatures to corelate static power measurements with their corresponding total power measurements.
6. The silicon static power measurements can be compared with the static power estimate from the Power Analyzer report. Alternatively, data for your compiled design can be imported as a `.csv` file, into the Early Power Estimator for Arria 10 to obtain static power estimates for comparison. Ensure that you set the power characteristics in the Power Analyzer or Early Power Estimator to *Maximum*.