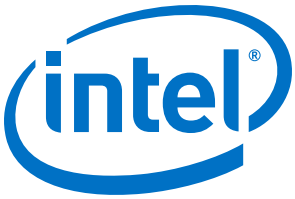

Low Latency 40-Gbps Ethernet Intel® Stratix® 10 IP Core User Guide

Updated for Intel® Quartus® Prime Design Suite: **20.3**

IP Version: **19.1.0**

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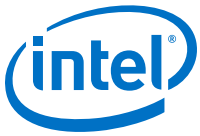


1. Datasheet

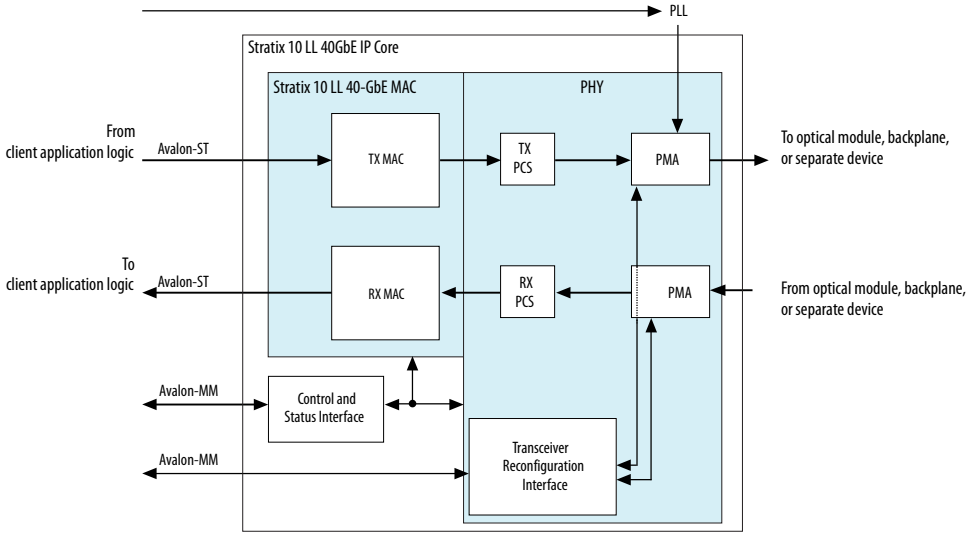
The Intel® Stratix® 10 Low Latency 40-Gbps Ethernet (LL 40GbE) IP core implements the *IEEE 802.3-2010 40G Ethernet Standard*. The IP core includes options to support unidirectional transport as defined in *Clause 66* of the *IEEE 802.3-2012 Ethernet Standard* and to support the *IEEE 802.3-2012 Backplane Ethernet Standard*.

The MAC client side interface for the Intel Stratix 10 LL 40GbE IP core is a 128-bit Avalon® streaming interface (Avalon-ST).

The IP core provides standard media access control (MAC), physical coding sublayer (PCS), and physical medium attachment (PMA) functions. The PHY comprises the PCS and PMA.

Figure 1. Intel Stratix 10 LL 40GbE Block Diagram

Main blocks, internal connections, and external block requirements.



1.1. Intel Stratix 10 LL 40GbE IP Core Supported Features

The Intel Stratix 10 LL 40GbE IP core supports the following features:

- Parameterizable through the IP Catalog available with the Intel Quartus® Prime Pro Edition software.
- Designed to the *IEEE 802.3ba-2010 High Speed Ethernet Standard* available on the IEEE website (www.ieee.org).
- Soft PCS logic that interfaces seamlessly to Intel FPGA 10.3125 gigabits per second (Gbps) serial transceivers.

- Standard XLAUI external interface consisting of FPGA hard serial transceiver lanes operating at 10.3125 Gbps.
- Supports 40GBASE-KR4/CR4 PHY and forward error correction (FEC) option for interfacing to backplanes. The option implements the *IEEE Backplane Ethernet Standard 802.3-2012*.
  - Supports option for auto-negotiation per Clause 73.
  - Supports option for link training per Clause 72.
  - Supports option for KR-FEC per Clause 74.
  - 40GBASE-KR4/CR4 PHY based on 64B/66B encoding with data striping and alignment markers to align data from multiple lanes.
- Supports Synchronous Ethernet (SyncE) by providing an optional CDR recovered clock output signal to the device fabric.
- Avalon Memory-Mapped (Avalon-MM) management interface to access the IP core control and status registers.
- Avalon-ST data path interface connects to client logic with the start of frame in the most significant byte (MSB). Interface has data width 128 bits.
- Support for jumbo packets, defined as packets greater than 1500 bytes.
- Receive (RX) CRC removal and pass-through control.
- Optional transmit (TX) CRC generation and insertion.
- RX CRC checking and error reporting.
- RX and TX preamble pass-through option for applications that require proprietary user management information transfer.
- Optional RX strict SFD checking per IEEE specification.
- RX malformed packet checking per IEEE specification.
- TX automatic frame padding to meet the 64-byte minimum Ethernet frame length.
- Received control frame type indication.
- Unidirectional transport as defined in *Clause 66 of the IEEE 802.3-2012 Ethernet Standard*
- Hardware and software reset control.
- MAC provides RX cut-through frame processing, no RX store-and-forward capability.
- Deficit idle counter (DIC) to maintain a 12-byte inter-packet gap (IPG) average.
- Optional fault signaling detects and reports local fault and generates remote fault, with *IEEE 802.3ba-2012 Ethernet Standard Clause 66* support.
- Optional access to Native PHY Debug Master Endpoint (NPDME) for serial link debugging.
- Programmable ready latency of 0 or 3 clock cycles for Avalon-ST TX interface.
- Optional statistics counters.

For a detailed specification of the Ethernet protocol refer to the *IEEE 802.3 Ethernet Standard*.

Related Information

IEEE website
The *IEEE 802.3 Ethernet Standard* is available on the IEEE website.

1.2. Intel Stratix 10 LL 40GbE Core Device Family and Speed Grade Support

1.2.1. Device Family Support

Table 1. Intel FPGA IP Core Device Support Levels

Device Support Level	Definition
Advance	The IP core is available for simulation and compilation for this device family. Timing models include initial engineering estimates of delays based on early post-layout information. The timing models are subject to change as silicon testing improves the correlation between the actual silicon and the timing models. You can use this IP core for system architecture and resource utilization studies, simulation, pinout, system latency assessments, basic timing assessments (pipeline budgeting), and I/O transfer strategy (datapath width, burst depth, I/O standards tradeoffs).
Preliminary	The IP core is verified with preliminary timing models for this device family. The IP core meets all functional requirements, but might still be undergoing timing analysis for the device family. It can be used in production designs with caution.
Final	The IP core is verified with final timing models for this device family. The IP core meets all functional and timing requirements for the device family and can be used in production designs.

Table 2. Intel Stratix 10 LL 40GbE IP Core Device Family Support

Shows the level of support offered by the Intel Stratix 10 LL 40GbE IP core for each Intel FPGA device family.

Device Family	Support
Intel Stratix 10	Advance
Other device families	No support

1.2.2. Intel Stratix 10 LL 40GbE IP Core Device Speed Grade Support

Table 3. Slowest Supported Device Speed Grades

IP Core	Device Family	Supported Speed Grades
Intel Stratix 10 LL 40GbE 40GBASE-KR4/CR4 variations	Intel Stratix 10	–2
Intel Stratix 10 LL 40GbE non-40GBASE-KR4/CR4 variations	Intel Stratix 10	–3

1.3. Resource Utilization

Resource utilization changes depending on the parameter settings you specify in the Intel Stratix 10 LL 40GbE parameter editor. For example, if you turn on statistics counters in the Intel Stratix 10 LL 40GbE parameter editor, the IP core requires additional resources to implement the additional functionality.

Table 4. IP Core Variation Encoding for Resource Utilization Table

IP core variations are named for easy comparison with the Arria 10 Low Latency 40GbE IP core. "On" indicates the parameter is turned on. The symbol "—" indicates the parameter is turned off or not available.

IP Core Variation / Parameter	A	B	C	E	F
Ready latency	0	0	3	3	3
Use external TX MAC PLL	On	On	—	—	—
Enable TX CRC insertion	—	On	On	On	On
Enable link fault generation	—	—	On	—	—
Enable preamble passthrough	—	—	On	—	—
Enable MAC stats counters	—	On	On	On	On
Enable KR4/CR4	—	—	—	On	On
Include FEC sublayer	—	—	—	—	On

Table 5. IP Core FPGA Resource Utilization

Lists the resources and expected performance for selected variations of the Intel Stratix 10 LL 40GbE IP core in a Stratix 10 device.

These results were obtained using the Quartus Prime Pro 17.1 Stratix 10 ES Editions software.

- The numbers of ALMs and logic registers are rounded up to the nearest 100.
- The numbers of ALMs, before rounding, are the **ALMs needed** numbers from the Quartus Prime Fitter Report.

IP Core Variation	ALMs	Dedicated Logic Registers	Memory M20K
A	7900	19100	1
B	11200	25500	1
C	12400	26900	1
E	17000	32800	11
F	17000	33200	11

Related Information

Intel Stratix 10 LL 40GbE IP Core Parameters on page 9
Information about the parameters and values in the IP core variations.

1.4. Release Information

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme. If an IP core version is not listed, the user guide for the previous IP core version applies.

The IP versioning scheme (X.Y.Z) number changes from one software version to another. A change in:

- X indicates a major revision of the IP. If you update your Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Table 6. Intel Stratix 10 LL 40GbE IP Core Current Release Information

Item	Description
IP Version	19.1.0
Intel Quartus Prime Version	19.3
Release Date	2019.09.27
Ordering Code	IP-40GEUMACPHY (IPR-40GEUMACPHY for renewal)

Related Information

Intel Stratix 10 Low Latency 40-Gbps Ethernet IP Core Release Information
Provides information about the new features and update for each IP release.

2. Intel Stratix 10 LL 40GbE IP Core Parameters

The Intel Stratix 10 LL 40GbE parameter editor has an **IP** tab with two subtabs, the **Main** tab and the **40GBASE-KR4/CR4** tab.

The Intel Stratix 10 LL 40GbE parameter editor also includes an **Example Design** tab. For information about that tab, refer to the *Intel Stratix 10 Low Latency 40G Ethernet Design Example User Guide*.

Table 7. Intel Stratix 10 LL 40GbE IP Core Parameters: Main Tab

Parameter	Range	Default Setting	Description
General			
Target transceiver tile	**H-Tile, L-tile**	The tile type of the Intel Quartus Prime project specific target device.	Specifies the transceiver tile on your target device. The Device setting of the Intel Quartus Prime project in which you generate the IP core determines the transceiver tile type. Unfortunately, at the time of publication (2017.05.08), the parameter editor displays a grayed-out listing of **H-Tile** in all cases. You can ignore this display; the IP core you generate does in fact target the correct transceiver tile type for your target Intel Stratix 10 device.
Protocol speed	**40GbE**	**40GbE**	Selects the Ethernet data rate.
Ready latency	**0**, **3**	**0**	Selects the readyLatency value on the TX client interface. readyLatency is an Avalon streaming interface property that defines the number of clock cycles of delay from when the IP core asserts the `l2_tx_ready` signal to the clock cycle in which the IP core can accept data on the TX client interface. Refer to the *Avalon Interface Specifications*. Selecting a latency of 3 eases timing closure at the expense of increased latency for the TX datapath.
PCS/PMA Options			
Use external TX MAC PLL	**Enabled**, **Disabled**	**Disabled**	When enabled, the IP core is configured to expect an input clock to drive the TX MAC. The input clock signal is `clk_txmac_in`.
Enable SyncE	**Enabled**, **Disabled**	**Disabled**	Exposes the RX recovered clock as an output signal. This feature supports the Synchronous Ethernet standard described in the International Telecommunication Union (ITU) Telecommunication Standardization Sector (ITU-T) G.8261, G.8262, and G.8264 recommendations.
PHY reference frequency	**322.265625 MHz**, **644.53125 MHz**	**644.53125 MHz**	Sets the expected incoming PHY `clk_ref` reference frequency. The input clock frequency must match the frequency you specify for this parameter (±100ppm).

continued...

Parameter	Range	Default Setting	Description
VCCR_GXB and VCCT_GXB supply voltage for the transceiver	**1_0V**, **1_1V**	**1_0V**	Specifies whether the transceiver supply voltage is 1.0 V or 1.1 V. The supply voltage must match the voltage you specify for this parameter.
MAC Options			
Enable TX CRC insertion	**Enabled**, **Disabled**	**Enabled**	When enabled, TX MAC computes and inserts the CRC-32 checksum in the out-going Ethernet frame. When disabled, the TX MAC does not compute a 32-bit FCS in the TX MAC frame. Instead, the client must provide frames with at least 64 bytes, plus the Frame Check Sequence (FCS).
Enable link fault generation	**Enabled**, **Disabled**	**Disabled**	When enabled, the IP core implements link fault signaling as defined in the *IEEE 802.3-2012 IEEE Ethernet Standard*. The MAC includes a Reconciliation Sublayer (RS) to manage local and remote faults. When enabled, the local RS TX logic can transmit remote fault sequences in case of a local fault and can transmit IDLE control words in case of a remote fault.
Enable preamble passthrough	**Enabled**, **Disabled**	**Disabled**	When enabled, the IP core is in RX and TX preamble pass-through mode. In RX preamble pass-through mode, the IP core passes the preamble and Start Frame Delimiter (SFD) to the client instead of stripping them out of the Ethernet packet. In TX preamble pass-through mode, the client specifies the preamble and provides the SFD to be sent in the Ethernet frame.
Enable MAC stats counters	**Enabled**, **Disabled**	**Enabled**	When enabled, the IP core includes statistics counters that characterize TX and RX traffic. The statistics module also supports shadow requests that verify counts by taking snapshots of intermediate results.
Enable Strict SFD check	**Enabled**, **Disabled**	**Disabled**	When enabled, the IP core can implement strict SFD checking, depending on register settings.
Flow Control Options			
Enable MAC flow control	**Enabled**, **Disabled**	**Disabled**	When enabled, the IP core implements flow control. When either link partner experiences congestion, the respective transmit control sends pause frames.
Number of queues in priority flow control	1-8	8	Specifies the number of queues used in managing flow control.
Configuration, Debug and Extension Options			
Enable Native PHY Debug Master Endpoint (NPDME)	**Enabled**, **Disabled**	**Disabled**	If enabled, the IP core turns on the following features in the Native PHY IP core that is included in the Intel Stratix 10 LL 40GbE IP core: • **Enable Native PHY Debug Master Endpoint (NPDME)** • **Enable capability registers** If turned off, the IP core is configured without these features. For information about these Intel Stratix 10 features, refer to the *Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide*.
Enable JTAG to Avalon Master Bridge	**Enabled**, **Disabled**	**Disabled**	If turned on, the IP core includes a JTAG to Avalon memory-mapped interface master bridge connecting internally to status and reconfiguration registers. This allows you to run the Ethernet Link Inspector using the System Console.

Table 8. Intel Stratix 10 LL 40GbE IP Core Parameters: 40GBASE-KR4/CR4 Tab

Parameter	Range	Default Setting	Description
KR4/CR4 General Options			
Enable KR4/CR4	• True • False	False	If this parameter is turned on, the IP core is a 40GBASE-KR4/CR4 variation. If this parameter is turned off, the IP core is not a 40GBASE-KR4/CR4 variation, and the other parameters on this tab are not available. *Note:* At the time of publication (2017.05.08), the Quartus Prime Pro 17.1 Stratix 10 ES Editions software does not provide hardware support for 40GBASE-KR4/CR4 variations of this IP core. The SRAM Object File (`.sof`) you generate for these variations does not function correctly in hardware. However, you can generate, simulate, and compile these variations.
Status clock rate	100.0–161.0 MHz	100.0 MHz	Sets the expected incoming `clk_status` frequency. The input clock frequency must match the frequency you specify for this parameter. The IP core is configured with this information: • To ensure the IP core measures the link fail inhibit time accurately. Determines the value of the Link Fail Inhibit timer (IEEE 802.3 clause 73.10.2) correctly. • If `clk_status` frequency is not 100 MHz, to adjust the PHY clock monitors to report accurate frequency information. This parameter determines the **PHY Management clock (MGMT_CLK) frequency in MHz** parameter of the underlying 10GBASE-KR PHY IP core. However, the default value of the **Status clock rate** parameter is not identical to the default value of the PHY IP core **PHY Management clock (MGMT_CLK) frequency in MHz** parameter.
Auto-Negotiation			
Enable Auto-Negotiation	• True • False	False	If this parameter is turned on, the IP core includes logic to implement auto-negotiation as defined in Clause 73 of *IEEE Std 802.3–2012*. If this parameter is turned off, the IP core does not include auto-negotiation logic and cannot perform auto-negotiation. Currently the IP core can only negotiate to KR4 mode.
Link fail inhibit time for 40Gb Ethernet	500–510 ms	504 ms	Specifies the time before link status is set to FAIL or OK. A link fails if the time duration specified by this parameter expires before link status is set to OK. For more information, refer to *Clause 73 Auto-Negotiation for Backplane Ethernet* in *IEEE Standard 802.3–2012*. The 40GBASE-KR4 IP core asserts the `rx_pcs_ready` signal to indicate link status is OK.
Enable 40GBASE-CR4 Technology Ability	• True • False	False	If this parameter is turned on, the IP core advertises CR-4 capability. If this parameter is turned off, but auto-negotiation is turned on, the IP core advertises KR-4 capability.
Auto-Negotiation Master	• Lane 0 • Lane 1 • Lane 2 • Lane 3	Lane 0	Selects the master channel for auto-negotiation.
Pause ability–C0	• True • False	True	If this parameter is turned on, the IP core indicates on the Ethernet link that it supports symmetric pauses as defined in *Annex 28B* of Section 2 of *IEEE Std 802.3–2008*.
Pause ability–C1	• True • False	True	If this parameter is turned on, the IP core indicates on the Ethernet link that it supports asymmetric pauses as defined in *Annex 28B* of Section 2 of *IEEE Std 802.3–2008*.
Link Training: General			

continued...

Parameter	Range	Default Setting	Description
Enable Link Training	• True • False	True	If this parameter is turned on, the IP core includes the link training module, which configures the remote link partner TX PMD for the lowest Bit Error Rate (BER). LT is defined in Clause 72 of *IEEE Std 802.3–2012*.
Maximum bit error count	$2^n - 1$ for n an integer in the range 4–10.	511	Specifies the maximum number of errors on a lane before the `Link Training Error` bit (40GBASE-KR4 register offset 0xD2, bit 4, 12, 20, or 28, depending on the lane) is set, indicating an unacceptable bit error rate. n is the width of the Bit Error Counter that is configured in the IP core. The value to which you set this parameter determines n, and thus the width of the Bit Error Counter. Because the default value of this parameter is 511, the default width of the Bit Error Counter is 10 bits. You can use this parameter to tune PMA settings. For example, if you see no difference in error rates between two different sets of PMA settings, you can increase the width of the bit error counter to determine if a larger counter enables you to distinguish between PMA settings.
Number of frames to send before sending actual data	• 127 • 255	127	Specifies the number of additional training frames the local link partner delivers to ensure that the link partner can correctly detect the local receiver state. This number is the value of `wait_timer` as specified in Clause 72.6.10.3.2 of *IEEE Std 802.3–2012*
Link Training: PMA Parameters			
VMAXRULE	0–31	30	Specifies the maximum V_{OD}.
VMINRULE	0–31	6	Specifies the minimum V_{OD}.
VODMINRULE	0–31	14	Specifies the minimum V_{OD} for the first tap.
VPOSTRULE	0–25	25	Specifies the maximum value that the internal algorithm for pre-emphasis ever tests in determining the optimum post-tap setting.
VPRERULE	0–16	16	Specifies the maximum value that the internal algorithm for pre-emphasis ever tests in determining the optimum pre-tap setting.
PREMAINVAL	0–31	30	Specifies the Preset V_{OD} value. This value is set by the Preset command of the link training protocol, defined in Clause 72.6.10.2.3.1 of *IEEE Std 802.3–2012*. *Note:* The default value is subject to change in future software releases.
PREPOSTVAL	0–31	0	Specifies the preset Post-tap value.
PREPREVAL	0–15	0	Specifies the preset Pre-tap value.
INITMAINVAL	0–31	25	Specifies the initial V_{OD} value. This value is set by the Initialize command of the link training protocol, defined in Clause 72.6.10.2.3.2 of *IEEE Std 802.3–2012*. *Note:* The default value is subject to change in future software releases.
INITPOSTVAL	0–25	13	Specifies the initial and reset Post-tap value. *Note:* The default value is subject to change in future software releases.
INITPREVAL	0–16	3	Specifies the initial and reset Pre-tap value. *Note:* The default value is subject to change in future software releases.
FEC Options			

continued...

Parameter	Range	Default Setting	Description
Include FEC sublayer	• True • False	False	If this parameter is turned on, the IP core includes logic to implement FEC.
Set FEC_Ability bit on power up or reset	• True • False	False	If this parameter is turned on, the IP core sets the FEC ability bit (40GBASE-KR4 register offset 0xB0, bit 16: `Assert KR FEC enable`) on power up and reset. This parameter is available if you turn on **Include FEC sublayer**.
Set FEC_Enable bit on power up or reset	• True • False	False	If this parameter is turned on, the IP core sets the FEC enable bit (40GBASE-KR4 register offset 0xB0, bit 18: `Assert KR FEC request`) on power up and reset. If you turn on this parameter but do not turn on **Set FEC_ability bit on power up or reset**, this parameter has no effect: the IP core cannot specify the value of 1 for FEC Requested without specifying the value of 1 for FEC Ability. This parameter is available if you turn on **Include FEC sublayer**.

Related Information

- Intel Stratix 10 Low Latency 40G Ethernet Design Example User Guide
  Information about the parameters on the **Example Design** tab.
- Avalon Interface Specifications
  Detailed information about Avalon streaming interfaces and the Avalon streaming interface readyLatency parameter.
- Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide
  Information about the **NPDME** and **Enable capability registers** parameters of the Intel Stratix 10 H-Tile Transceiver PHY IP core.

3. Getting Started

3.1. Installing and Licensing Intel FPGA IP Cores

The Intel Quartus Prime software installation includes the Intel FPGA IP library. This library provides many useful IP cores for your production use without the need for an additional license. Some Intel FPGA IP cores require purchase of a separate license for production use. The Intel FPGA IP Evaluation Mode allows you to evaluate these licensed Intel FPGA IP cores in simulation and hardware, before deciding to purchase a full production IP core license. You only need to purchase a full production license for licensed Intel IP cores after you complete hardware testing and are ready to use the IP in production.

The Intel Quartus Prime software installs IP cores in the following locations by default:

Figure 2. IP Core Installation Path

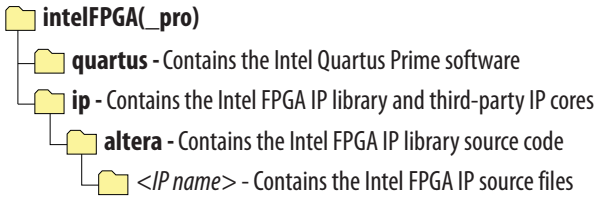


Table 9. IP Core Installation Locations

Location	Software	Platform
`<drive>:\intelFPGA_pro\quartus\ip\altera`	Intel Quartus Prime Pro Edition	Windows*
`<drive>:\intelFPGA\quartus\ip\altera`	Intel Quartus Prime Standard Edition	Windows
`<home directory>:/intelFPGA_pro/quartus/ip/altera`	Intel Quartus Prime Pro Edition	Linux*
`<home directory>:/intelFPGA/quartus/ip/altera`	Intel Quartus Prime Standard Edition	Linux

Note: The Intel Quartus Prime software does not support spaces in the installation path.

3.2. Specifying the Intel Stratix 10 LL 40GbE IP Core Parameters and Options

The Intel Stratix 10 LL 40GbE parameter editor allows you to quickly configure your custom IP variation. Use the following steps to specify IP core options and parameters in the Intel Quartus Prime Pro Edition software.

1. In the Intel Quartus Prime Pro Edition, click **File ➤ New Project Wizard** to create a new Intel Quartus Prime project, or **File ➤ Open Project** to open an existing Intel Quartus Prime project. The wizard prompts you to specify a device.
2. In the IP Catalog (**Tools ➤ IP Catalog**), locate and double-click the name of the IP core to customize. The New IP Variation window appears.
3. Specify a top-level name for your custom IP variation. The parameter editor saves the IP variation settings in a file named *<your_ip>*`.ip`.
4. Click **OK**. The parameter editor appears.
5. On the **IP** and **40GBASE-KR4/CR4** tabs, specify the parameters for your IP core variation. Refer to Intel Stratix 10 LL 40GbE IP Core Parameters on page 9 for information about specific IP core parameters.
6. Optionally, to generate a simulation testbench or compilation and hardware design example, follow the instructions in the *Intel Stratix 10 Low Latency 40G Ethernet Design Example User Guide*.
7. Click **Generate HDL**. The **Generation** dialog box appears.
8. Specify output file generation options, and then click **Generate**. The IP variation files generate according to your specifications.
9. Click **Finish**. The parameter editor adds the top-level `.ip` file to the current project automatically. If you are prompted to manually add the `.ip` file to the project, click **Project ➤ Add/Remove Files in Project** to add the file.
10. After generating and instantiating your IP variation, make appropriate pin assignments to connect ports.

Related Information

Intel Stratix 10 Low Latency 40G Ethernet Design Example User Guide

3.3. Simulating the IP Core

You can simulate your IP core variation with the functional simulation model and the testbench generated with the IP core. The functional simulation model is a cycle-accurate model that allows for fast functional simulation of your IP core instance using industry-standard Verilog HDL simulators. If your IP core variation does not generate a matching testbench, you can create your own testbench to exercise the IP core functional simulation model.

The functional simulation model and testbench files are generated in project subdirectories. These directories also include scripts to compile and run the example design.

Note: Use the simulation models only for simulation and not for synthesis or any other purposes. Using these models for synthesis creates a nonfunctional design.

In the top-level wrapper file for your simulation project, you can set the following RTL parameters to enable simulation optimization. These optimizations significantly decrease the time to reach link initialization.

- SIM_SHORT_RST: Shortens the reset times to speed up simulation.
- SIM_SHORT_AM: Shortens the interval between alignment markers to accelerate alignment marker lock. Alignment markers are used when Reed-Solomon FEC is enabled.

In the top-level wrapper file for your 40GBASE-KR4/CR4 IP core simulation model, you can define the ALTERA_RESERVED_XCVR_FULL_KR_TIMERS RTL parameter. Defining this parameter directs the simulation model to exercise full auto-negotiation and link training functionality if enabled. By default, the parameter is undefined and simulation shortens auto-negotiation and link training. The Intel-provided testbench does not define this parameter.

In general, parameters are set through the IP core parameter editor and you should not change them manually. The only exceptions are these simulation parameters.

To set the simulation optimization parameters on the PHY blocks, add the following lines to the top-level wrapper file:

```
defparam <dut instance>.SIM_SHORT_RST = 1'b1;
defparam <dut instance>.SIM_SHORT_AM = 1'b1;
```

Note: You can use the example testbench as a guide for setting the simulation parameters in your own simulation environment. These lines are already present in the Intel-provided testbench for the IP core.

Related Information

- Simulating Intel FPGA IP Cores
- Intel Stratix 10 Low Latency 40G Ethernet Design Example User Guide
  Describes the Intel Stratix 10 LL 40GbE testbench and design example and how to simulate the testbench.

3.4. Generated File Structure

The Intel Quartus Prime Pro Edition software generates the following output files for Low Latency 40-Gbps Ethernet Intel Stratix 10 IP Core. .

Figure 3. IP Core Generated Files

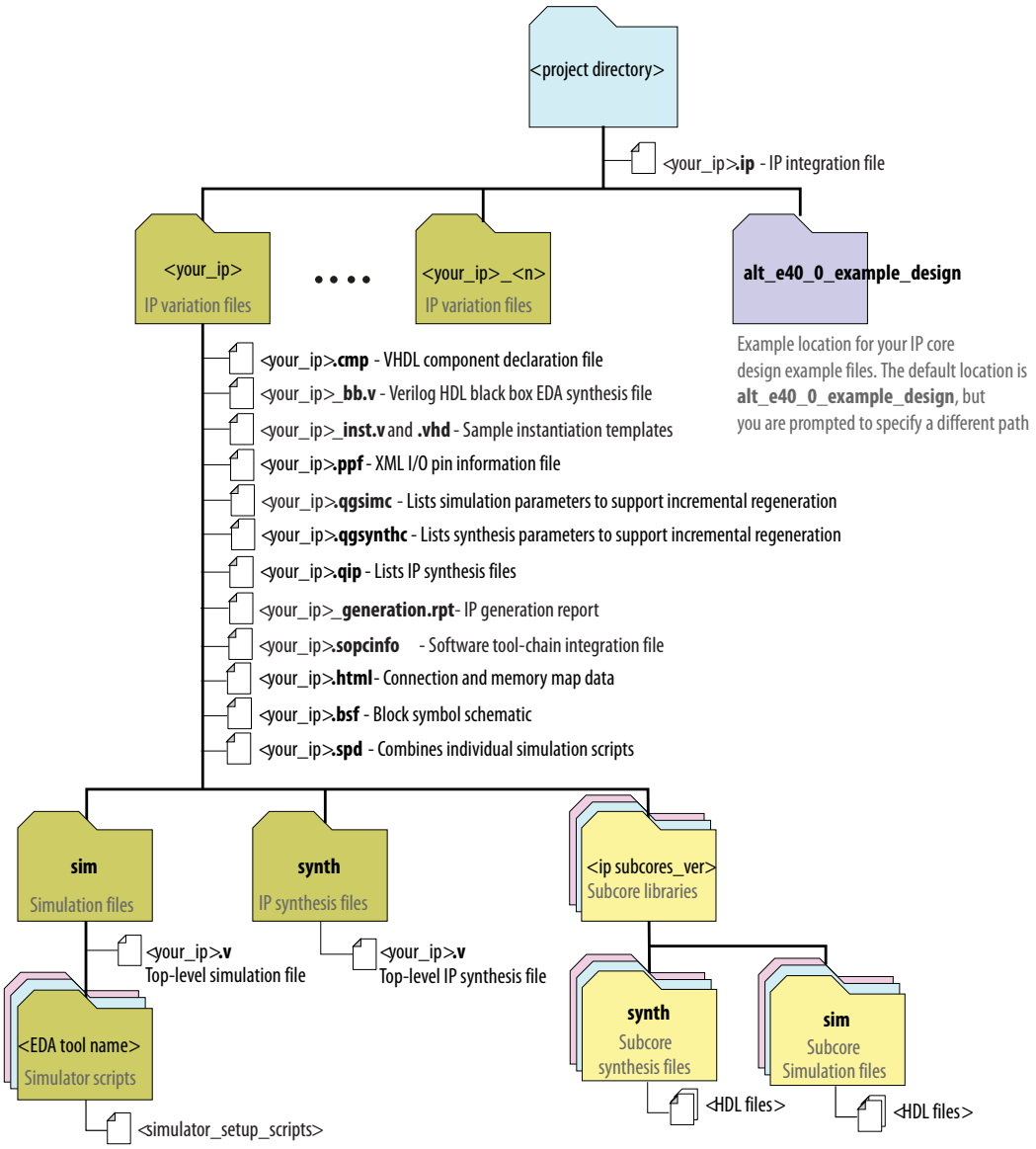


Table 10. IP Core Generated Files

File Name	Description
<*your_ip*>.ip	The Platform Designer (Standard) system or top-level IP variation file. <*your_ip*> is the name that you give your IP variation.
<*your_ip*>.cmp	The VHDL Component Declaration (**.cmp**) file is a text file that contains local generic and port definitions that you can use in VHDL design files. This IP core does not support VHDL. However, the Intel Quartus Prime Pro Edition generates this file.
<*your_ip*>.html	A report that contains connection information, a memory map showing the address of each slave with respect to each master to which it is connected, and parameter assignments.

continued...

File Name	Description
<*your_ip*>_generation.rpt	IP or Platform Designer (Standard) generation log file. A summary of the messages during IP generation.
<*your_ip*>.qgsimc	Lists simulation parameters to support incremental regeneration.
<*your_ip*>.qgsynthc	Lists synthesis parameters to support incremental regeneration.
<*your_ip*>.qip	Contains all the required information about the IP component to integrate and compile the IP component in the Intel Quartus Prime Pro Edition software.
<*your_ip*>.csv	Contains information about the upgrade status of the IP component.
<*your_ip*>.bsf	A Block Symbol File (.**bsf**) representation of the IP variation for use in Intel Quartus Prime Block Diagram Files (**.bdf**).
<*your_ip*>.spd	Required input file for `ip-make-simscript` to generate simulation scripts for supported simulators. The **.spd** file contains a list of files generated for simulation, along with information about memories that you can initialize.
<*your_ip*>.ppf	The Pin Planner File (**.ppf**) stores the port and node assignments for IP components created for use with the Pin Planner.
<*your_ip*>_bb.v	You can use the Verilog black-box (**_bb.v**) file as an empty module declaration for use as a black box.
<*your_ip*>_inst.v and _inst.vhd	HDL example instantiation template. You can copy and paste the contents of this file into your HDL file to instantiate the IP variation. This IP core does not support VHDL. However, the Intel Quartus Prime Pro Edition generates the `_inst.vhd` file.
<*your_ip*>.regmap	If IP contains register information, **.regmap** file generates. The **.regmap** file describes the register map information of master and slave interfaces. This enables register display views and user customizable statistics in the System Console.
<*your_ip*>.svd	Allows hard processor system (HPS) System Debug tools to view the register maps of peripherals connected to HPS within a Platform Designer (Standard) system. During synthesis, the **.svd** files for slave interfaces visible to System Console masters are stored in the **.sof** file in the debug section. System Console reads this section, which Platform Designer (Standard) can query for register map information. For system slaves, Platform Designer (Standard) can access the registers by name.
<*your_ip*>.v	HDL files that instantiate each submodule or child IP core for synthesis or simulation.
mentor/	Contains a ModelSim* script `msim_setup.tcl` to set up and run a simulation.
aldec/	Contains a Riviera-PRO script `rivierapro_setup.tcl` to setup and run a simulation. This IP core does not support simulation with the Aldec Riviera-PRO simulator. However, the Intel Quartus Prime Pro Edition generates this directory.
synopsys/vcs/ synopsys/vcsmx/	Contains a shell script `vcs_setup.sh` to set up and run a VCS* simulation. Contains a shell script `vcsmx_setup.sh` and `synopsys_ sim.setup` file to set up and run a VCS MX simulation.
cadence/	Contains a shell script `ncsim_setup.sh` and other setup files to set up and run an NCSIM simulation.
submodules/	Contains HDL files for the IP core submodule.
<*child IP cores*>/	For each generated child IP core directory, Platform Designer (Standard) generates `synth/` and `sim/` sub-directories.

For information about the file structure of the design example, refer to the *Intel Stratix 10 Low Latency 40G Ethernet Design Example User Guide*.

Related Information

Intel Stratix 10 Low Latency 40G Ethernet Design Example User Guide
Information about the Intel Stratix 10 LL 40GbE design example file structure.

3.5. Integrating Your IP Core in Your Design

3.5.1. Pin Assignments

When you integrate your Intel Stratix 10 LL 40GbE core instance in your design, you must make appropriate pin assignments. While compiling the IP core alone, you can create virtual pins to avoid making specific pin assignments for top-level signals. When you are ready to map the design to hardware, you can change to the correct pin assignments.

Related Information

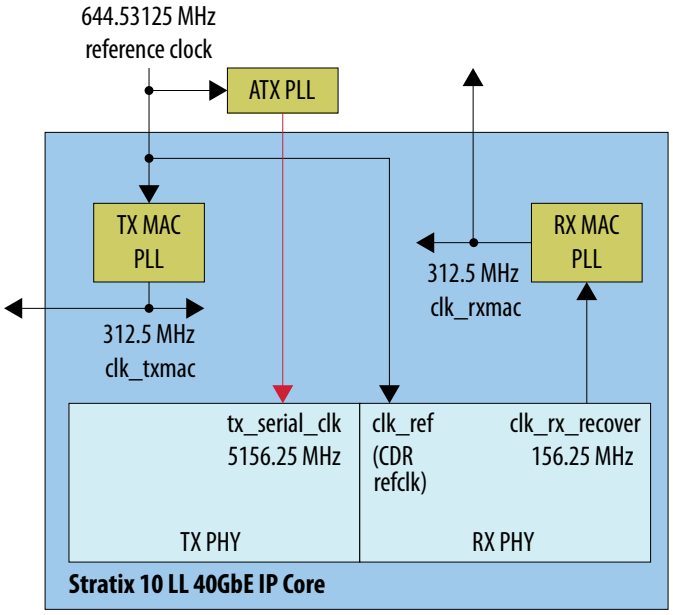
Intel Quartus Prime Help
For information about the Intel Quartus Prime software, including virtual pins.

3.5.2. Adding the Transceiver PLL

Intel Stratix 10 LL 40GbE IP cores require an external PLL to drive the TX transceiver serial clock, in order to compile and to function correctly in hardware. In many cases, the same PLL can be shared with other transceivers in your design.

Figure 4. PLL Configuration Example

The TX transceiver PLL is instantiated with an Intel FPGA ATX PLL IP core. The TX transceiver PLL must always be instantiated outside the Intel Stratix 10 LL 40GbE IP core.



You can use the IP Catalog to create a transceiver PLL.

- Select **Stratix 10 Transceiver ATX PLL**.
- In the parameter editor, set the following parameter values:
  - **PLL output frequency** to **5156.25 MHz**. The transceiver performs dual edge clocking, using both the rising and falling edges of the input clock from the PLL. Therefore, this PLL output frequency setting supports a 10.3125 Gbps data rate through the transceiver.
  - **PLL integer reference clock frequency** to **644.53125** MHz.

You must connect the `tx_serial_clk` input pin of the Intel Stratix 10 LL 40GbE IP core PHY link to the output port of the ATX PLL.

3.5.3. Clock Requirements for 40GBASE-KR4/CR4 Variations

In 40GBASE-KR4/CR4 IP core designs, you must drive the clocks for the two IP core register interfaces (`reconfig_clk` and `clk_status`) from the same clock source.

3.5.4. Adding the External TX MAC PLL

If you turn on **Use external TX MAC PLL** in the Intel Stratix 10 LL 40GbE parameter editor, you must connect the `clk_txmac_in` input port to a clock source, usually a PLL on the device.

The `clk_txmac_in` signal drives the `clk_txmac` clock in the IP core TX MAC and PHY. If you turn off this parameter, the `clk_txmac_in` input clock signal is not available.

The required TX MAC clock frequency is 312.5 MHz. User logic must drive `clk_txmac_in` from a PLL whose input is the PHY reference clock, `clk_ref`.

3.5.5. Placement Settings for the Intel Stratix 10 LL 40GbE Core

The Quartus Prime software provides the options to specify design partitions and Logic Lock (Standard) or Logic Lock regions for incremental compilation, to control placement on the device. To achieve timing closure for your design, you might need to provide floorplan guidelines using one or both of these features.

The appropriate floorplan is always design-specific, and depends on your design.

Related Information

Intel Quartus Prime Pro Edition User Guide: Design Constraints
Describes incremental compilation, design partitions, and Logic Lock regions.

3.6. Intel Stratix 10 LL 40GbE IP Core Testbench

Intel provides a compilation-only example design and a testbench with most variations of the Intel Stratix 10 LL 40GbE IP core.

To generate the testbench, you must first set the parameter values for the IP core variation you intend to generate. If you do not set the parameter values identically, the testbench you generate might not exercise the IP core variation you generate. If your IP core variation does not meet the criteria for a testbench, the generation process does not create a testbench.

3.6.1. Understanding the Testbench Behavior

The testbenches send traffic through the IP core in transmit-to-receive loopback mode, exercising the transmit side and receive side of the IP core in the same data flow. These testbenches send traffic to allow the Ethernet lanes to lock, and then send packets to the transmit client data interface and check the data as it returns through the receive client data interface.

The Intel Stratix 10 LL 40GbE IP core implements virtual lanes as defined in the *IEEE 802.3ba-2012 Ethernet Standard*. The IP core is fixed at four virtual lanes; the four virtual lanes are typically transmitted over four 10 Gbps physical lanes. When the lanes arrive at the receiver the lane streams are in an undefined order. Each lane carries a periodic PCS-VLANE alignment tag to restore the original ordering. The simulation establishes a random permutation of the physical lanes that is used for the remainder of the simulation.

Within each virtual lane stream, the data is 64B/66B encoded. Each word has two framing bits which are always either 01 or 10, never 00 or 11. The RX logic uses this pattern to lock onto the correct word boundaries in each serial stream. The process is probabilistic due to false locks on the pseudo-random scrambled stream.

Both the word lock and the alignment marker lock implement hysteresis as defined in the *IEEE Standard for Ethernet, Section 4*. Multiple successes are required to acquire lock and multiple failures are required to lose lock. The "fully locked" messages in the simulation log indicate the point at which a physical lane has successfully identified the word boundary and virtual lane assignment.

In the event of a catastrophic error, the RX PCS automatically attempts to reacquire alignment. The MAC properly identifies errors in the datastream.

3.7. Compiling the Full Design and Programming the FPGA

You can use the **Start Compilation** command on the Processing menu in the Intel Quartus Prime software to compile your design. After successfully compiling your design, program the targeted Intel FPGA with the Programmer and verify the design in hardware.

Note: The Intel Stratix 10 LL 40GbE core design example synthesis directories include Synopsys Constraint (`.sdc`) files that you can copy and modify for your own design.

Related Information

- Incremental Compilation for Hierarchical and Team-Based Design
- Programming Intel Devices

- Stratix 10 Low Latency 40G Ethernet Design Example User Guide
  Information about generating the design example and the design example directory structure.

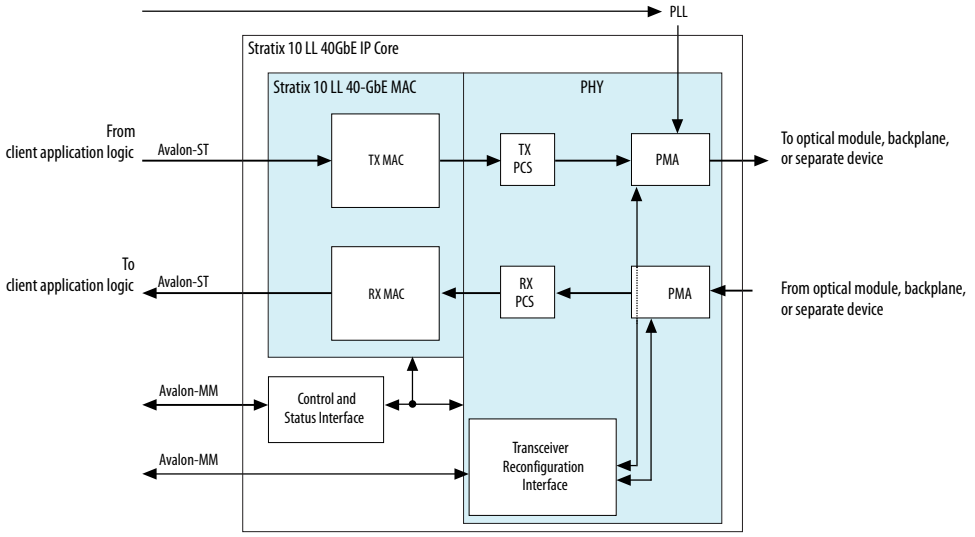
4. Functional Description

4.1. Intel Stratix 10 LL 40GbE Core Functional Description

The Intel Stratix 10 LL 40GbE core implements an Ethernet MAC in accordance with the *IEEE 802.3 Ethernet Standard*. The IP core implements an Ethernet PCS and PMA (PHY) that handles the frame encapsulation and flow of data between a client logic and Ethernet network.

Figure 5. Intel Stratix 10 LL 40GbE Core Block Diagram

Main blocks, internal connections, and external block requirements.



In the TX direction, the MAC assembles packets and sends them to the PHY. It completes the following tasks:

- Accepts client frames.
- Inserts the inter-packet gap (IPG), preamble, start of frame delimiter (SFD), and padding. The source of the preamble and SFD depends on whether the IP core is in preamble-pass-through mode.
- Adds the CRC bits if enabled.
- Updates statistics counters if enabled.

In the RX direction, the PMA passes frames to the PCS that sends them to the MAC. The MAC completes the following tasks:

- Performs CRC and malformed packet checks.
- Updates statistics counters if enabled.
- Strips out the CRC, preamble, and SFD.
- Passes the remainder of the frame to the client.

In preamble pass-through mode, the MAC passes on the preamble and SFD to the client instead of stripping them out. In RX CRC pass-through mode, the MAC passes on the CRC bytes to the client and asserts the end-of-packet signal in the same clock cycle as the final CRC byte.

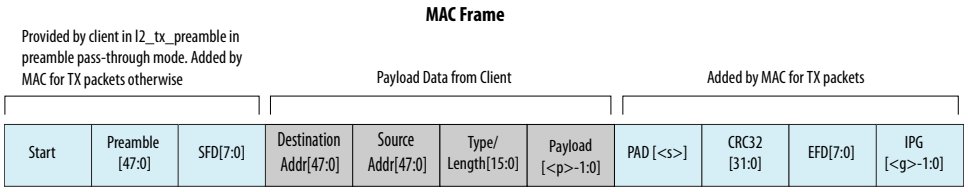
4.1.1. Intel Stratix 10 LL 40GbE Core TX MAC Datapath

The TX MAC module receives the client payload data with the destination and source addresses. It then adds, appends, or updates various header fields in accordance with the configuration specified. The MAC does not modify the destination address, the source address, or the payload received from the client. However, the TX MAC module adds a preamble, if the IP core is not configured to receive the preamble from user logic. It pads the payload of frames greater than eight bytes to satisfy the minimum Ethernet frame payload of 46 bytes. By default, the MAC inserts the CRC bytes. The TX MAC module inserts IDLE bytes to maintain an average IPG of 12.

Figure 6. Typical Client Frame at the Transmit Interface

Illustrates the changes that the TX MAC makes to the client frame. This figure uses the following notational conventions:

- <*p*> = payload size, which is arbitrarily large
- <*s*> = number of padding bytes (0–46)
- <*g*> = number of IPG bytes



4.1.1.1. Frame Padding

When the length of the client frame is less than 64 bytes, the TX MAC module inserts pad bytes (0x00) after the payload to create a frame length equal to the minimum size of 64 bytes (including CRC).

The IP core filters out all client frames with lengths less than 9 bytes.

4.1.1.2. Preamble Insertion

In the TX datapath the MAC prepends an eight-byte preamble to the client frame. If you turn on **Enable link fault generation**, this MAC module also incorporates the functions of the reconciliation sublayer (RS).

The source of the 7-byte preamble (including a Start byte) and 1-byte SFD depends on whether you turn on **Enable preamble passthrough** in the parameter editor.

If the preamble pass-through feature is enabled, the client provides the eight-byte preamble (comprising seven bytes of preamble, and final 1-byte SFD) on a dedicated preamble bus, `l2_tx_preamble[63:0]`. In this case, the client is responsible for providing the correct Start byte (0xFB) and an appropriate SFD byte. If the preamble pass-through feature is disabled, the MAC inserts the standard Ethernet preamble in the transmitted Ethernet frame.

When `l2_tx_startofpacket` is asserted, `l2_tx_preamble[63:0]` contains the preamble data and `l2_tx_data[127:0]` contains the first 16 bytes of frame data, starting from destination address.

Note that a single parameter in the Intel Stratix 10 LL 40GbE parameter editor turns on both RX and TX preamble passthrough.

4.1.1.3. Inter-Packet Gap Generation and Insertion

The TX MAC maintains the minimum inter-packet gap (IPG) between transmitted frames required by the IEEE 802.3 Ethernet standard. The deficit idle counter (DIC) maintains the average IPG of 12 bytes.

4.1.1.4. Frame Check Sequence (CRC-32) Insertion

The TX MAC computes and inserts a CRC32 checksum in the transmitted MAC frame. The frame check sequence (FCS) field contains a 32-bit CRC value. The MAC computes the CRC32 over the frame bytes that include the source address, destination address, length, data, and pad (if applicable). The CRC checksum computation excludes the preamble, SFD, and FCS. The encoding is defined by the following generating polynomial:

```
FCS(X) = X32 +X26 +X23 +X22 +X16 +X12 +X11 +X10 +X8 +X7 +X5 +X4 +X2 +X1 +1
```

CRC bits are transmitted with MSB (X32) first.

You can configure your IP core TX MAC to implement TX CRC insertion or not, by turning **Enable TX CRC insertion** on or off in the IP core parameter editor. By default, the CRC insertion feature is enabled.

4.1.2. Intel Stratix 10 LL 40GbE Core RX MAC Datapath

The RX MAC receives Ethernet frames and forwards the payload with relevant header bytes to the client after performing some MAC functions on header bytes. The RX MAC processes all incoming valid frames.

Figure 7. Flow of Client Frame With Preamble Pass-Through Turned On

This figure uses the following notational conventions:

- <*p*> = payload size, which is arbitrarily large.
- <*s*> = number of padding bytes (0–46).

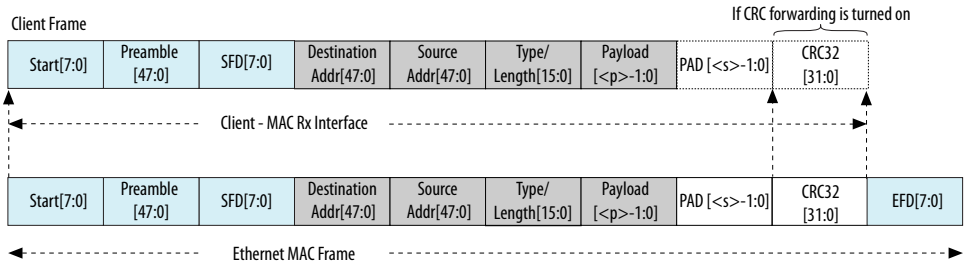
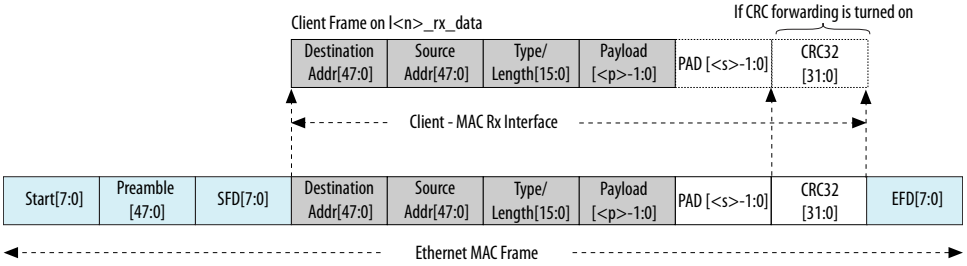


Figure 8. Flow of Client Frame With Preamble Pass-Through Turned Off

This figure uses the following notational conventions:

- <*p*> = payload size, which is arbitrarily large.
- <*s*> = number of padding bytes (0–46).



4.1.2.1. IP Core Preamble Processing

If you turn on **Enable preamble passthrough** in the parameter editor, the RX MAC forwards preamble bytes. The TX MAC requires the preamble bytes to be included in the frames at the Avalon Streaming interface.

If you turn off **Enable preamble passthrough**, the IP core removes the preamble bytes. `l2_rx_startofpacket` is aligned to the MSB of the destination address.

Note that a single parameter in the Intel Stratix 10 LL 40GbE parameter editor turns on both RX and TX preamble passthrough.

4.1.2.2. IP Core Strict SFD Checking

The Intel Stratix 10 LL 40GbE core RX MAC checks all incoming packets for a correct Start byte (0xFB). If you turn on **Enable Strict SFD check** in the Intel Stratix 10 LL 40GbE parameter editor, you enable the RX MAC to check the incoming preamble and SFD for the following values:

- SFD = 0xD5
- Preamble = 0x555555555555

The RX MAC checks one or both of these values depending on the values in bits [4:3] of the RXMAC_CONTROL register at offset 0x50A.

Table 11. Strict SFD Checking Configuration

Enable Strict SFD check	0x50A[4]: Preamble Check	0x50A[3]: SFD Check	Fields Checked	Behavior if Check Fails
Off	Don't Care	Don't Care	Start byte	IP core does not recognize a malformed Start byte as a Start byte
On	0	0	Start byte	
	0	1	Start byte and SFD	IP Core drops the packet
	1	0	Start byte and preamble	
	1	1	Start byte and preamble and SFD	

4.1.2.3. Length/Type Field Processing

This two-byte header represents either the length of the payload or the type of MAC frame.

- Length/type < 0x600—The field represents the payload length of a basic Ethernet frame. The MAC RX continues to check the frame and payload lengths.
- Length/type >= 0x600—The field represents the frame type. The following frame types are possible:
  - Length/type = 0x8100—VLAN or stacked VLAN tagged frames. The MAC RX continues to check the frame and payload lengths.
  - Length/type = 0x8808—Control frames. The next two bytes are the Opcode field that indicates the type of control frame. For pause frames (Opcode = 0x0001) and PFC frames (Opcode = 0x0101), the MAC RX proceeds with pause frame processing.

    Note: Pause frame processing is not available in the Quartus Prime Pro 17.1 Stratix 10 ES Editions software. In this release, the IP core passes these frames to the RX client interface and updates the appropriate `l2_rxstatus_data` bits. However, the IP core does not implement flow control.
  - For other field values, the MAC RX forwards the receive frame to the client.

4.1.2.3.1. Length Checking

The MAC function checks the frame and payload lengths of basic, VLAN tagged, and stacked VLAN tagged frames.

The IP core checks that the frame length is valid—is neither undersized nor oversized. A valid frame length is at least 64 (0x40) bytes and does not exceed the following maximum value for the different frame types:

- Basic frames—The number of bytes specified in the `MAX_RX_SIZE_CONFIG` register.
- VLAN tagged frames—The value specified in the `MAX_RX_SIZE_CONFIG` register plus four bytes.
- Stacked VLAN tagged frames—The value specified in the `MAX_RX_SIZE_CONFIG` register plus eight bytes.

If the length/type field in a basic MAC frame or the client length/type field in a VLAN tagged frame has a value less than 0x600, the IP core also checks the payload length. The IP core keeps track of the payload length as it receives a frame, and checks the length against the relevant frame field. The payload length is valid if it satisfies the following conditions:

- The actual payload length matches the value in the length/type or client length/type field.
- Basic frames—the payload length is between 46 (0x2E)and 1536 (0x0600) bytes, excluding 1536.
- VLAN tagged frames—the payload length is between 42 (0x2A)and 1536 (0x0600), excluding 1536.
- Stacked VLAN tagged frames—the payload length is between 38 (0x26) and 1536 (0x0600), excluding 1536.

The RX MAC does not drop frames with invalid length or invalid payload length. If the frame or payload length is not valid, the MAC function asserts output error bits.

- `l2_rx_error[2]`—Undersized frame.
- `l2_rx_error[3]`—Oversized frame.
- `l2_rx_error[4]`—Payload length error.

If the length field value is greater than the actual payload length, the IP core asserts `l2_rx_error[4]`. If the length field value is less than the actual payload length, the MAC RX considers the frame to have excessive padding and does not assert `l2_rx_error[4]`.

4.1.2.4. RX CRC Checking and Dynamic Forwarding

By default, the RX MAC strips off the CRC bytes before forwarding the packet to the MAC client. You can configure the core to retain the RX CRC and forward it to the client by updating the `MAC_CRC_CONFIG` register.

4.1.3. Link Fault Signaling Interface

Link fault signaling reflects the health of the link. It operates between the remote Ethernet device Reconciliation Sublayer (RS) and the local Ethernet device RS. The link fault modules communicate status during the interframe period.

You enable link fault signaling by turning on **Enable link fault generation** in the parameter editor. For bidirectional fault signaling, the IP core implements the functionality defined in the *IEEE 802.3ba 40G/100G Ethernet Standard* and *Ethernet Clause 81.3.4* based on the `LINK_FAULT` configuration register settings.
For unidirectional fault signaling, the core implements *Clause 66 of the IEEE 802.3-2012 Ethernet Standard*.

Local Fault (LF)

If an Ethernet PHY sublayer detects a fault that makes the link unreliable, it notifies the RS of the local fault condition. If unidirectional is not enabled, the core follows *Clause 46*. The RS stops sending MAC data, and continuously generates a remote fault status on the TX datapath. After a local fault is detected, the RX PCS modifies the MII data and control to send local fault sequence ordered sets. Refer to *Link Fault Signaling Based On Configuration and Status* below.

The RX PCS cannot recognize the link fault under the following conditions:

- The RX PCS is not fully aligned.
- The bit error rate (BER) is high.

Remote Fault (RF)

If unidirectional is not enabled, the core follows *Clause 46*. If the RS receives a remote fault status, the TX datapath stops sending MAC data and continuously generates idle control characters. If the RS stops receiving fault status messages, it returns to normal operation, sending MAC client data. Refer to *Link Fault Signaling Based On Configuration and Status* below.

Link Status Signals

The MAC RX generates two link fault signals: `local_fault_status` and `remote_fault_status`.

Note: These signals are real time status signals that reflect the status of the link regardless of the settings in the link fault configuration register.

This register is generated only if you turn on **Enable link fault generation**. The MAC TX interface uses the link fault status signals for additional link fault signaling.

Table 12. Link Fault Signaling Based On Configuration and Status

For more information about the `LINK_FAULT` register, refer to TX MAC Registers.

LINK_FAULT Register (0x405)				Real Time Link Status		Configured TX Behavior		Comment
Bit [0]	Bit [3]	Bit [1]	Bit [2]	LF Received	RF Received	TX Data	TX RF	
1'b0	Don't care	Don't care	Don't care	Don't care	Don't care	On	Off	Disable Link fault signaling on TX. RX still reports link status. TX side Link fault signaling disabled on the link. TX data and idle.
1'b1	1'b1	Don't care	Don't care	Don't care	Don't care	Off	On	Force RF. TX: Stop data. Transmit RF only
1'b1	1'b0	1'b1	1'b1	Don't care	Don't care	On	Off	Unidir: Backwards compatible. TX: Transmit data and idle. No RF.
1'b1	1'b0	1'b1	1'b0	1'b1	1'b0	On	On	Unidir: LF received. TX: Transmit data 1 column IDLE after end of packet and RF
1'b1	1'b0	1'b1	1'b0	1'b0	1'b1	On	Off	Unidir: RF receives TX: Transmit data and idle. No RF.
1'b1	1'b0	1'b1	1'b0	1'b0	1'b0	On	Off	Unidir: No link fault TX: Transmit data and idle. No RF.
1'b1	1'b0	1'b0	Don't care	1'b1	1'b0	Off	On	Bidir: LF received

continued...

LINK_FAULT Register (0x405)				Real Time Link Status		Configured TX Behavior		Comment
Bit [0]	Bit [3]	Bit [1]	Bit [2]	LF Received	RF Received	TX Data	TX RF	
								TX: Stop data. Transmit RF only.
1'b1	1'b0	1'b0	Don't care	1'b0	1'b1	Off	Off	Bidir: RF received TX: Stop data. Idle only. No RF.
1'b1	1'b0	1'b0	Don't care	1'b0	1'b0	On	Off	Bidir: No link fault TX: Transmit data and idle. No RF.

Related Information

IEEE website
The Ethernet specifications are available on the IEEE website.

4.1.4. Intel Stratix 10Low Latency 40GBASE-KR4 IP Core Variations

The Intel Stratix 10 LL 40GBASE-KR4 IP core supports low-level control of analog transceiver properties for link training and auto-negotiation in the absence of a predetermined environment for the IP core. For example, an Ethernet IP core in a backplane may have to communicate with different link partners at different times. When it powers up, the environment parameters may be different than when it ran previously. The environment can also change dynamically, necessitating reset and renegotiation of the Ethernet link.

The Intel Stratix 10 LL 40GbE IP core 40GBASE-KR4 variations implement the *IEEE Backplane Ethernet Standard 802.3-2012*. The Intel Stratix 10 LL 40GbE IP core provides this reconfiguration functionality in Intel Stratix 10 devices by configuring each physical Ethernet lane with an Intel Backplane Ethernet 10GBASE-KR PHY IP core if you turn on **Enable KR4** in the Intel Stratix 10 LL 40GbE parameter editor.

The IP core includes the option to implement the following features:

- KR auto-negotiation provides a process to explore coordination with a link partner on a variety of different common features. The 40GBASE-KR4 variations of the Intel Stratix 10 LL 40GbE IP core can auto-negotiate only to a 40GBASE-KR4 configuration. Turn on the **Enable Auto-Negotiation** parameter to configure support for auto-negotiation.
- Link training provides a process for the IP core to train the link to the data frequency of incoming data, while compensating for variations in process, voltage, and temperature. Turn on the **Enable Link Training** parameter to configure support for link training.
- After the link is up and running, forward error correction (FEC) provides an error detection and correction mechanism to enable noisy channels to achieve the Ethernet-mandated bit error rate (BER) of 10^{-12}. Turn on the **Include FEC sublayer** parameter to configure support for FEC.

The Intel Stratix 10 LL 40GBASE-KR4 IP core variations include separate link training and FEC modules for each of the four Ethernet lanes, and a single auto-negotiation module. You specify the master lane for performing auto-negotiation in the parameter editor, and the IP core also provides register support to modify the selection dynamically.

Intel provides a testbench for Intel Stratix 10 LL 40GBASE-KR4 IP core variations that generate their own TX MAC clock (**Use external TX MAC PLL** is turned off). Intel provides a hardware design example for all Intel Stratix 10 LL 40GBASE-KR4 IP core variations that generate their own TX MAC clock, to assist you in integrating your Intel Stratix 10 LL 40GBASE-KR4 IP core into your complete design. You can examine the design example for an example of how to drive and connect the 40GBASE-KR4 IP core.

IP core FEC functionality relies on register settings in the Intel Stratix 10 LL 40GBASE-KR4 registers and on some specific register fields in the Intel Stratix 10 device registers.

To simulate correctly and to run correctly in hardware, you must drive the `reconfig_clk` and the `clk_status` inputs from the same source clock.

Related Information

Intel Stratix 10 Low Latency 40G Ethernet Design Example User Guide

4.2. User Interface to Ethernet Transmission

The IP core reverses the bit stream for transmission per Ethernet requirements. The transmitter handles the insertion of the inter-packet gap, frame delimiters, and padding with zeros as necessary. The transmitter also handles FCS computation and insertion.

The IP core transmits complete packets. After transmission begins, it must complete with no IDLE insertions. Between the end of one packet and the beginning of the next packet, the data input is not considered and the transmitter sends IDLE characters. An unbounded number of IDLE characters can be sent between packets.

4.2.1. Order of Transmission

The IP core transmits bytes on the Ethernet link starting with the preamble and ending with the FCS in accordance with the IEEE 802.3 standard. On the transmit client interface, the IP core expects the client to send the most significant bytes of the frame first, and to send each byte in big-endian format. Similarly, on the receive client interface, the IP core sends the client the most significant bytes of the frame first, and orders each byte in big-endian format.

Figure 9. Byte Order on the Client Interface Lanes

Describes the byte order on the Avalon streaming interface. Destination Address[40] is the broadcast/multicast bit (a type bit), and Destination Address[41] is a locally administered address bit.

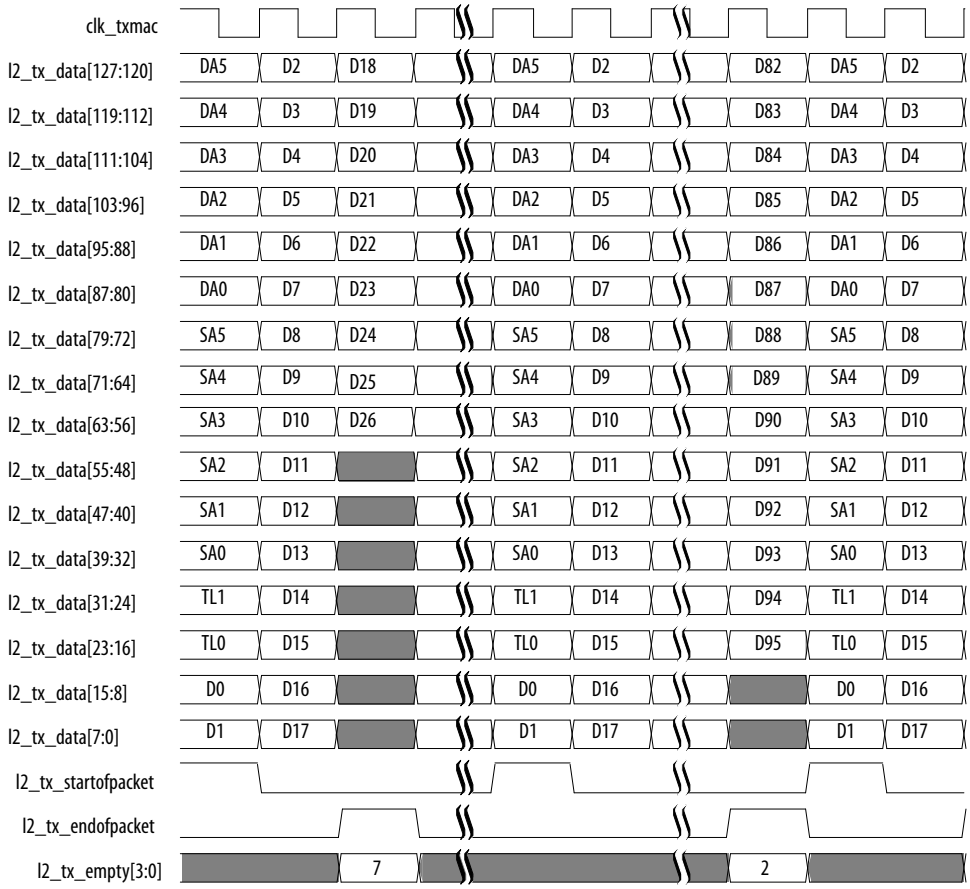
	Destination Address (DA)						Source Address (SA)						Type/ Length (TL)		Data (D)		
Octet	5	4	3	2	1	0	5	4	3	2	1	0	1	0	00	...	NN
Bit	[47:40]	[39:32]	[31:24]	[23:16]	[15:8]	[7:0]	[47:40]	[39:32]	[31:24]	[23:16]	[15:8]	[7:0]	[15:8]	[7:0]	MSB[7 :0]	...	LSB[7:0]

For example, the destination MAC address includes the following six octets AC-DE-48-00-00-80. The first octet transmitted (octet 0 of the MAC address described in the 802.3 standard) is AC and the last octet transmitted (octet 5 of the MAC address) is 80. The first bit transmitted is the low-order bit of AC, a zero. The last bit transmitted is the high order bit of 80, a one.

The preceding table and the following figure show that in this example, 0xAC is driven on DA5 (DA[47:40]) and 0x80 is driven on DA0 (DA[7:0]).

Figure 10. Octet Transmission on the Intel Stratix 10 LL 40GbE Avalon Streaming Interface

In the following diagram Preamble pass through is disabled.



4.2.2. Bit Order For TX and RX Datapaths

The TX bit order matches the placement shown in the PCS lanes as illustrated in *IEEE Standard for Ethernet, Section 4, Figure 49-5*. The RX bit order matches the placement shown in *IEEE Standard for Ethernet, Section 4, Figure 49-6*.

Related Information

IEEE website

The *IEEE Standard for Ethernet, Section 4* is available on the IEEE website.

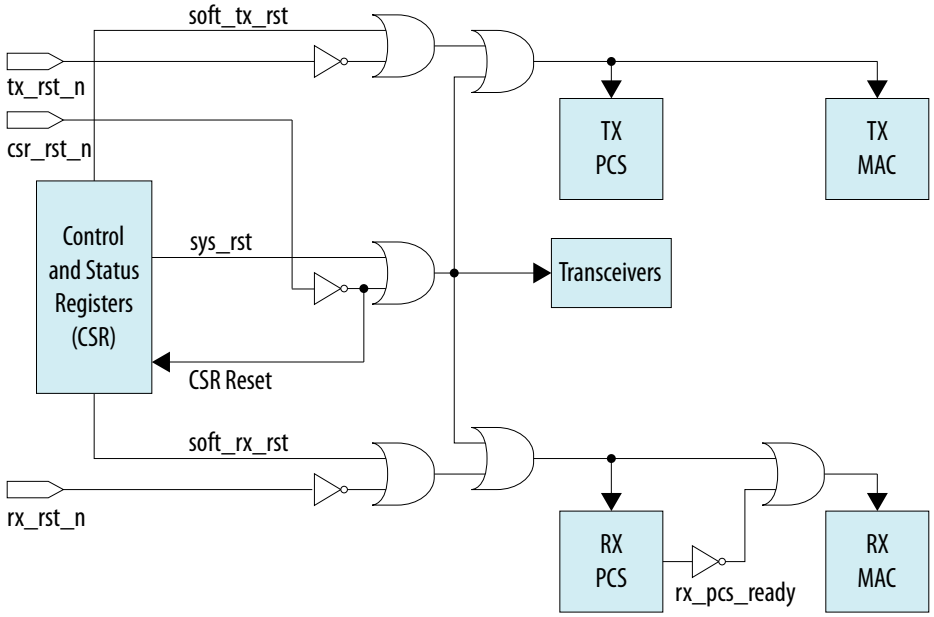
5. Reset

Control and Status registers control three parallel soft resets. These soft resets are not self-clearing. Software clears them by writing to the appropriate register. In addition, the IP core has three hard reset signals.

Asserting the external hard reset `csr_rst_n` returns all Control and Status registers to their original values, except the statistics counters. An additional dedicated reset signal resets the transceiver reconfiguration interface.

Figure 11. Conceptual Overview of General IP Core Reset Logic

The three hard resets are top-level ports. The three soft resets are internal signals which are outputs of the `PHY_CONFIG` register. Software writes the appropriate bit of the `PHY_CONFIG` to assert a soft reset.



The general reset signals reset the following functions:

- `soft_tx_rst`, `tx_rst_n`: Resets the IP core in the TX direction. Resets the TX PCS and TX MAC. This reset leads to deassertion of the `tx_lanes_stable` output signal.
- `soft_rx_rst`, `rx_rst_n`: Resets the IP core in the RX direction. Resets the RX PCS and RX MAC. This reset leads to deassertion of the `rx_pcs_ready` output signal.
- `sys_rst`, `csr_rst_n`: Resets the IP core. Resets the TX and RX MACs, PCS, and transceivers.

  Note: `csr_rst_n` resets the Control and Status registers, except the statistics counters. `sys_rst` does not reset any Control and Status registers.

  This reset leads to deassertion of the `tx_lanes_stable` and `rx_pcs_ready` output signals.

In addition, the synchronous `reconfig_reset` signal resets the IP core transceiver reconfiguration interface, an Avalon memory-mapped interface. Associated clock is the `reconfig_clk`, which clocks the transceiver reconfiguration interface.

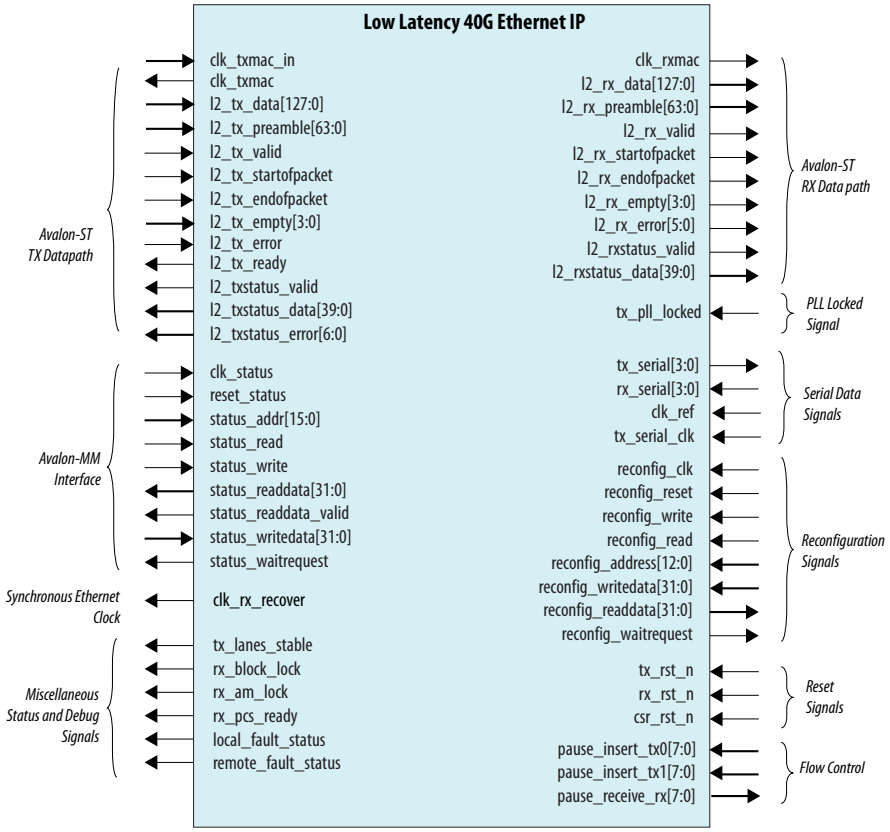
Note: The IP core has a top-level `reset_status` signal. However, this signal is currently unconnected in the IP core and has no effect. This signal is expected to be deprecated in future Intel Stratix 10 releases.

Related Information

Reset Signals on page 42

6. Interfaces and Signal Descriptions

Figure 12. Intel Stratix 10 LL 40GbE Intel FPGA IP Signals and Interfaces



6.1. TX MAC Interface to User Logic

The TX MAC provides an Avalon streaming interface to the FPGA fabric. The datapath comprises 2, 64-bit words. The minimum packet size is nine bytes.

Table 13. Avalon Streaming TX MAC Interface Signals

All interface signals are clocked by the `clk_txmac` clock. The value you specify for **Ready latency** in the Intel Stratix 10 LL 40GbE parameter editor is the Avalon streaming interface readyLatency value on this interface.

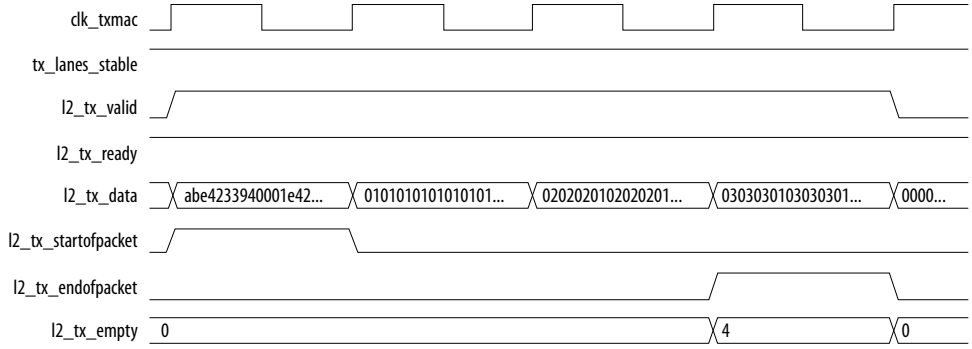
Signal	Direction	Description
`clk_txmac`	Output	The TX clock for the IP core is `clk_txmac`. The frequency of this clock is 312.5 MHz.

continued...

Signal	Direction	Description
		If you turn on **Use external TX MAC PLL** in the Intel Stratix 10 LL 40GbE parameter editor, the `clk_txmac_in` input clock drives `clk_txmac`.
`l2_tx_data[127:0]`	Input	Data input to MAC. Bit 127 is the MSB and bit 0 is the LSB. Bytes are read in the usual left to right order.
`l2_tx_preamble[63:0]`	Input	User preamble data. Available when you turn on **Enable preamble passthrough** in the Intel Stratix 10 LL 40GbE parameter editor. User logic drives the custom preamble data when `l2_tx_startofpacket` is asserted.
`l2_tx_valid`	Input	When asserted, indicates valid data.
`l2_tx_startofpacket`	Input	When asserted, indicates the first byte of a frame. When `l2_tx_startofpacket` is asserted, the MSB of `l2_tx_data` drives the start of packet. Packets that drive `l2_tx_startofpacket` and `l2_tx_endofpacket` in the same cycle are ignored.
`l2_tx_endofpacket`	Input	When asserted, indicates the end of a packet. Packets that drive `l2_tx_startofpacket` and `l2_tx_endofpacket` in the same cycle are ignored.
`l2_tx_empty[3:0]`	Input	Specifies the number of empty bytes when `l2_tx_endofpacket` is asserted.
`l2_tx_ready`	Output	When asserted, indicates that the MAC can accept the data. The IP core asserts the `l2_tx_ready` signal on clock cycle <*n*> to indicate that clock cycle <*n* + readyLatency> is a ready cycle. The client may only assert `l2_tx_valid` and transfer data during ready cycles.
`l2_tx_error`	Input	When asserted in an EOP cycle (while `l2_tx_endofpacket` is asserted), directs the IP core to insert an error in the packet before sending it on the Ethernet link. *Note:* This functionality is not available in the Quartus Prime Pro 17.1 Stratix 10 ES Editions software.
`l2_txstatus_valid`	Output	When asserted, indicates that `l2_txstatus_data` and `l2_txstatus_error[6:0]` are driving valid data.
`l2_txstatus_data[39:0]`	Output	Specifies information about the transmit frame. The following fields are defined: • [Bit 39]: When asserted, indicates a PFC frame • [Bit 38]: When asserted, indicates a unicast frame • Bit[37]: When asserted, indicates a multicast frame • Bit[36]: When asserted, indicates a broadcast frame • Bit[35]: When asserted, indicates a pause frame • Bit[34]: When asserted, indicates a control frame • Bit[33]: When asserted, indicates a VLAN frame • Bit[32]: When asserted, indicates a stacked VLAN frame • Bits[31:16]: Specifies the frame length from the first byte of the destination address to the last bye of the FCS • Bits[15:0]: Specifies the payload length
`l2_txstatus_error[6:0]`	Output	Specifies the error type in the transmit frame. The following fields are defined: • Bits[6:3]: Reserved • Bit[2]: Payload length error • Bit[1]: Oversized frame • Bit[0]: Reserved.

Figure 13. Client to MAC Avalon streaming interface

`l2_tx_data` reception order is highest byte to lowest byte. The first byte of the destination address is on `l2_tx_data[127:120]` , 0xabe4233 . . . in this timing diagram. The ready latency is 0 in this example.



Related Information

Avalon Interface Specifications
Detailed information about Avalon streaming interface and the Avalon streaming interface readyLatency parameter.

6.2. RX MAC Interface to User Logic

The RX MAC provides an Avalon streaming interface to the FPGA fabric. The datapath comprises 2, 64-bit words.

Table 14. Avalon Streaming RX MAC Interface Signals

All interface signals are clocked by the `clk_rxmac` clock.

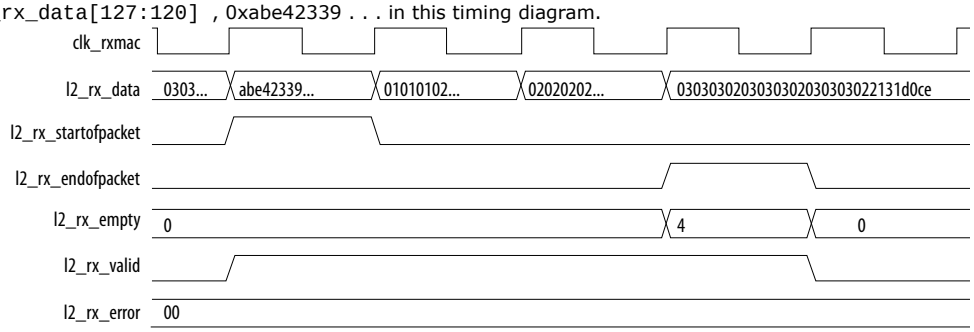
Signal	Direction	Description
`clk_rxmac`	Output	Clock for the RX MAC. Recovered from the incoming data. This clock is guaranteed stable when `rx_pcs_ready` is asserted. The frequency of this clock is 312.5 MHz. All RX MAC interface signals are synchronous to `clk_rxmac`.
`l2_rx_data[127:0]`	Output	Data output from the MAC. Bit 127 is the MSB and bit 0 is the LSB. Bytes are read in the usual left to right order. The IP core reverses the byte order to meet the requirements of the Ethernet standard.
`l2_rx_preamble[63:0]`	Output	Received preamble data. Available when you select PREAMBLE PASS-THROUGH mode. Valid when `l2_rx_startofpacket` is asserted.
`l2_rx_valid`	Output	When asserted, indicates that `l2_rx_data[127:0]` is driving data.
`l2_rx_startofpacket`	Output	When asserted, indicates the first byte of a frame.
`l2_rx_endofpacket`	Output	When asserted, indicates the last data byte of a frame, before the frame check sequence (FCS). In CRC pass-through mode, it is the last byte of the FCS. The packet can end at any byte position.
`l2_rx_empty[3:0]`	Output	Specifies the number of empty bytes when `l2_rx_endofpacket` is asserted. The packet can end at any byte position. The empty bytes are the low-order bytes.

continued...

Signal	Direction	Description
l2_rx_error[5:0]	Output	When asserted in the same cycle as l2_rx_endofpacket, indicates the current packet should be treated as an error packet. The 6 bits of l<*n*>_rx_error specify the following errors: • l2_rx_error[5]: Unused. • l2_rx_error[4]: Payload length error. The length field has a value less than 1535 (0x600) bytes and the received payload length is less than what is advertised in the length field. • l2_rx_error[3]: Oversized frame. The frame size is greater than the value specified in the MAX_RX_SIZE_CONFIG register. • l2_rx_error[2]: Undersized frame – The frame size is less than 64 bytes. Frame size = header size + payload size. • l2_rx_error[1]: CRC Error. The computed CRC value differs from the received CRC. • l2_rx_error[0]: Malformed packet. The packet is terminated with a non-terminate control character. When this bit is asserted, l2_rx_error[1] is also asserted.
l2_rxstatus_valid	Output	When asserted, indicates that l2_rxstatus_data is driving valid data.
l2_rxstatus_data[39:0]	Output	Specifies information about the received frame. The following fields are defined: • [Bit 39]: When asserted, indicates a PFC frame • [Bit 38]: When asserted, indicates a unicast frame • Bit[37]: When asserted, indicates a multicast frame • Bit[36]: When asserted, indicates a broadcast frame • Bit[35]: When asserted, indicates a pause frame • Bit[34]: When asserted, indicates a control frame • Bit[33]: When asserted, indicates a VLAN frame • Bit[32]: When asserted, indicates a stacked VLAN frame • Bits[31:16]: Specifies the frame length from the first byte of the destination address to the last bye of the FCS • Bits[15:0]: Specifies the payload length

Figure 14. MAC to Client Avalon Streaming Interface

l2_rx_data reception order is highest byte to lowest byte. The first byte of the destination address is on l2_rx_data[127:120] , 0xabe42339 . . . in this timing diagram.



6.3. Transceivers

The transceivers require a separately instantiated advanced transmit (ATX) PLL to generate the high speed serial clock. For Intel Stratix 10 LL 40GbE IP core, you can use the same ATX PLL for all four transceivers. In many cases, the same ATX PLL can serve as input to additional transceivers that have similar input clocking requirements. In comparison to the fractional PLL (fPLL) and clock multiplier unit PLL, the ATX PLL has the best jitter performance and supports the highest frequency operation.

Table 15. Transceiver Signals

Signal	Direction	Description
`tx_serial[3:0]`	Output	TX transceiver data. Each `tx_serial` bit becomes two physical pins that form a differential pair.
`rx_serial[3:0]`	Input	RX transceiver data. Each `rx_serial` bit becomes two physical pins that form a differential pair.
`clk_ref`	Input	The PLL reference clock. Input to the clock data recovery (CDR) circuitry in the RX PMA. The frequency of this clock is 644.53125 MHz.
`tx_serial_clk`	Input	High speed serial clock driven by the ATX PLL. The frequency of this clock is 5.15625 GHz. The IP core fans out the clock to target each of the four transceiver PHY links. You must drive this clock from a single TX transceiver PLL that you configure separately from the Intel Stratix 10 LL 40GbE IP core.
`tx_pll_locked`	Input	Lock signal from ATX PLL. Indicates the ATX PLL is locked.

6.4. Transceiver Reconfiguration Signals

You access the transceiver control and status registers using the transceiver reconfiguration interface. This is an Avalon memory-mapped interface.

The Avalon memory-mapped interface implements a standard memory-mapped protocol. You can connect an Avalon master to this bus to access the registers of the embedded Transceiver PHY IP core.

Table 16. Reconfiguration Interface Ports with Shared Native PHY Reconfiguration Interface

All interface signals are clocked by the `reconfig_clk` clock.

Port Name	Direction	Description
`reconfig_clk`	Input	Avalon clock. The clock frequency is 100-161 MHz. **All signals transceiver reconfiguration interface signals are synchronous to `reconfig_clk`.**
`reconfig_reset`	Input	Resets the Avalon memory-mapped interface and all of the registers to which it provides access.
`reconfig_write`	Input	Write enable signal. Signal is active high.
`reconfig_read`	Input	Read enable signal. Signal is active high.
`reconfig_address[12:0]`	Input	Address bus.
`reconfig_writedata[31:0]`	Input	A 32-bit data write bus. `reconfig_address` specifies the address.
`reconfig_readdata[31:0]`	Output	A 32-bit data read bus. Drives read data from the specified address. Signal is valid after `reconfig_waitrequest` is deasserted.
`reconfig_waitrequest`	Output	Indicates the Avalon memory-mapped interface is busy. Keep the `reconfig_write` or `reconfig_read` asserted until `reconfig_waitrequest` is deasserted.

Note: This IP internally implements the auto adaptation triggering for RX PMA CTLE/DFE mode.

Related Information

Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide
Provides more information about the transceiver reconfiguration interface, including timing diagrams for reads and writes.

6.5. Avalon Memory-Mapped Management Interface

You access control and status registers using an Avalon memory-mapped management interface. The interface responds regardless of the link status. It also responds when the IP core is in a reset state driven by any reset signal or soft reset other than the `csr_rst_n` signal. Asserting the `csr_rst_n` signal resets all control and status registers except the statistics registers; while this reset is in process, the Avalon memory-mapped management interface does not respond.

Table 17. Avalon Memory-Mapped Management Interface

Note: All `status_*` signals are synchronous to `clk_status` signal.

Signal	Direction	Description
`clk_status`	Input	The clock that drives the control and status registers. The frequency of this clock is 100-161 MHz.
`reset_status`	Input	Connect this signal to 1'b0. This signal remains visible as a top-level signal for backward compatibility.
`status_addr[15:0]`	Input	Drives the Avalon memory-mapped register address.
`status_read`	Input	When asserted, specifies a read request.
`status_write`	Input	When asserted, specifies a write request.
`status_readdata[31:0]`	Output	Drives read data. Valid when `status_readdata_valid` is asserted.
`status_readdata_valid`	Output	When asserted, indicates that `status_read_data[31:0]` is valid.
`status_writedata[31:0]`	Input	Drives the write data. The packet can end at any byte position. The empty bytes are the low-order bytes.
`status_waitrequest`	Output	Indicates that the control and status interface is not ready to complete the transaction. `status_waitrequest` is only used for read transactions.

Related Information

Typical Read and Write Transfers section in the *Avalon Interface Specifications*
Describes typical Avalon memory-mapped read and write transfers with a slave-controlled waitrequest signal.

6.6. Miscellaneous Status and Debug Signals

The miscellaneous status and debug signals are asynchronous.

Table 18. Avalon Memory-Mapped Interface

Signal	Direction	Description
`tx_lanes_stable`	Output	Asserted when all TX lanes are stable and ready to transmit data.
`rx_block_lock`	Output	Asserted when all lanes have identified 66-bit block boundaries in the serial data stream.
`rx_am_lock`	Output	Asserted when all lanes have identified alignment markers in the data stream.

continued...

Signal	Direction	Description
rx_pcs_ready	Output	Asserted when the RX lanes are fully aligned and ready to receive data.
local_fault_status	Output	Asserted when the RX MAC detects a local fault. This signal is available only if you turn on **Enable link fault generation** in the parameter editor.
remote_fault_status	Output	Asserted when the RX MAC detects a remote fault. This signal is available only if you turn on **Enable link fault generation** in the parameter editor.

6.7. Reset Signals

The IP core has three external hard reset inputs. These resets are asynchronous and are internally synchronized. Assert resets for ten cycles or until you observe the effect of their specific reset. Asserting the external hard reset csr_rst_n returns control and status registers to their original values, with the exception of the statistics counters. rx_pcs_ready and tx_lanes_stable are asserted when the IP core has exited reset successfully.

Table 19. Reset Signals

Signal	Direction	Description
tx_rst_n	Input	Active low hard reset signal. Resets the TX interface, including the TX PCS and TX MAC. This reset leads to the deassertion of the tx_lanes_stable output signal.
rx_rst_n	Input	Active low hard reset signal. Resets the RX interface, including the RX PCS and RX MAC. This reset leads to the deassertion of the rx_pcs_ready output signal.
csr_rst_n	Input	Active low hard global reset. Resets the full IP core. Resets the TX MAC, RX MAC, TX PCS, RX PCS, transceivers, and control and status registers, except the statistics counters. This reset leads to the deassertion of the tx_lanes_stable and rx_pcs_ready output signals.

Related Information

Reset on page 33

6.8. Clocks

You must set the transceiver reference clock (clk_ref) frequency to a value that the IP core supports. The Intel Stratix 10 LL 40GbE IP core supports a clk_ref frequency of 644.53125 MHz ±100 ppm or 322.265625 MHz ±100 ppm. The ±100ppm value is required for any clock source providing the transceiver reference clock.

SyncE IP core variations are IP core variations for which you turn on **Enable SyncE** in the parameter editor. These variations provide the RX recovered clock as a top-level output signal.

The Synchronous Ethernet standard, described in the ITU-T G.8261, G.8262, and G.8264 recommendations, requires that the TX clock be filtered to maintain synchronization with the RX reference clock through a sequence of nodes. The expected usage is that user logic drives the TX PLL reference clock with a filtered version of the RX recovered clock signal, to ensure the receive and transmit functions remain synchronized. In this usage model, a design component outside the Intel Stratix 10 LL 40GbE IP core performs the filtering.

Table 20. Clock Inputs

Describes the input clocks that you must provide.

Signal Name	Description
`clk_ref`	The input clock `clk_ref` is the reference clock for the transceiver RX CDR PLL. This clock must have a frequency of 644.53125 MHz or 322.265625 MHz with a ±100 ppm accuracy per the *IEEE 802.3ba-2010 Ethernet Standard.* In addition, `clk_ref` must meet the jitter specification of the *IEEE 802.3ba-2010 Ethernet Standard*. The PLL and clock generation logic use this reference clock to derive the transceiver and PCS clocks. The input clock should be a high quality signal on the appropriate dedicated clock pin. Refer to the relevant device datasheet for transceiver reference clock phase noise specifications.
`clk_txmac_in`	If you turn on **Use external TX MAC PLL** in the Intel Stratix 10 LL 40GbE parameter editor, this clock drives the TX MAC. The port is expected to receive the clock from the external TX MAC PLL and drives the internal clock `clk_txmac`. The required TX MAC clock frequency is 312.5 MHz. User logic must drive `clk_txmac_in` from a PLL whose input is the PHY reference clock, `clk_ref`.
`tx_serial_clk`	This input clock is part of the external PLL interface. The IP core fans out the clock to target each of the four transceiver PHY links. You must drive this clock from a single TX transceiver PLL that you configure separately from the Intel Stratix 10 LL 40GbE IP core. The required frequency is 5156.25 MHz.
`clk_status`	Clocks the control and status interface. The clock quality and pin chosen are not critical. `clk_status` is expected to be a 100–161 MHz clock. If you turn on **Enable KR4/CR4**, you must drive this clock and `reconfig_clk` with the same clock.
`reconfig_clk`	Clocks the transceiver reconfiguration interface. The clock quality and pin chosen are not critical. `reconfig_clk` is expected to be a 100–161 MHz clock. If you turn on **Enable KR4/CR4**, you must drive this clock and `clk_status` with the same clock.

Table 21. Clock Outputs

Describes the output clocks that the IP core provides. In most cases these clocks participate in internal clocking of the IP core as well.

Signal Name	Description
`clk_txmac`	The TX clock for the IP core is `clk_txmac`. The TX MAC clock frequency is 312.5 MHz. If you turn on **Use external TX MAC PLL** in the Intel Stratix 10 LL 40GbE parameter editor, the `clk_txmac_in` input clock drives `clk_txmac`.
`clk_rxmac`	The RX clock for the IP core is `clk_rxmac`. The RX MAC clock frequency is 312.5 MHz. This clock is only reliable when `rx_pcs_ready` has the value of 1. The IP core generates `clk_rxmac` from a recovered clock that relies on the presence of incoming RX data.
`clk_rx_recover`	RX recovered clock. This clock is available only if you turn on **Enable SyncE** in the Intel Stratix 10 LL 40GbE parameter editor. The RX recovered clock frequency is 156.25 MHz during normal operation. In 40GBASE-KR4CR4 variations, the `clk_rx_recover` clock frequency settles at 156.25 MHz only after the IP core completes auto-negotiation and link training. The expected usage is that you drive the TX transceiver PLL reference clock with a filtered version of `clk_rx_recover`, to ensure the receive and transmit functions remain synchronized in your Synchronous Ethernet system. To do so you must instantiate an additional component in your design. The IP core does not provide filtering.

6.9. Flow Control Interface

Flow Control Interface signals become available when you turn on **Enable MAC Flow Control** in the parameter editor.

Table 22. Flow Control Signals

Signal Name	Direction	Description
pause_insert_tx0[(FCQN-1):0] pause_insert_tx1[(FCQN-1):0]	Input	This signal is available if you specify pause on PFC. The signal indicates to the MAC whether XON or XOFF Pause or PFC flow control frame should be sent. • FCQN = 1 for Pause • FCQN = 1 ~ 8 for PFC The request for XON/XOFF flow control frame transmission can be done in either 1 or 2-bit request mode. **1-bit mode request model:** The IP core ignores pause_insert_tx1[(FCQN-1):0]. The following encoding is defined: • 0: No request • 0 to 1: Generate XOFF request • 1: Continue to generate XOFF request • 1 to 0: Generate XON request **2-bit mode request model:** The higher-order bit is in pause_insert_tx1[(FCQN-1):0] and the lower-order bit is in pause_insert_tx0[(FCQN-1):0]. The XON/XOFF request is a level-based request. The following encoding is defined: • 00: No further XON/XOFF request. In an XON/XOFF flow control frame is in progress, it is sent. • 01: Generate XON flow control frame and continuously sends them thereafter • 10: Generate XOFF flow control frame and continuously sends them thereafter • 11: Invalid request
pause_receive_rx[(FCQN-1):0]	Output	Each pause_receive_rx[(FCQN-1):0] bit indicates the corresponding queue is being paused. This is a level-based signal.

7. Control, Status, and Statistics Register Descriptions

This section provides information about the memory-mapped registers. You access these registers using the IP core Avalon memory-mapped control and status interface. The registers use 32-bit addresses; they are not byte addressable.

Write operations to a read-only register field have no effect. Read operations that address a Reserved register return an unspecified result. Write operations to Reserved registers have no effect. Accesses to registers that do not exist in your IP core variation, or to register bits that are not defined in your IP core variation, have an unspecified result. You should consider these registers and register bits Reserved. Although you can only access registers in 32-bit read and write operations, you should not attempt to write or ascribe meaning to values in undefined register bits.

Table 23. Register Base Addresses

Word Offset	Register Type
0xB0-0xFF	Intel Stratix 10 LL 40GBASE-KR4/CR4 registers
0x300-0x3FF	PHY registers
0x400-0x4FF	TX MAC registers
0x500-0x5FF	RX MAC registers
0x800-0x8FF	Statistics Counter registers - TX direction
0x900-0x9FF	Statistics Counter registers - RX direction

7.1. Intel Stratix 10 LL 40GBASE-KR4/CR4 Registers

Most 40GBASE-KR4 registers are 10GBASE-KR PHY registers of the Intel Stratix 10 10GBASE-KR PHY IP core. Exceptions are:

- The register offsets of the 10GBASE-KR PHY registers are offset by negative 0x400 in the 40GBASE-KR4 variations of the Intel Stratix 10 LL 40GbE core. The Intel Stratix 10 10GBASE-KR PHY IP core registers begin at offset 0x4B0. In the Intel Stratix 10 LL 40GBASE-KR4 IP core, these registers begin at offset 0x0B0.
- The LL 40GBASE-KR4 variations of the Intel Stratix 10 LL 40GbE core have additional 40GBASE-KR4 related registers and register fields.
- The FEC error insertion feature requires that you program some Intel Stratix 10 device registers through the Intel Stratix 10 dynamic reconfiguration interface. The FEC error count is collected in other Intel Stratix 10 device registers that you access through the Intel Stratix 10 dynamic reconfiguration interface. You access the relevant Intel Stratix 10 device registers at offsets 0xBD through 0xE3 for Lane 0, 0x8BD through 0x8E3 for Lane 1, 0x10BD through 0x10E3 for Lane 2, and 0x18BD through 0x18E3 for Lane 3. The descriptions of the Intel Stratix 10 LL 40GBASE-KR4 registers that depend on these Intel Stratix 10 device registers provide the individual Intel Stratix 10 register information.

Table 24. Intel Stratix 10 LL 40GBASE-KR4/CR4 Register Map

Word Offset	Register Type
0xB0-0xBF	General 40GBASE-KR4/CR4 registers
0xC0-0xCF	Auto-negotiation registers
0xD0-0xEF	Link training registers

Table 25. Intel Stratix 10 LL 40GbE Core 40GBASE-KR4 Registers

Register fields not listed are Reserved.

To modify a field value in any Intel Stratix 10 LL 40GBASE-KR4 register, you must perform a read-modify-write operation to ensure you do not modify the values of any other fields in the register.

Address	Name	Bit	Description	HW Reset Value	Access
0x0B0	Reset SEQ	[0]	When set to 1, resets the 40GBASE-KR4/CR4 sequencer (auto rate detect logic), may initiate a PCS reconfiguration, and may restart auto-negotiation, link training or both if AN and LT are enabled (40GBASE-KR4/CR4 mode). SEQ Force Mode[3:0] forces these modes. This reset self clears.		RWSC
	Disable AN Timer	[1]	Auto-negotiation disable timer. If disabled (Disable AN Timer = 1) , AN may get stuck and require software support to remove the ABILITY_DETECT capability if the link partner does not include this feature (does not implement auto-negotiation). In addition, software may have to take the link out of loopback mode if the link is stuck in the ACKNOWLEDGE_DETECT state. To enable this timer set Disable AN Timer = 0.		RW
	Disable LF Timer	[2]	When set to 1, disables the Link Fail timer. You can use this mode to characterize the link for link training. When set to 0, the Link Fault timer is enabled, and auto-negotation restarts at LF timer timeout.		RW
	SEQ Force Mode[3:0]	[7:4]	Forces the sequencer to a specific protocol. Must write the Reset SEQ bit (bit [0]) to 1 for the Force to take effect. The following encodings are defined: • 0000: No force • 0001: GigE mode (unsupported) • 0010: XAUI mode (unsupported) • 0100: 40GBASE-R4 mode (without auto-negotiation and without link training) • 0101: 40GBASE-KR4/CR4 mode • 1100: 40GBASE-R4 mode with FEC (without auto-negotiation and without link training)	4'b0	RW
	Enable Stratix 10 Calibration	[8]	When set to 1, it enables the Intel Stratix 10 HSSI reconfiguration calibration as part of the PCS dynamic reconfiguration. 0 skips the calibration when the PCS is reconfigured.	1'b1	RW
	LT Failure Response	[12]	When set to 1, LT failure causes the PHY to go into data mode (any of 40GBASE-R4, 40GBASE-KR4/CR4, or 40GBASE-R4 mode, as determined by current register and parameter settings). When set to 0, LT failure restarts auto-negotiation (if enabled). If auto-negotiation is not enabled, the PHY restarts LT.	1'b1 in simulation; 1'b0 in hardware	RW

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Address	Name	Bit	Description	HW Reset Value	Access
	Assert KR FEC ability 171.0	[16]	When set to 1, FEC is enabled (local FEC capability is on for auto-negotiation). When set to 0, FEC is disabled (local FEC capability is off for auto-negotiation). Resets to the **Set FEC_Ability bit on power up or reset** parameter value.	**Set FEC_Ability bit on power up or reset** parameter value	RW
	Assert KR FEC request	[18]	When set to 1, enables the FEC request in auto-negotiation. When this bit changes, you must assert the Reset SEQ bit (0xB0[0]) to renegotiate with the new value. When set to 0, disables the FEC request. Resets to the **Set FEC_Enable bit on power up or reset** parameter value.	**Set FEC_Enable bit on power up or reset** parameter value	RW
0x0B1	SEQ Link Ready	[0]	When asserted, the Sequencer is indicating that the link is ready.		RO
	SEQ AN timeout	[1]	When asserted, the Sequencer has had an auto-negotiation timeout. This bit is latched and is reset when the sequencer restarts auto-negotiation.		RO LH (latched high)
	SEQ LT timeout	[2]	When set, indicates that the Sequencer has had a link-training timeout. This bit is latched and is reset when the sequencer restarts auto-negotiation.		RO LH
	SEQ Reconfig Mode[5:0]	[13:8]	Specifies the Sequencer mode for PCS reconfiguration. The following modes are defined: • Bit 8, mode[0]: AN mode • Bit 9, mode[1]: LT Mode • Bit 10, mode[2]: 40G data mode • Bit 11, mode[3]: Reserved for GigE • Bit 12, mode[4]: Reserved for XAUI • Bit13, mode[5]: 40G FEC data mode		
	KR4 FEC ability 170.0	[16]	When set to 1, indicates that the 40GBASE-KR4/CR4 PHY supports FEC. For more information, refer to *Clause 45.2.1.84 of IEEE 802.3-2012.*	**Include FEC sublayer** parameter value	RO
	KR4 FEC errind ability 170.1	[17]	When set to 1, indicates that the 40GBASE-KR4/CR4 PHY is capable of reporting FEC decoding errors to the PCS. For more information, refer to *Clause 74.8.3 of IEEE 802.3-2012.*	**Include FEC sublayer** parameter value	RO
	FEC Block Lock	[23:20]	FEC Block Lock for lanes [3:0]: bit [20] is FEC block lock for lane 0, bit [21] is FEC block lock for lane 1, bit [22] is FEC block lock for lane 2, and bit [23] is FEC block lock for lane 3.	4'b0	RO

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Address	Name	Bit	Description	HW Reset Value	Access
0xB2	KR FEC TX Error Insert, Lane 0	11	Writing a 1 inserts one error pulse into the TX FEC for lane 0, depending on the Transcoder and Burst error settings for lane 0. You must select these settings through the Intel Stratix 10 dynamic reconfiguration interface to the Intel Stratix 10 device registers before you write a 1 to the KR FEC TX Error Insert, Lane 0 bit. To select these settings for Lane 0, perform a read-modify-write operation sequence at register offset 0xBD. You select a Transcoder error by setting the `transcode_err` bit (bit 0), resetting the `burst_err` bit (bit 1), resetting the `burst_err_len` field (bits [7:4]), and leaving the remaining bits at their previous values. You select a Burst error by setting the `burst_err` bit (bit 1), specifying the burst error length in the `burst_err_len` field (bits [7:4]), resetting the `transcode_err` bit (bit 0), and leaving the remaining bits at their previous values.	1'b0	RWSC
	RCLR_ERRBLK_CNT, Lane 0	12	Writing a 1 resets the error block counters.Writing a 0 causes counting to resume. Each lane has a 32-bit corrected error block counter and a 32-bit uncorrected error block counter in the Arria 10 device registers. Refer to *Clause 74.8.4.1* and *Clause 74.8.4.2* of *IEEE Std 802.3-2012*. For Lane 0, the corrected error block counter is in the Intel Stratix 10 device registers you access through the Intel Stratix 10 dynamic reconfiguration interface at offsets 0xDC to 0xDF: `blkcnt_corr[31:0]` is in {0xDF[7:0],0xDE[7:0],0xDD[7:0],0xDC[7:0]}. For Lane 0, the uncorrected error block counter is in the Intel Stratix 10 device registers you access through the Intel Stratix 10 dynamic reconfiguration interface at offsets 0xE0 to 0xE3: `blkcnt_uncorr[31:0]` is in {0xE3[7:0],0xE2[7:0],0xE1[7:0],0xE0[7:0]}.		RW
0x0B5	Register 0xB2 refers to Lane 0. This register is the equivalent of register 0xB2 for Lane 1. The relevant FEC error Intel Stratix 10 device registers for Lane 1 are at 0x8BD through 0x8E3 (additional offset of 0x800).				RW
0x0B8	This register is the equivalent of register 0xB2 for Lane 2. The relevant FEC error Intel Stratix 10 device registers for Lane 2 are at 0x10BD through 0x10E3 (additional offset of 0x1000 compared to the Lane 0 device registers).				RW
0x0BB	This register is the equivalent of register 0xB2 for Lane 3. The relevant FEC error Intel Stratix 10 device registers for Lane 3 are at 0x18BD through 0x18E3 (additional offset of 0x1800 compared to the Lane 0 device registers).				RW
0x0C0	`AN enable`	[0]	When set to 1, enables Auto Negotiation function. When set to 0, disables the Auto Negotiation state variable `mr_autoneg_enable` described in Clause 73.10.1 in *IEEE 802.3-2012*. For additional information, refer to Clause 45.2.7, Management Register Requirements, in *IEEE 802.3-2012*.	1'b1	RW
	`AN base pages ctrl`	[1]	When set to 1, the user base pages are enabled. You can send any arbitrary data via the user base page low or high bits. When set to 0, the user base pages are disabled and the state machine generates the base pages to send.		RW

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Address	Name	Bit	Description	HW Reset Value	Access
	AN next pages ctrl	[2]	When set to 1, the user next pages are enabled. You can send any arbitrary data via the user next page low or high bits. When set to 0, the user next pages are disabled. The state machine generates the null message to send as next pages.		RW
	Local device remote fault	[3]	When set to 1, the local device signals Remote Faults in the Auto Negotiation pages. When set to 0, the local device does not signal Remote Faults.		RW
	Force TX nonce value	[4]	When set to 1, forces the TX nonce value to support some UNH testing modes. Reset this bit to the value of 0 for normal operation.		RW
	Override AN Parameters Enable	[5]	When set to 1, overrides the AN_TECH (**Enable 40GBASE-CR4 Technology Ability** and **Include FEC sublayer**), AN_FEC (**Set FEC_Ability bit on power up or reset** and **Set FEC_Enable bit on power up or reset**), and AN_PAUSE (**Pause ability–C0** and **Pause ability–C1**) parameters and uses the bits in 0xC3[30:16] instead. You must reset the Sequencer (0xB0[0]) to reconfigure and restart in Auto Negotiation mode.		RW
	Ignore nonce field	[7]	When set to 1, tells the IP core to ignore the TX nonce field. This mode supports auto-negotiation when the IP core is in loopback mode.		RW
0x0C1	Reset AN	[0]	When set to 1, resets all the 40GBASE-KR4/CR4 auto-negotiation state machines. This bit is self-clearing. When set to 0, disables the Auto Negotiation state variable `mr_main_reset` (7.0.15) described in Clause 73.10.1 in *IEEE 802.3-2012*. For additional information, refer to Clause 45.2.7, Management Register Requirements, in *IEEE 802.3-2012*.		RWSC
	Restart AN TX SM	[4]	When set to 1, restarts the 40GBASE-KR4/CR4 TX state machines. This bit is self-clearing. This bit is active only when the TX state machine is in the Auto Negotiation state. When set to 0, disables the Auto Negotiation state variable `mr_restart_negotiation` (7.0.9) described in Clause 73.10.1 in *IEEE 802.3-2012*. For more information, refer to 7.0.9 in Clause 45.2.7, Management Register Requirements, in *IEEE 802.3-2012*		RWSC
	AN Next Page	[8]	When asserted, new next page info is ready to send. The data is in the XNP TX registers. When 0, the TX interface sends null pages. This bit is self-clearing. Next Page (NP) is encoded in bit D15 of Link Codeword. For more information, refer to Clause 73.6.9 and 7.16.15 of Clause 45.2.7.6 of *IEEE 802.3-2012*.		RWSC
0x0C2	AN page received	[1]	When set to 1, a page has been received. When 0, a page has not been received. The current value clears when the register is read. For more information, refer to 7.1.6 (state variable `mr_page_rx`) in Clause 73.8 of *IEEE 802.3-2012*.		RO LH
	AN Complete	[2]	When asserted, auto-negotiation has completed. When 0, auto-negotiation is in progress. For more information, refer to 7.1.5 (state variable `mr_autoneg_complete`) in Clause 73.8 of *IEEE 802.3-2012*.		RO

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Address	Name	Bit	Description	HW Reset Value	Access
	AN ADV Remote Fault	[3]	When set to 1, fault information has been sent to the link partner. When 0, a fault has not occurred. The current value clears when the register is read. Remote Fault (RF) is encoded in bit D13 of the base Link Codeword. For more information, refer to Clause 73.6.7 of and 7.16.13 (state variable mr_adv_ability) of *IEEE 802.3-2012*.		RO LH
	AN RX SM Idle	[4]	When set to 1, the auto-negotiation state machine is in the idle state. Incoming data is not Clause 73 compatible. When 0, the auto-negotiation is in progress.		RO
	AN Ability	[5]	When set to 1, the transceiver PHY is able to perform auto-negotiation. When set to 0, the transceiver PHY is not able to perform auto-negotiation. If your IP core variation includes auto-negotiation, this bit is tied to 1. For more information, refer to 7.1.3 and 7.48.0 in Clause 45 of *IEEE 802.3-2012*.		RO
	AN Status	[6]	When set to 1, the link is up. When 0, the link is down. The current value clears when the register is read. For more information, refer to 7.1.2 of Clause 45 of *IEEE 802.3-2012*.		RO LL (latched low)
	LP AN Ability	[7]	When set to 1, the link partner is able to perform auto-negotiation. When set to 0, the link partner is not able to perform auto-negotiation. For more information, refer to 7.1.0 in Clause 45 of *IEEE 802.3-2012*.		RO
	FEC negotiated – enable FEC from SEQ	[8]	When set to 1, the transceiver PHY has negotiated to perform FEC. When set to 0, the transceiver PHY has not negotiated to perform FEC. For more information, refer to 7.48.4 in Clause 45 of *IEEE 802.3-2012*.		RO
	Seq AN Failure	[9]	When set to 1, a sequencer auto-negotiation failure has been detected. When set to 0, an auto-negotiation failure has not been detected.		RO
	KR4 AN Link Ready [5:0]	[17:12]	Provides a one-hot encoding of an_receive_idle = true and link status for the supported link as described in Clause 73.10.1. The following encodings are defined: • 6'b000000: 1000BASE-KX • 6'b000001: 10GBASE-KX4 • 6'b000100: 10GBASE-KR • 6'b001000: 40GBASE-KR4 • 6'b010000: 40GBASE-CR4 • 6'b100000: 100GBASE-CR10 The only valid values for the LL 40GBASE-KR4/CR4 IP core are 6'b001000: 40GBASE-KR4 and 6'b010000: 40GBASE-CR4.	6'b001000	RO
0x0C3	User base page low	[15:0]	The Auto Negotiation TX state machine uses these bits if the Auto Negotiation base pages control bit (0xC0[1]) is set. The following bits are defined: • [4:0]: Selector • [9:5]: Echoed nonce bits which are set by the state machine • [12:10]: Pause bits		RW

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Address	Name	Bit	Description	HW Reset Value	Access
			• [13]: Remote Fault bit • [14]: ACK which is controlled by the SM • [15]: Next page bit Bit [49], the PRBS bit, is generated by the Auto Negotiation TX state machine.		
	`Override AN_TECH[5:0]`	[21:16]	AN_TECH value with which to override the current value. The following bits are defined: • [16]: `AN_TECH[0]`= 1000BASE-KX • [17]: `AN_TECH[1]` = XAUI • [18]: `AN_TECH[2]` = 10GBASE-KR • [19]: `AN_TECH[3]` = 40G • [20]: `AN_TECH[4]` = CR-4 • [21]: `AN_TECH[5]` = 100G You must set 0x4C0[5] for the override to take effect.		RW
	`Override AN_FEC[1:0]`	[25:24]	AN_FEC value with which to override the current value. The following bits are defined: • [24]: `AN_ FEC[0]` = Capability • [25]: `AN_ FEC[1]` = Request You must set 0x4C0[5] for the override to take effect.		RW
	`Override AN_PAUSE[2:0]`	[30:28]	AN_PAUSE value with which to override the current value. The following bits are defined: • [28]: `AN_PAUSE[0]` = Pause Ability • [29]: `AN_PAUSE[1]` = Asymmetric Direction • [30]: `AN_PAUSE[2]` = Reserved You must set 0x4C0[5] for the override to take effect.		RW
0x0C4	`User base page high`	[31:0]	The Auto Negotiation TX state machine uses these bits if the Auto Negotiation base pages ctrl bit (0xC0[1]) is set. The following bits are defined: • [31:30]: Correspond to page bits [47:46] which are the FEC bits. • [29:5]: Correspond to page bits [45:21] which are the technology ability bits. • [4:0]: Correspond to bits [20:16] which are TX nonce bits. Bit [49], the PRBS bit, is generated by the Auto Negotiation TX state machine.		RW
0x0C5	`User Next page low`	[15:0]	The Auto Negotiation TX state machine uses these bits if the Auto Negotiation next pages control bit (0xC0[2]) is set. The following bits are defined: • [11]: Toggle bit • [12]: ACK2 bit • [13]: MP bit • [14]: ACK which is controlled by the SM • [15]: Next page bit For more information, refer to Clause 73.7.7.1 Next Page encodings of *IEEE 802.3-2012*. Bit [49], the PRBS bit, is generated by the Auto Negotiation TX state machine.		RW

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Address	Name	Bit	Description	HW Reset Value	Access
0x0C6	User Next page high	[31:0]	The Auto Negotiation TX state machine uses these bits if the Auto Negotiation next pages ctrl bit (0xC0[2]) is set. Bits [31:0] correspond to page bits [47:16]. Bit [49], the PRBS bit, is generated by the Auto Negotiation TX state machine.		RW
0x0C7	LP base page low	[15:0]	The Auto Negotiation RX state machine receives these bits from the link partner. The following bits are defined: • [4:0]: Selector • [9:5]: Echoed nonce bits which are set by the state machine • [12:10]: Pause bits • [13]: Remote Fault bit • [14]: ACK which is controlled by the SM • [15]: Next page bit Bit [49], the PRBS bit, is not included.		RO
0x0C8	LP base page high	[31:0]	The Auto Negotiation RX state machine receives these bits from the link partner. The following bits are defined: • [31:30]: Correspond to page bits [47:46] which are the FEC bits. • [29:5]: Correspond to page bits [45:21] which are the technology ability bits. • [4:0]: Correspond to bits [20:16] which are TX nonce bits. Bit [49], the PRBS bit, is not included.		RO
0x0C9	LP Next page low	[15:0]	The Auto Negotiation RX state machine receives these bits from the link partner. The following bits are defined: • [11]: Toggle bit • [12]: ACK2 bit • [13]: MP bit • [14]: ACK which is controlled by the SM • [15]: Next page bit For more information, refer to Clause 73.7.7.1 Next Page encodings of *IEEE 802.3-2012*. Bit [49], the PRBS bit, is not included.		RO
0x0CA	LP Next page high	[31:0]	The Auto Negotiation RX state machine receives these bits from the link partner. Bits [31:0] correspond to page bits [47:16]. Bit [49], the PRBS bit, is not included.		RO
0x0CB	AN LP ADV Tech_A[24:0]	[24:0]	Received technology ability field bits of Clause 73 Auto Negotiation. Provides a one-hot encoding to specify one of the following protocols: • Bit [0]: 1000BASE-KX • Bit [1]: 10GBASE-KX4 • Bit [2]: 10GBASE-KR • Bit [3]: 40GBASE-KR4 • Bit [4]: 40GBASE-CR4 • Bit [5]: 100GBASE-CR10 • Bits [24:6] are reserved The only valid values for the LL 40GBASE-KR4 IP core are 'b001000: 40GBASE-KR4 and 'b010000: 40GBASE-CR4.	25'b0	RO

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Address	Name	Bit	Description	HW Reset Value	Access
	AN LP ADV FEC_F[1:0]	[26:25]	Received FEC ability bits FEC (F0:F1) is encoded in bits D46:D47 of the base Link Codeword. F0 is FEC ability. F1 is FEC requested.		RO
	AN LP ADV Remote Fault	[27]	Received Remote Fault (RF) ability bits. RF is encoded in bit D13 of the base link codeword in Clause 73 AN.		RO
	AN LP ADV Pause Ability_C[2:0]	[30:28]	Received pause ability bits. Pause (C0:C1) is encoded in bits D11:D10 of the base link codeword in Clause 73 AN as follows: • C0 is the same as PAUSE as defined in Annex 28B • C1 is the same as ASM_DIR as defined in Annex 28B • C2 is reserved		RO
0x0D0	Link training enable	[0]	When set to 1, enables the 40GBASE-KR4/CR4 start-up protocol. When 0, disables the 40GBASE-KR4/CR4 start-up protocol. The default value is 1. For more information, refer to Clause 72.6.10.3.1 and 10GBASE-KR PMD control register bit (150.1) of *IEEE 802.3-2012*.	1'b1	RW
	dis_max_wait_tmr	[1]	When set to 1, disables the LT max_wait_timer. Used for characterization mode when setting much longer BER timer values.		RW
	main_step_cnt[3:0]	[7:4]	Specifies the number of equalization steps for each main tap update. Devices have about 40 steps, so a value of 2 provides about 20 settings for the internal algorithm to test. A value of 3 provides 13 settings. The valid range is 1-15.	4'b0001	RW
	prepost_step_cnt[3:0]	[11:8]	Specifies the number of equalization steps for each pre- and post-tap update. Devices have 16-31 steps, a smaller range than for main_step_cnt. Set this value to provide fewer settings than for the main tap.	4'b0001	RW
	equal_cnt[2:0]	[14:12]	Number to make error counts equal. Adds hysteresis to the error count to avoid local minimums. The following values are defined: • 3'b000 = 0 • 3'b001 = 2 • 3'b010 = 4 • 3'b011 = 8 • 3'b100 = 16 • 3'b101 = 32 • 3'b110 = 64 • 3'b111 = 128	3'b101	RW
	disable Initialize PMA on max_wait_timeout	[15]	When set to 1, PMA values (VOD, Pre-tap, Post-tap) are not initialized upon entry into the Training_Failure state. This happens when max_wait_timer_done, which sets training_failure = true (0xD2[3])). Used for UNH testing. When set to 0, PMA values are initialized upon entry into Training_Failure state. Refer to Figure 72-5 of *IEEE 802.3-2012* for more details.	1'b0	
	Ovride LP Coef Enable	[16]	When set to 1, overrides the link partner's equalization coefficients; software changes the update commands sent to the link partner TX equalizer coefficients. When set to 0, uses the Link Training	1'b0	RW

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Address	Name	Bit	Description	HW Reset Value	Access
			logic to determine the link partner coefficients. Used with 0x0D1[7:4] and with bits[7:0] of 0x0D4 through 0x0D7.		
	Ovride Local RX Coef Enable	[17]	When set to 1, overrides the local device equalization coefficients generation protocol. When set, the software changes the local TX equalizer coefficients. When set to 0, uses the update command received from the link partner to determine local device coefficients. Used with 0x0D1[11:8] and bits[23:16] of 0x0D4 through 0x0D7.	1'b0	RW
0x0D1	Restart Link training, Lane 0	[0]	When set to 1, resets the 40GBASE-KR4 start-up protocol. When set to 0, continues normal operation. This bit self clears. Refer to the state variable mr_restart_training as defined in *Clause 72.6.10.3.1* and 10GBASE-KR PMD control register bit (150.0) in *IEEE Std 802.3-2012*.	1'b0	RW SC
	Restart Link training, Lane 1	[1]	This bit is the equivalent of register 0xD1[0] for Lane 1.	1'b0	RW SC
	Restart Link training, Lane 2	[2]	This bit is the equivalent of register 0xD1[0] for Lane 2.	1'b0	RW SC
	Restart Link training, Lane 3	[3]	This bit is the equivalent of register 0xD0[0] for Lane 3.	1'b0	RW SC
0x0D1	Updated TX Coef new, Lane 0	[4]	When set to 1, indicates that new link partner coefficients are available to send. The LT logic starts sending the new values set in 0xD4[7:0] to the remote device. When set to 0, continues normal operation. This bit self clears. This override of normal operation can only occur if 0xD0[16] (Ovride LP Coef enable) has the value of 1. If 0xD0[16] has the value of 0, this register field (0xD1[4]) has no effect.	1'b0	RW SC
	Updated TX Coef new, Lane 1	[5]	This bit is the equivalent of register 0xD1[4] for Lane 1. If set to the value of 1, LT logic sends the new values set in 0xE1[7:0] to the remote device.[6]		
	Updated TX Coef new, Lane 2		[6This bit is the equivalent of register 0xD1[4] for Lane 2. If set to the value of 1, LT logic sends the new values set in 0xE5[7:0] to the remote device.	1'b0	RW SC
	Updated TX Coef new, Lane 3	[7]	This bit is the equivalent of register 0xD1[4] for Lane 3. If set to the value of 1, LT logic sends the new values set in 0xE9[7:0] to the remote device.	1'b0	RW SC
0x0D1	Updated RX Coef new, Lane 0	[8]	When set to 1, indicates that new local device coefficients are available for Lane 1. The LT logic changes the local TX equalizer coefficients as specified in 0xD4[23:16]. When set to 0, continues normal operation. This bit self clears. This override of normal operation can only occur if 0xD0[17] (Ovride Local RX Coef enable) has the value of 1. If 0xD0[17] has the value of 0, this register field (0xD1[8]) has no effect.	1'b0	RW

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Address	Name	Bit	Description	HW Reset Value	Access
	Updated RX Coef new, Lane 1	[9]	This bit is the equivalent of register 0xD1[8] for Lane 1. If set to the value of 1, LT logic changes the local TX equalizer coefficients as specified in 0xE1[23:16].		
	Updated RX Coef new, Lane 2	[10]	This bit is the equivalent of register 0xD1[8] for Lane 2. If set to the value of 1, LT logic changes the local TX equalizer coefficients as specified in 0xE5[23:16].	1'b0	RW
	Updated RX Coef new, Lane 3	[11]	This bit is the equivalent of register 0xD1[8] for Lane 3. If set to the value of 1, LT logic changes the local TX equalizer coefficients as specified in 0xE9[23:16].	1'b0	RW
0x0D2	Link Trained - Receiver status, Lane 0	[0]	When set to 1, the receiver is trained and is ready to receive data. When set to 0, receiver training is in progress. For more information, refer to the state variable `rx_trained` as defined in Clause 72.6.10.3.1 of *IEEE 802.3-2012*.		RO
	Link Training Frame lock, Lane 0	[1]	When set to 1, the training frame delineation has been detected. When set to 0, the training frame delineation has not been detected. For more information, refer to the state variable `frame_lock` as defined in Clause 72.6.10.3.1 of *IEEE 802.3-2012*.		RO
	Link Training Start-up protocol status, Lane 0	[2]	When set to 1, the start-up protocol is in progress. When set to 0, start-up protocol has completed. For more information, refer to the state variable `training` as defined in Clause 72.6.10.3.1 of *IEEE 802.3-2012*.		RO
	Link Training failure, Lane 0	[3]	When set to 1, a training failure (max_wait_timeout) has been detected. When set to 0, a training failure has not been detected. For more information, refer to the state variable `training_failure` as defined in Clause 72.6.10.3.1 of *IEEE 802.3-2012*.		RO
	Link Training Frame lock Error, Lane 0	[5]	When set to 1, indicates a frame lock was lost during Link Training. If the tap settings specified by the fields of 0xD5 are the same as the initial parameter value, the frame lock error was unrecoverable. When set to 0, frame lock was not lost.		RO
	Link Trained - Receiver status, Lane 1 Link Training Frame lock, Lane 1 Link Training Start-up protocol status, Lane 1 Link Training failure, Lane 1	[13], [11:8]	Register bits 0xD2[5] and [3:0] refer to Lane 0. These bits are the equivalent of 0xD2[5] and [3:0], respectively, for Lane 1. For `Link Training Frame lock Error, Lane 1`, if the tap settings specified by the fields of 0xE2 are the same as the initial parameter value, the frame lock error was unrecoverable.		RO

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Address	Name	Bit	Description	HW Reset Value	Access
	Link Training Frame lock Error, Lane 1				
	Link Trained - Receiver status, Lane 2 Link Training Frame lock, Lane 2 Link Training Start-up protocol status, Lane 2 Link Training failure, Lane 2 Link Training Frame lock Error, Lane 2	[21], [19:16]	These bits are the equivalent of 0xD2[5] and [3:0], respectively, for Lane 2. For Link Training Frame lock Error, Lane 2, if the tap settings specified by the fields of 0xE6 are the same as the initial parameter value, the frame lock error was unrecoverable.		RO
	Link Trained - Receiver status, Lane 3 Link Training Frame lock, Lane 3 Link Training Start-up protocol status, Lane 3 Link Training failure, Lane 3 Link Training Frame lock Error, Lane 3	[29], [27:24]	These bits are the equivalent of 0xD2[5] and [3:0], respectively, for Lane 3. For Link Training Frame lock Error, Lane 3, if the tap settings specified by the fields of 0xEA are the same as the initial parameter value, the frame lock error was unrecoverable.		RO
0x0D3	ber_time_frames	[9:0]	Specifies the number of training frames to examine for bit errors on the link for each step of the equalization settings. Used only when ber_time_k_frames has the value of 0. The following values are defined:	0x003 in simulati	RW

continued...

Address	Name	Bit	Description	HW Reset Value	Access
			• A value of 2 is about 10^3 bytes • A value of 20 is about 10^4 bytes • A value of 200 is about 10^5 bytes	on; 0 in hardware	
	`ber_time_k_frames`	[19:10]	Specifies the number of thousands of training frames to examine for bit errors on the link for each step of the equalization settings. Set `ber_time_m_frames` to the value of 0 for time/bits to match the following values: • A value of 3 is about 10^7 bits = about 1.3 ms • A value of 25 is about 10^8 bits = about 11ms • A value of 250 is about 10^9 bits = about 11 0ms	0 in simulation; 0x00F in hardware	RW
	`ber_time_m_frames`	[29:20]	Specifies the number of millions of training frames to examine for bit errors on the link for each step of the equalization settings. Set `ber_time_k_frames` to the value of 0x3E8 (decimal 1000) for time/bits to match the following values: • A value of 3 is about 10^{10} bits = about 1.3 seconds • A value of 25 is about 10^{11} bits = about 11 seconds • A value of 250 is about 10^{12} bits = about 110 seconds	10'b0	RW
0x0D4	`LD coefficient update[5:0], Lane 0`	[5:0]	Reflects the contents of the first 16-bit word of the control channel that the IP core most recently sent on Lane 0. Normally, the bits in this register are read-only; however, when you override training by setting the `Ovride LP Coef enable` control bit (0x0D0 bit [16]), these bits become writable. The following fields are defined: • [5: 4]: Coefficient (+1) update — 2'b11: Reserved — 2'b01: Increment — 2'b10: Decrement — 2'b00: Hold • [3:2]: Coefficient (0) update (same encoding as [5:4]) • [1:0]: Coefficient (-1) update (same encoding as [5:4]) Before you can send these bits, you must enable the override in 0x0D0[16] and also signal a new word in 0x0D1[4]. For more information, refer to bit 10G BASE-KR LD coefficient update register bits (154.5:0) in Clause 45.2.1.80.3 of *IEEE 802.3-2012*.		RO/RW
	`LD Initialize Coefficients, Lane 0`	[6]	When set to 1, requests the link partner coefficients be set to configure the TX equalizer for Lane 0 to its INITIALIZE state. When set to 0, continues normal operation on Lane 0. The IP core sends this value in bit 12 of the control channel on Lane 0. For more information, refer to 10G BASE-KR LD coefficient update register bits (154.12) in Clause 45.2.1.80.3 and Clause 72.6.10.2.3.2 of *IEEE 802.3-2012*.		RO/RW
	`LD Preset Coefficients, Lane 0`	[7]	When set to 1, requests the link partner coefficients be set to a state where equalization is turned off on Lane 0. When set to 0 the link operates normally. The IP core sends this value in bit 13 of the control channel on Lane 0. For more information, refer to 10G		RO/RW

continued...

Address	Name	Bit	Description	HW Reset Value	Access
			BASE-KR LD coefficient update register bit (154.13) in Clause 45.2.1.80.3 and Clause 72.6.10.2.3.2 of *IEEE 802.3-2012*.		
	`LD coefficient status[5:0], Lane 0`	[13:8]	Status report register for the contents of the second, 16-bit word of the control channel that the IP core most recently sent on Lane 0. The following fields are defined: • [5:4]: Coefficient (+1) — 2'b11: Maximum — 2'b01: Minimum — 2'b10: Updated — 2'b00: Not updated • [3:2]: Coefficient (0) (same encoding as [5:4]) • [1:0]: Coefficient (-1) (same encoding as [5:4]) For more information, refer to 10G BASE-KR LD status report register bit (155.5:0) in Clause 45.2.1.81 of *IEEE 802.3-2012*.		RO
	`Link Training ready - LD Receiver ready, Lane 0`	[14]	When set to 1, the local device receiver has determined that training is complete and is prepared to receive data. The IP core sends this value in bit 15 of the control channel on Lane 0. When set to 0, the local device receiver is requesting that training continue. Values for the receiver ready bit are defined in Clause 72.6.10.2.4.4. For more information, refer to 10G BASE-KR LD status report register bit (155.15) in Clause 45.2.1.81 of *IEEE 802.3-2012*.		RO
	`LP Coefficient Update[5:0], Lane 0`	[21:16]	Reflects the contents of the first 16-bit word of the control channel that the IP core most recently received on Lane 0. Normally the bits in this register are read only; however, when training is disabled by setting low the Link Training enable control bit (`Link training enable` at 0xD0[0]), these bits become writable. The following fields are defined: • [5: 4]: Coefficient (+1) update — 2'b11: Reserved — 2'b01: Increment — 2'b10: Decrement — 2'b00: Hold • [3:2]: Coefficient (0) update (same encoding as [5:4]) • [1:0]: Coefficient (-1) update (same encoding as [5:4]) Before you can send these bits, you must enable the override in 0x0D0 bit [17] and also signal a new word in 0x0D2 bit [8]. For more information, refer to bit 10G BASE-KR LP coefficient update register bits (152.5:0) in Clause 45.2.1.78.3 of *IEEE 802.3-2012*.		RO/RW
	`LP Initialize Coefficients, Lane 0`	[22]	When set to 1, the local device transmit equalizer coefficients are set to the INITIALIZE state. When set to 0, normal operation continues. The function and values of the initialize bit are defined in Clause 72.6.10.2.3.2. The IP core receives this value on Lane 0 in bit 12 of the control channel. For more information, refer to 10G BASE-KR LP coefficient update register bits (152.12) in Clause 45.2.1.78.3 of *IEEE 802.3-2012*.		RO/RW

continued...

Address	Name	Bit	Description	HW Reset Value	Access
	LP Preset Coefficients, Lane 0	[23]	When set to 1, the local device TX coefficients are set to a state where equalization is turned off. Preset coefficients are used. When set to 0, the local device operates normally. The IP core receives this value on Lane 0 in bit 13 of the control channel. The function and values of the preset bit are defined in 72.6.10.2.3.1. The function and values of the initialize bit are defined in Clause 72.6.10.2.3.1. For more information, refer to 10G BASE-KR LP coefficient update register bits (152.13) in Clause 45.2.1.78.3 of *IEEE 802.3-2012*.		RO/RW
	LP coefficient status[5:0], Lane 0	[29:24]	Status report register reflects the contents of the second, 16-bit word of the control channel that the IP core most recently received on Lane 0. The following fields are defined: • [5:4]: Coefficient (+1) — 2'b11: Maximum — 2'b01: Minimum — 2'b10: Updated — 2'b00: Not updated • [3:2]: Coefficient (0) (same encoding as [5:4]) • n [1:0]: Coefficient (-1) (same encoding as [5:4]) For more information, refer to 10G BASE-KR LP status report register bits (153.5:0) in Clause 45.2.1.79 of *IEEE 802.3-2012*.		RO
	LP Receiver ready, Lane 0	[30]	When set to 1, the link partner receiver has determined that training is complete and is prepared to receive data. When set to 0, the link partner receiver is requesting that training continue. The IP core receives this value on Lane 0 in bit 15 of the control channel. Values for the receiver ready bit are defined in Clause 72.6.10.2.4.4. For more information, refer to 10G BASE-KR LP status report register bits (153.15) in Clause 45.2.1.79 of *IEEE 802.3-2012*.		RO
0x0D5	LT V_{OD} setting, Lane 0	[4:0]	Stores the most recent TX V_{OD} setting trained by the link partner's RX based on the LT coefficient update logic driven by Clause 72. It reflects Link Partner commands to fine-tune the TX taps.		RO
	LT Post-tap setting, Lane 0	[13:8]	Stores the most recent TX post-tap setting trained by the link partner's RX based on the LT coefficient update logic driven by Clause 72. It reflects Link Partner commands to fine-tune the TX taps.		RO
	LT Pre-tap setting, Lane 0	[20:16]	Stores the most recent TX pre-tap setting trained by the link partner's RX based on the LT coefficient update logic driven by Clause 72. It reflects Link Partner commands to fine-tune the TX taps.		RO
0x0D6	LT VODMAX ovrd, Lane 0	[4:0]	Override value for the **VMAXRULE** parameter on Lane 0. When enabled, this value substitutes for the **VMAXRULE** to allow channel-by-channel override of the device settings. This only effects the local device TX output for the channel specified. This value must be greater than the **INITMAINVAL** parameter for proper operation. Note this also overrides the **PREMAINVAL** parameter value.	0x1C (28 decimal) for simulation; 0 for hardware	RW

continued...

Address	Name	Bit	Description	HW Reset Value	Access
	LT VODMAX ovrd Enable, Lane 0	[5]	When set to 1, enables the override value for the **VMAXRULE** parameter stored in the LT VODMAX ovrd, Lane 0 register field.	1 for simulation; 0 for hardware	RW
	LT VODMin ovrd, Lane 0	[12:8]	Override value for the **VODMINRULE** parameter on Lane 0. When enabled, this value substitutes for the **VMINRULE** to allow channel-by-channel override of the device settings. This override only effects the local device TX output for this channel. The value to be substituted must be less than the **INITMAINVAL** parameter and greater than the **VMINRULE** parameter for proper operation.	0x19 (25 decimal) for simulation; 0 for hardware	RW
	LT VODMin ovrd Enable, Lane 0	[13]	When set to 1, enables the override value for the **VODMINRULE** parameter stored in the LT VODMin ovrd, Lane 0 register field.	1 for simulation; 0 for hardware	RW
	LT VPOST ovrd, Lane 0	[21:16]	Override value for the **VPOSTRULE** parameter on Lane 0. When enabled, this value substitutes for the **VPOSTRULE** to allow channel-by-channel override of the device settings. This override only effects the local device TX output for this channel. The value to be substituted must be greater than the **INITPOSTVAL** parameter for proper operation.	6 for simulation; 0 for hardware	RW
	LT VPOST ovrd Enable, Lane 0	[22]	When set to 1, enables the override value for the **VPOSTRULE** parameter stored in the LT VPOST ovrd, Lane 0 register field.	1 for simulation; 0 for hardware	RW
	LT VPre ovrd, Lane 0	[28:24]	Override value for the **VPRERULE** parameter on Lane 0. When enabled, this value substitutes for the **VPOSTRULE** to allow channel-by-channel override of the device settings. This override only effects the local device TX output for this channel. The value to be substituted must be greater than the **INITPREVAL** parameter for proper operation.	4 for simulation; 0 for hardware	RW
	LT VPre ovrd Enable, Lane 0	[29]	When set to 1, enables the override value for the **VPRERULE** parameter stored in the LT VPre ovrd, Lane 0 register field.	1 for simulation; 0 for compilation	RW
0xE0	Register 0xD3 refers to Lane 0. This register, register 0xE0, is the equivalent of register 0xD3 for Lane 1 link training.				RW
0xE1	Register 0xD4 refers to Lane 0. This register, register 0xE1, is the equivalent of register 0xD4 for Lane 1 link training.				R / RW
0xE2	Register 0xD5 refers to Lane 0. This register, register 0xE2, is the equivalent of register 0xD5 for Lane 1 link training.				RO
0xE3	Register 0xD6 refers to Lane 0. This register, register 0xE3, is the equivalent of register 0xD6 for Lane 1 link training..				RW

continued...

Address	Name	Bit	Description	HW Reset Value	Access
0xE4	This register is the equivalent of register 0xD3 for Lane 2 link training.				RW
0xE5	This register is the equivalent of register 0xD4 for Lane 2 link training.				R / RW
0xE6	This register is the equivalent of register 0xD5 for Lane 2 link training.				RO
0xE7	This register is the equivalent of register 0xD6 for Lane 2 link training.				RW
0xE8	This register is the equivalent of register 0xD3 for Lane 3 link training.				RW
0xE9	This register is the equivalent of register 0xD4 for Lane 3 link training.				R / RW
0xEA	This register is the equivalent of register 0xD5 for Lane 3 link training.				RO
0xEB	This register is the equivalent of register 0xD6 for Lane 3 link training.				RW

7.2. PHY Registers

Table 26. PHY Registers

The global hard reset `csr_rst_n` resets all of these registers. The TX reset `tx_rst_n` and RX reset `rx_rst_n` signals do not reset these registers.

Addr	Name	Description	Reset	Access
0x300	`REVID`	IP core PHY module revision ID.	0x0627 2016	RO
0x301	`SCRATCH`	Scratch register available for testing.	0x0000 0000	RW
0x302	`PHY_NAME_0`	First characters of IP core variation identifier string, "0040". The "00" is unprintable.	0x0000 3430	RO
0x303	`PHY_NAME_1`	Next characters of IP core variation identifier string, "00GE". The "00" is unprintable.	0x0000 4745	RO
0x304	`PHY_NAME_2`	Final characters of IP core variation identifier string, "0pcs". The "0" is unprintable.	0x0070 6373	RO
0x310	`PHY_CONFIG`	PHY configuration registers. The following bit fields are defined: • Bit[0]: : `sys_rst`. Full system reset (except registers). Set this bit to initiate the internal reset sequence. • Bit[1]: `soft_txp_rst`. TX soft reset. Resets TX PCS and TX MAC. • Bit[2]: `soft_rxp_rst`. RX soft reset. Resets RX PCS and RX MAC. • Bits[31:3]: Reserved.	29'hX_3'b0 (1)	RW
0x312	`WORD_LOCK`	When asserted, indicates that the virtual channel has identified 66 bit block boundaries in the serial data stream.	28'hX4'b0 (1)	RO
0x313	`EIO_SLOOP`	Serial PMA loopback. Setting a bit puts the corresponding transceiver in serial loopback mode. In serial loopback mode, the TX lane loops back to the RX lane on an internal loopback path.	28'hX4'b0 (1)	RW

continued...

(1) X means "Don't Care".

(2) Register value convert in decimal.

Addr	Name	Description	Reset	Access
0x314	EIO_FLAG_SEL	Supports indirect addressing of individual FIFO flags in the PCS Native PHY IP core. Program this register with the encoding for a specific FIFO flag. The flag values (one per transceiver) are then accessible in the EIO_FLAGS register. The value in the EIO_FLAG_SEL register directs the IP core to make available the following FIFO flag: • 3'b000: TX FIFO full • 3'b001: TX FIFO empty • 3b010: TX FIFO partially full • 3'b011: TX FIFO partially empty • 3b100: RX FIFO full • 3b101: RX FIFO empty • 3b110: RX FIFO partially full • 3b111: RX FIFO partially empty	29'hX3'b0 (1)	RW
0x315	EIO_FLAGS	PCS indirect data. To read a FIFO flag, set the value in the EIO_FLAG_SEL register to indicate the flag you want to read. After you specify the flag in the EIO_FLAG_SEL register, each bit [n] in the EIO_FLAGS register has the value of that FIFO flag for the transceiver channel for lane [n].	28'hX4'b0 (1)	RO
0x321	EIO_FREQ_LOCK	Each asserted bit indicates that the corresponding lane RX clock data recovery (CDR) phase-locked loop (PLL) is locked.	28'hX4'b0 (1)	RO
0x322	PHY_CLK	The following encodings are defined: • Bit[0]: Indicates if the TX PCS is ready • Bit [1]: Indicates if the TX MAC PLL is locked. • Bit[2]: Indicates if the RX CDR PLL is locked.	29'hX3'b00 (1)	RO
0x323	FRM_ERR	Each asserted bit indicates that the corresponding virtual lane has a frame error. You can read this register to determine if the IP core sustains a low number of frame errors, below the threshold to lose word lock. These bits are sticky, unless the IP core loses word lock. Write 1'b1 to the SCLR_FRM_ERR register to clear. If the IP core loses word lock, it clears this register.	28'hX_4'b0 (1)	RO
0x324	SCLR_FRM_ERR	Synchronous clear for FRM_ERR register. Write 1'b1 to this register to clear the FRM_ERR register and bit [1] of the LANE_DESKEWED register. A single bit clears all sticky framing errors. This bit does not auto-clear. Write a 1'b0 to continue logging frame errors.	0x0	RW
0x325	EIO_RX_SOFT_PURGE_S	Set bit [0] to clear the RX FIFO for all four physical lanes.	0x0000	RO

continued...

(1) X means "Don't Care".

(2) Register value convert in decimal.

Addr	Name	Description	Reset	Access
		• Bit[11]: If set to 1, disables the bitslip request from PCS to PMA. • Bit[12]: If set to 1, disables the reset request from PCS to PMA. To use the transceiver toolkit, this bit must be set to 1.		
0x326	RX_PCS_FULLY_ALIGNED_S	Indicates the RX PCS is fully aligned and ready to accept traffic. • Bit[0]: RX PCS fully aligned status. • Bit[1]: RX PCS bit error rate status. A bit value of 1 indicates a bit error rate higher than 10^{-4} or there are at least 16 errors within 50 us. This bit value is only valid when the link fault generation is enabled.	31'hX1'b0 (1)	RO
0x328	AM_LOCK	When asserted indicates that the physical channel has identified virtual lane alignment markers in the data stream.	28'hX_4'b0 (1)	RO
0x329	LANE_DESKEWED	The following encodings are defined: • Bit [0]: Indicates all lanes are deskewed. • Bit [1]: When asserted indicates a change in lanes deskewed status. To clear this sticky bit, write 1'b1 to the corresponding bit of the SCLR_FRM_ERR register. This is a latched signal.	30'hX2'b00 (1)	RO
0x330	PCS_VLANE	The following encodings are defined: • Bit[1:0]: Virtual index for physical lane 0. • Bit[3:2]: Virtual index for physical lane 1. • Bit[5:4]: Virtual index for physical lane 2. • Bit[7:6]: Virtual index for physical lane 3.	24'bX8'b0 (1)	RO
0x340	KHZ_REF	The register indicates the value of reference clock frequency. Apply the following definition for the frequency value: [(Register value (2) * clk_status)/10] KHZ	0x0000 0000	RO
0x341	KHZ_RX	The register indicates the value of RX clock (clk_rxmac) frequency. Apply the following definition for the frequency value: [(Register value (2) * clk_status)/10] KHZ	0x0000 0000	RO
0x342	KHZ_TX	The register indicates the value of TX clock (clk_txmac) frequency. Apply the following definition for the frequency value: [(Register value (2) * clk_status)/10] KHZ	0x0000 0000	RO

(1) X means "Don't Care".

(2) Register value convert in decimal.

7.3. TX MAC Registers

Table 27. TX MAC Registers

Addr	Name	Description	Reset	Access
0x400	TXMAC_REVID	TX MAC revision ID for 40GbE TX MAC CSRs.	0x0627 2016	RO
0x401	TXMAC_SCRATCH	Scratch register available for testing.	0x0000 0000	RW
0x402	TXMAC_NAME_0	First 4 characters of module variation identifier string, "40gMACTxCSR".	0x3430 674D	RO
0x403	TXMAC_NAME_1	Next 4 characters of IP core variation identifier string, "ACTx".	0x4143 5278	RO
0x404	TXMAC_NAME_2	Final 4 characters of IP core variation identifier string, "0CSR". The "0" is unprintable.	0x0043 5352	RO
0x405	LINK_FAULT	Link Fault Configuration Register. The following bits are defined: • `Force Remote Fault` bit[3]: When link fault generation is enabled, stops data transmission and forces transmission of a remote fault. • `Disable Remote Fault` bit[2]: When both link fault reporting and unidirectional transport are enabled, the core transmits data and does not transmit remote faults (RF). This bit takes effect when the value of this register is 28'hX4'b0111. • `Unidir Enable` bit[1]: When asserted, the core includes Clause 66 support for the remote link fault reporting on the Ethernet link. • `Link Fault Reporting Enable` bit[0]: The following encodings are defined: — 1'b1: The PCS generates the proper fault sequence on Ethernet link, when conditions are met. — 1'b0: The PCS does not generate the fault sequence.	28'hX_4'b0001 (3)	RW
0x406	IPG_COL_REM	Specifies the number of IDLE columns to be removed in every Alignment Marker period to compensate for alignment marker insertion. You can program this register to a larger value than the default value, for clock compensation. Bits [31:8] of this register are Reserved.	0xXXXX 0004 (3)	RW
0x407	MAX_TX_SIZE_CONFIG	Specifies the maximum TX frame length. Frames that are longer are considered oversized. They are transmitted, but also increment the CNTR_TX_OVERSIZE register. Bits [31:16] of this register are Reserved.	0xXXXX 2580 (3)	RW
0x40A	TX_MAC_CONTROL	TX MAC Control Register. A single bit is defined:	30'hX2'b0X (3)	RW

continued...

(3) X means "Don't Care".

Addr	Name	Description	Reset	Access
		• Bit[1]: VLAN detection disabled. This bit is deasserted by default, implying VLAN detection is enabled.		

7.4. RX MAC Registers

Table 28. RX MAC Registers

Addr	Name	Description	Reset	Access
0x500	RXMAC_REVID	RX MAC revision ID for Stratix 10 40GbE IP core.	0x0627 2016	RO
0x501	RXMAC_SCRATCH	Scratch register available for testing.	0x0000 0000	RW
0x502	RXMAC_NAME_0	First 4 characters of IP core variation identifier string, "40gMACRxCSR".	0x3430 674D	RO
0x503	RXMAC_NAME_1	Next 4 characters of IP core variation identifier string, "ACRx".	0x4143 5278	RO
0x504	RXMAC_NAME_2	Final 4 characters of IP core variation identifier string, "0CSR". The "0" is unprintable.	0x0043 5352	RO
0x506	MAX_RX_SIZE_CONFIG	Specifies the maximum frame length available. The MAC asserts `l2_rx_error[3]` when the length of the received frame exceeds the value of this register. If the IP core receives an Ethernet frame of size greater than the number of bytes specified in this register, and the IP core includes statistics registers, the IP core increments the 64-bit `CNTR_RX_OVERSIZE` counter.	0xXXXX 2580 (4)	RW
0x507	MAC_CRC_CONFIG	The RX CRC forwarding configuration register. The following encodings are defined: • 1'b0: Remove RX CRC, do not forward it to the RX client interface • 1'b1: Retain RX CRC, forward it to the RX client interface In either case, the IP core checks the incoming RX CRC and flags errors.	31'hX1'b0 (4)	RW
0x508	LINK_FAULT	Link Fault Status Register. • Bit[0]: Local fault status bit. • Bit[1]: Remote fault status bit. For regular (non-unidirectional) Link Fault, implements *IEEE 802.3 BA Ethernet Clause 81.3.4.* For unidirectional Link Fault, implements *IEEE 802.3 Ethernet Clause 66.*	30'hX2'b00 (4)	RO
0x50A	RX_MAC_CONTROL	RX MAC Control Register. The following bits are defined:	30'h0_2'b0X (4)	RW

continued...

(3) X means "Don't Care".

(4) X means "Don't Care".

Addr	Name	Description	Reset	Access
		• Bit[4]: Preamble check. Strict SFD checking option to compare each packet preamble to 0x555555555555. This field is available only if you turn on **Enable Strict SFD check**. • Bit[3]: SFD check. Strict SFD checking option to compare each SFD byte to 0x5D. This field is available only if you turn on **Enable Strict SFD check**. • Bit [1]: VLAN detection disabled. This bit is deasserted by default implying VLAN detection is enabled.		

7.5. Statistics Registers

The Intel Stratix 10 LL 40GbE statistics registers count Ethernet traffic and errors. The 64-bit statistics registers are designed to roll over, to ensure timing closure on the FPGA. However, these registers should never roll over if the link is functioning properly. The statistics registers check the size of frames, which includes the following fields:

- Size of the destination address
- Size of the source address
- Size of the data
- Four bytes of CRC

The statistics counters module is a synthesis option. The statistics registers are counters that are implemented inside the CSR. When you turn on the **Enable MAC stats counters** parameter in the Intel Stratix 10 LL 40GbE parameter editor, the counters are implemented in the CSR. When you turn off the **Enable MAC stats counters** parameter in the Intel Stratix 10 LL 40GbE parameter editor, the counters are not implemented in the CSR, and read access to the counters returns undefined results.

After system power-up, the statistics counters have random values. You must clear these registers and confirm the system is stable before using their values. You can clear the registers with the `csr_rst_n` input signal, or with the configuration registers at offsets 0x845 and 0x945.

The configuration register at offset 0x845 allows you to clear all of the TX statistics counters. The configuration register at offset 0x945 allows you to clear all of the RX statistics counters. If you exclude these registers, you can monitor the statistics counter increment vectors that the IP core provides at the client side interface and maintain your own counters.

Reading the value of a statistics register does not affect its value.

To ensure that the counters you read are consistent, you should issue a shadow request to create a snapshot of all of the TX or RX statistics registers, by setting bit [2] of the configuration register at offset 0x845 or 0x945, respectively. Until you reset

(4) X means "Don't Care".

this bit, the counters continue to increment but the readable values remain constant. You can read bit [1] of the status register at offset 0x846 or 0x946, respectively, to confirm your shadow request has been granted or released.

7.5.1. TX Statistics Registers

Table 29. Transmit Side Statistics Registers

Address	Name-	Description	Access
0x800	CNTR_TX_FRAGMENTS_LO	Number of transmitted frames less than 64 bytes and reporting a CRC error (lower 32 bits).	RO
0x801	CNTR_TX_FRAGMENTS_HI	Number of transmitted frames less than 64 bytes and reporting a CRC error (upper 32 bits).	RO
0x802	CNTR_TX_JABBERS_LO	Number of transmitted oversized frames reporting a CRC error (lower 32 bits).	RO
0x803	CNTR_TX_JABBERS_HI	Number of transmitted oversized frames reporting a CRC error (upper 32 bits).	RO
0x804	CNTR_TX_FCS_LO	Number of transmitted packets with FCS errors. (lower 32 bits).	RO
0x805	CNTR_TX_FCS_HI	Number of transmitted packets with FCS errors. (upper 32 bits).	RO
0x806	CNTR_TX_CRCERR_LO	Number of transmitted frames with a frame of length at least 64 reporting a CRC error (lower 32 bits).	RO
0x807	CNTR_TX_CRCERR_HI	Number of transmitted frames with a frame of length at least 64 reporting a CRC error (upper 32 bits).	RO
0x808	CNTR_TX_MCAST_DATA_ERR_LO	Number of errored multicast frames transmitted, excluding control frames (lower 32 bits).	RO
0x809	CNTR_TX_MCAST_DATA_ERR_HI	Number of errored multicast frames transmitted, excluding control frames (upper 32 bits).	RO
0x80A	CNTR_TX_BCAST_DATA_ERR_LO	Number of errored broadcast frames transmitted, excluding control frames (lower 32 bits).	RO
0x80B	CNTR_TX_BCAST_DATA_ERR_HI	Number of errored broadcast frames transmitted, excluding control frames (upper 32 bits).	RO
0x80C	CNTR_TX_UCAST_DATA_ERR_LO	Number of errored unicast frames transmitted, excluding control frames (lower 32 bits).	RO
0x80D	CNTR_TX_UCAST_DATA_ERR_HI	Number of errored unicast frames transmitted, excluding control frames (upper 32 bits).	RO
0x80E	CNTR_TX_MCAST_CTRL_ERR_LO	Number of errored multicast control frames transmitted (lower 32 bits).	RO
0x80F	CNTR_TX_MCAST_CTRL_ERR_HI	Number of errored multicast control frames transmitted (upper 32 bits).	RO
0x810	CNTR_TX_BCAST_CTRL_ERR_LO	Number of errored broadcast control frames transmitted (lower 32 bits).	RO
0x811	CNTR_TX_BCAST_CTRL_ERR_HI	Number of errored broadcast control frames transmitted (upper 32 bits).	RO
0x812	CNTR_TX_UCAST_CTRL_ERR_LO	Number of errored unicast control frames transmitted (lower 32 bits).	RO

continued...

Address	Name-	Description	Access
0x813	CNTR_TX_UCAST_CTRL_ERR_HI	Number of errored unicast control frames transmitted (upper 32 bits).	RO
0x814	CNTR_TX_PAUSE_ERR_LO	Number of errored pause frames transmitted (lower 32 bits).	RO
0x815	CNTR_TX_PAUSE_ERR_HI	Number of errored pause frames transmitted (upper 32 bits).	RO
0x816	CNTR_TX_64B_LO	Number of 64-byte transmitted frames (lower 32 bits), including the CRC field but excluding the preamble and SFD bytes.	RO
0x817	CNTR_TX_64B_HI	Number of 64-byte transmitted frames (upper 32 bits), including the CRC field but excluding the preamble and SFD bytes.	RO
0x818	CNTR_TX_65to127B_LO	Number of transmitted frames between 65–127 bytes (lower 32 bits).	RO
0x819	CNTR_TX_65to127B_HI	Number of transmitted frames between 65–127 bytes (upper 32 bits).	RO
0x81A	CNTR_TX_128to255B_LO	Number of transmitted frames between 128–255 bytes (lower 32 bits).	RO
0x81B	CNTR_TX_128to255B_HI	Number of transmitted frames between 128–255 bytes (upper 32 bits).	RO
0x81C	CNTR_TX_256to511B_LO	Number of transmitted frames between 256–511 bytes (lower 32 bits).	RO
0x81D	CNTR_TX_256to511B_HI	Number of transmitted frames between 256–511 bytes (upper 32 bits).	RO
0x81E	CNTR_TX_512to1023B_LO	Number of transmitted frames between 512–1023 bytes (lower 32 bits).	RO
0x81F	CNTR_TX_512to1023B_HI	Number of transmitted frames between 512–1023 bytes (upper 32 bits).	RO
0x820	CNTR_TX_1024to1518B_LO	Number of transmitted frames between 1024–1518 bytes (lower 32 bits).	RO
0x821	CNTR_TX_1024to1518B_HI	Number of transmitted frames between 1024–1518 bytes (upper 32 bits).	RO
0x822	CNTR_TX_1519toMAXB_LO	Number of transmitted frames of size between 1519 bytes and the number of bytes specified in the MAX_TX_SIZE_CONFIG register (lower 32 bits).	RO
0x823	CNTR_TX_1519toMAXB_HI	Number of transmitted frames of size between 1519 bytes and the number of bytes specified in the MAX_TX_SIZE_CONFIG register (upper 32 bits).	RO
0x824	CNTR_TX_OVERSIZE_LO	Number of oversized frames (frames with more bytes than the number specified in the MAX_TX_SIZE_CONFIG register) transmitted (lower 32 bits).	RO
0x825	CNTR_TX_OVERSIZE_HI	Number of oversized frames (frames with more bytes than the number specified in the MAX_TX_SIZE_CONFIG register) transmitted (upper 32 bits).	RO
0x826	CNTR_TX_MCAST_DATA_OK_LO	Number of valid multicast frames transmitted, excluding control frames (lower 32 bits).	RO
0x827	CNTR_TX_MCAST_DATA_OK_HI	Number of valid multicast frames transmitted, excluding control frames (upper 32 bits).	RO

continued...

Address	Name-	Description	Access
0x828	CNTR_TX_BCAST_DATA_OK_LO	Number of valid broadcast frames transmitted, excluding control frames (lower 32 bits).	RO
0x829	CNTR_TX_BCAST_DATA_OK_HI	Number of valid broadcast frames transmitted, excluding control frames (upper 32 bits).	RO
0x82A	CNTR_TX_UCAST_DATA_OK_LO	Number of valid unicast frames transmitted, excluding control frames (lower 32 bits).	RO
0x82B	CNTR_TX_UCAST_DATA_OK_HI	Number of valid unicast frames transmitted, excluding control frames (upper 32 bits).	RO
0x82C	CNTR_TX_MCAST_CTRL_LO	Number of valid multicast frames transmitted, excluding data frames (lower 32 bits).	RO
0x82D	CNTR_TX_MCAST_CTRL_HI	Number of valid multicast frames transmitted, excluding data frames (upper 32 bits).	RO
0x82E	CNTR_TX_BCAST_CTRL_LO	Number of valid broadcast frames transmitted, excluding data frames (lower 32 bits).	RO
0x82F	CNTR_TX_BCAST_CTRL_HI	Number of valid broadcast frames transmitted, excluding data frames (upper 32 bits).	RO
0x830	CNTR_TX_UCAST_CTRL_LO	Number of valid unicast frames transmitted, excluding data frames (lower 32 bits).	RO
0x831	CNTR_TX_UCAST_CTRL_HI	Number of valid unicast frames transmitted, excluding data frames (upper 32 bits).	RO
0x832	CNTR_TX_PAUSE_LO	Number of valid pause frames transmitted (lower 32 bits).	RO
0x833	CNTR_TX_PAUSE_HI	Number of valid pause frames transmitted (upper 32 bits).	RO
0x834	CNTR_TX_RUNT_LO	Number of transmitted runt packets (lower 32 bits). The IP core does not transmit frames of length less than nine bytes. The IP core pads frames of length nine bytes to 64 bytes to extend them to 64 bytes. Therefore, this counter does not increment in normal operating conditions.	RO
0x835	CNTR_TX_RUNT_HI	Number of transmitted runt packets (upper 32 bits). The IP core does not transmit frames of length less than nine bytes. The IP core pads frames of length nine bytes to 64 bytes to extend them to 64 bytes. Therefore, this counter does not increment in normal operating conditions.	RO
0x836–0x844	Reserved		
0x845	CNTR_TX_CONFIG	Bits[2:0]: Configuration of TX statistics counters: • Bit[2]: Shadow request (active high): When set to the value of 1, TX statistics collection is paused. The underlying counters continue to operate, but the readable values reflect a snapshot at the time the pause flag was activated. Write a 0 to release. • Bit[1]: Parity-error clear. When software sets this bit, the IP core clears the parity bit CNTR_TX_STATUS[0]. This bit (CNTR_TX_CONFIG[1]) is self-clearing. • Bit[0]: Software can set this bit to the value of 1 to reset all of the TX statistics registers at the same time. This bit is self-clearing. Bits[31:3] are Reserved.	RW
0x846	CNTR_TX_STATUS	• Bit[1]: Indicates that the TX statistics registers are paused (while CNTR_TX_CONFIG[2] is asserted). • Bit[0]: Indicates the presence of at least one parity error in the TX statistics counters. Bits[31:2] are Reserved.	RO

continued...

Address	Name-	Description	Access
0x847–0x85F	Reserved		
0x860	TxPayloadOctetsOK_LO	Number of transmitted payload bytes in frames with no FCS, undersized, oversized, or payload length errors. If VLAN detection is turned off for the TX MAC (bit[1] of the TX_MAC_CONTROL register at offset 0x40A has the value of 1), the IP core counts the VLAN header bytes (4 bytes for VLAN and 8 bytes for stacked VLAN) as payload bytes. This register is compliant with the requirements for a OctetsTransmittedOK in section 5.2.2.1.8 of the *IEEE Standard 802.3-2008*.	RO
0x861	TxPayloadOctetsOK_HI		RO
0x862	TxFrameOctetsOK_LO	Number of transmitted bytes in frames with no FCS, undersized, oversized, or payload length errors. This register is compliant with the requirements for ifOutOctets in RFC3635 (Managed Objects for Ethernet-like Interface Types) and TX etherStatsOctets in RFC2819(Remote Network Monitoring Management Information Base (RMON)).	RO
0x863	TxFrameOctetsOK_HI		RO

7.5.2. RX Statistics Registers

Table 30. Receive Side Statistics Registers

Address	Name	Description	Access
0x900	CNTR_RX_FRAGMENTS_LO	Number of received frames less than 64 bytes and reporting a CRC error (lower 32 bits)	RO
0x901	CNTR_RX_FRAGMENTS_HI	Number of received frames less than 64 bytes and reporting a CRC error (upper 32 bits)	RO
0x902	CNTR_RX_JABBERS_LO	Number of received oversized frames reporting a CRC error (lower 32 bits)	RO
0x903	CNTR_RX_JABBERS_HI	Number of received oversized frames reporting a CRC error (upper 32 bits)	RO
0x904	CNTR_RX_FCS_LO	Number of received packets with FCS errors. This register maintains a count of the number of pulses on the l<n>_rx_fcs_error or rx_fcs_error output signal (lower 32 bits)	RO
0x905	CNTR_RX_FCS_HI	Number of received packets with FCS errors. This register maintains a count of the number of pulses on the l<n>_rx_fcs_error output signal (upper 32 bits)	RO
0x906	CNTR_RX_CRCERR_LO	Number of received frames with a frame of length at least 64, with CRC error (lower 32 bits)	RO
0x907	CNTR_RX_CRCERR_HI	Number of received frames with a frame of length at least 64, with CRC error (upper 32 bits)	RO
0x908	CNTR_RX_MCAST_DATA_ERR_LO	Number of errored multicast frames received, excluding control frames (lower 32 bits)	RO
0x909	CNTR_RX_MCAST_DATA_ERR_HI	Number of errored multicast frames received, excluding control frames (upper 32 bits)	RO
0x90A	CNTR_RX_BCAST_DATA_ERR_LO	Number of errored broadcast frames received, excluding control frames (lower 32 bits)	RO
0x90B	CNTR_RX_BCAST_DATA_ERR_HI	Number of errored broadcast frames received, excluding control frames (upper 32 bits)	RO
0x90C	CNTR_RX_UCAST_DATA_ERR_LO	Number of errored unicast frames received, excluding control frames (lower 32 bits)	RO

continued...

Address	Name	Description	Access
0x90D	CNTR_RX_UCAST_DATA_ERR_HI	Number of errored unicast frames received, excluding control frames (upper 32 bits)	RO
0x90E	CNTR_RX_MCAST_CTRL_ERR_LO	Number of errored multicast control frames received (lower 32 bits)	RO
0x90F	CNTR_RX_MCAST_CTRL_ERR_HI	Number of errored multicast control frames received (upper 32 bits)	RO
0x910	CNTR_RX_BCAST_CTRL_ERR_LO	Number of errored broadcast control frames received (lower 32 bits)	RO
0x911	CNTR_RX_BCAST_CTRL_ERR_HI	Number of errored broadcast control frames received (upper 32 bits)	RO
0x912	CNTR_RX_UCAST_CTRL_ERR_LO	Number of errored unicast control frames received (lower 32 bits)	RO
0x913	CNTR_RX_UCAST_CTRL_ERR_HI	Number of errored unicast control frames received (upper 32 bits)	RO
0x914	CNTR_RX_PAUSE_ERR_LO	Number of errored pause frames received (lower 32 bits)	RO
0x915	CNTR_RX_PAUSE_ERR_HI	Number of errored pause frames received (upper 32 bits)	RO
0x916	CNTR_RX_64B_LO	Number of 64-byte received frames (lower 32 bits), including the CRC field but excluding the preamble and SFD bytes	RO
0x917	CNTR_RX_64B_HI	Number of 64-byte received frames (upper 32 bits), including the CRC field but excluding the preamble and SFD bytes	RO
0x918	CNTR_RX_65to127B_LO	Number of received frames between 65–127 bytes (lower 32 bits)	RO
0x919	CNTR_RX_65to127B_HI	Number of received frames between 65–127 bytes (upper 32 bits)	RO
0x91A	CNTR_RX_128to255B_LO	Number of received frames between 128 –255 bytes (lower 32 bits)	RO
0x91B	CNTR_RX_128to255B_HI	Number of received frames between 128 –255 bytes (upper 32 bits)	RO
0x91C	CNTR_RX_256to511B_LO	Number of received frames between 256 –511 bytes (lower 32 bits)	RO
0x91D	CNTR_RX_256to511B_HI	Number of received frames between 256 –511 bytes (upper 32 bits)	RO
0x91E	CNTR_RX_512to1023B_LO	Number of received frames between 512–1023 bytes (lower 32 bits)	RO
0x91F	CNTR_RX_512to1023B_HI	Number of received frames between 512 –1023 bytes (upper 32 bits)	RO
0x920	CNTR_RX_1024to1518B_LO	Number of received frames between 1024–1518 bytes (lower 32 bits)	RO
0x921	CNTR_RX_1024to1518B_HI	Number of received frames between 1024–1518 bytes (upper 32 bits)	RO
0x922	CNTR_RX_1519toMAXB_LO	Number of received frames between 1519 bytes and the maximum size defined in the MAX_RX_SIZE_CONFIG register (lower 32 bits)	RO

continued...

Address	Name	Description	Access
0x923	CNTR_RX_1519toMAXB_HI	Number of received frames between 1519 bytes and the maximum size defined in the MAX_RX_SIZE_CONFIG register (upper 32 bits)	RO
0x924	CNTR_RX_OVERSIZE_LO	Number of oversized frames (frames with more bytes than the number specified in the MAX_RX_SIZE_CONFIG register) received (lower 32 bits)	RO
0x925	CNTR_RX_OVERSIZE_HI	Number of oversized frames (frames with more bytes than the number specified in the MAX_RX_SIZE_CONFIG register) received (upper 32 bits)	RO
0x926	CNTR_RX_MCAST_DATA_OK_LO	Number of valid multicast frames received, excluding control frames (lower 32 bits)	RO
0x927	CNTR_RX_MCAST_DATA_OK_HI	Number of valid multicast frames received, excluding control frames (upper 32 bits)	RO
0x928	CNTR_RX_BCAST_DATA_OK_LO	Number of valid broadcast frames received, excluding control frames (lower 32 bits)	RO
0x929	CNTR_RX_BCAST_DATA_OK_HI	Number of valid broadcast frames received, excluding control frames (upper 32 bits)	RO
0x92A	CNTR_RX_UCAST_DATA_OK_LO	Number of valid unicast frames received, excluding control frames (lower 32 bits)	RO
0x92B	CNTR_RX_UCAST_DATA_OK_HI	Number of valid unicast frames received, excluding control frames (upper 32 bits)	RO
0x92C	CNTR_RX_MCAST_CTRL_LO	Number of valid multicast frames received, excluding data frames (lower 32 bits)	RO
0x92D	CNTR_RX_MCAST_CTRL_HI	Number of valid multicast frames received, excluding data frames (upper 32 bits)	RO
0x92E	CNTR_RX_BCAST_CTRL_LO	Number of valid broadcast frames received, excluding data frames (lower 32 bits)	RO
0x92F	CNTR_RX_BCAST_CTRL_HI	Number of valid broadcast frames received, excluding data frames (upper 32 bits)	RO
0x930	CNTR_RX_UCAST_CTRL_LO	Number of valid unicast frames received, excluding data frames (lower 32 bits)	RO
0x931	CNTR_RX_UCAST_CTRL_HI	Number of valid unicast frames received, excluding data frames (upper 32 bits)	RO
0x932	CNTR_RX_PAUSE_LO	Number of received pause frames, with or without error (lower 32 bits)	RO
0x933	CNTR_RX_PAUSE_HI	Number of received pause frames, with or without error (upper 32 bits)	RO
0x934	CNTR_RX_RUNT_LO	Number of received runt packets (lower 32 bits) A runt is a packet of size less than 64 bytes but greater than eight bytes. If a packet is eight bytes or smaller, it is considered a decoding error and not a runt frame, and the IP core does not flag it nor count it as a runt.	RO
0x935	CNTR_RX_RUNT_HI	Number of received runt packets (upper 32 bits) A runt is a packet of size less than 64 bytes but greater than eight bytes. If a packet is eight bytes or smaller, it is considered a decoding error and not a runt frame, and the IP core does not flag it nor count it as a runt.	RO
0x936–0x944	Reserved		

continued...

Address	Name	Description	Access
0x945	CNTR_RX_CONFIG	Bits[2:0]: Configuration of RX statistics counters: • Bit[2]: Shadow request (active high): When set to the value of 1, RX statistics collection is paused. The underlying counters continue to operate, but the readable values reflect a snapshot at the time the pause flag was activated. Write a 0 to release. • Bit[1]: Parity-error clear. When software sets this bit, the IP core clears the parity bit CNTR_RX_STATUS[0]. This bit (CNTR_RX_CONFIG[1]) is self-clearing. • Bit[0]: Software can set this bit to the value of 1 to reset all of the RX statistics registers at the same time. This bit is self-clearing. Bits[31:3] are Reserved.	RW
0x946	CNTR_RX_STATUS	• Bit[1]: Indicates that the RX statistics registers are paused (while CNTR_RX_CONFIG[2] is asserted). • Bit[0]: Indicates the presence of at least one parity error in the RX statistics counters. Bits [31:2] are Reserved.	RO
0x947–0x95F	Reserved		
0x960	RxPayloadOctetsOK_LO	Number of received payload bytes in frames with no FCS, undersized, oversized, or payload length errors. If VLAN detection is turned off for the RX MAC (bit [1] of the RXMAC_CONTROL register at offset 0x50A has the value of 1), the IP core counts the VLAN header bytes (4 bytes for VLAN and 8 bytes for stacked VLAN) as payload bytes. This register is compliant with the requirements for aOctetsReceivedOK in section 5.2.2.1.14 of the *IEEE Standard 802.3-2008*.	RO
0x961	RxPayloadOctetsOK_HI		RO
0x962	RxFrameOctetsOK_LO	Number of received bytes in frames with no FCS, undersized, oversized, or payload length errors. This register is compliant with the requirements for ifInOctets in RFC3635 (Managed Objects for Ethernet-like Interface Types) and RX etherStatsOctets in RFC2819 (Remote Network Monitoring Management Information Base (RMON)).	RO
0x963	RxFrameOctetsOK_HI		RO

8. Debugging the Link

You can use the Ethernet Link Inspector (ELI) tool to debug your link.

The ELI is an inspection tool that can continuously monitor an Ethernet link that contains an Ethernet IP, which includes Ethernet lane alignment status, clock data recovery (CDR) lock, media access controller (MAC) statistics, Forward Error Correction (FEC) statistics, and others. If needed, the ELI can capture an event with the help of Signal Tap Logic Analyzer to further examine the link behavior during Auto-negotiation (AN), Link Training (LT), or any other event during the link operation. The ELI also creates a graphical user interface (GUI) to represent the link behavior and is available in the Intel Quartus Prime Pro software.

To use ELI, turn on Enable JTAG to Avalon Master Bridge feature in the IP, For more information, refer to the Intel Stratix 10 LL 40GbE IP Core Parameters on page 9.

The following steps should help you identify and resolve common problems that occur when bringing up a Intel Stratix 10 LL 40GbE core link:

1. Establish word lock—The RX lanes should be able to achieve word lock even in the presence of extreme bit error rates. If the IP core is unable to achieve word lock, check the transceiver clocking and data rate configuration. Check for cabling errors such as the reversal of the TX and RX lanes. Check the clock frequency monitors (KHZ_TX, KHZ_RX PHY registers) in the Control and Status registers.

   To check for word lock: Clear the FRM_ERR register by writing the value of 1 followed by another write of 0 to the SCLR_FRM_ERR register at offset 0x324.Then read the FRM_ERR register at offset 0x323. If the value is zero, the core has word lock. If non-zero the status is indeterminate
2. When having problems with word lock, check the EIO_FREQ_LOCK register at address 0x321. The values in this register define the status of the recovered clock. In normal operation, all the bits should be asserted. A non-asserted (value-0) or toggling logic value on the bit that corresponds to any lane, indicates a clock recovery problem. Clock recovery difficulties are typically caused by the following problems:
   - Bit errors
   - Failure to establish the link
   - Incorrect clock inputs to the IP core
3. Check the PMA FIFO levels by selecting appropriate bits in the EIO_FLAG_SEL register and reading the values in the EIO_FLAGS register. During normal operation, the TX and RX FIFOs should be nominally filled. Observing the TX FIFO is either empty or full typically indicates a problem with clock frequencies. The RX FIFO should never be full, although an empty RX FIFO can be tolerated.

4. Establish lane integrity—When operating properly, the lanes should not experience bit errors at a rate greater than roughly one per hour per day. Bit errors within data packets are identified as FCS errors. Bit errors in control information, including IDLE frames, generally cause errors in XL/CGMII decoding.
5. Verify packet traffic—The Ethernet protocol includes automatic lane reordering so the higher levels should follow the PCS. If the PCS is locked, but higher level traffic is corrupted, there may be a problem with the remote transmitter virtual lane tags.
6. Tuning—You can adjust transceiver analog parameters to improve the bit error rate.

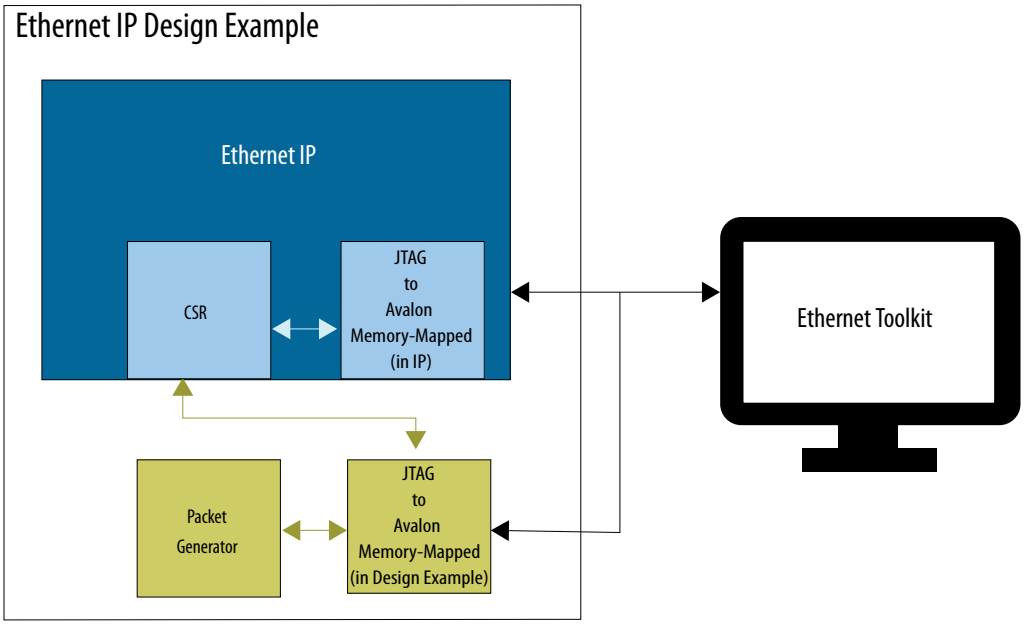
In addition, your IP core can experience loss of signal on the Ethernet link after it is established. In this case, the TX functionality is unaffected, but the RX functionality is disrupted. The following symptoms indicate a loss of signal on the Ethernet link:

- The IP core deasserts the `rx_pcs_ready` signal, indicating the IP core has lost alignment marker lock.
- The IP core deasserts the RX PCS fully aligned status bit (bit [0]) of the `RX_PCS_FULLY_ALIGNED_S` register at offset 0x326. This change is linked to the change in value of the `rx_pcs_ready` signal.
- If **Enable link fault generation** is turned on, the IP core sets `local_fault_status` to the value of 1.
- The IP core triggers the RX digital reset process.

9. Ethernet Toolkit Overview

The Ethernet Toolkit is a TCL based debugging tool that allows you to interact with an Ethernet Intel FPGA IP in real time.

Figure 15. Block Diagram of the Ethernet Toolkit



You can use the Ethernet Toolkit with hardware design that has standalone Ethernet IP. You can also use the Ethernet Toolkit with an Intel Quartus Prime generated Ethernet IP design example.

9.1. Features

The Ethernet Toolkit offers the following features when used with hardware design that has standalone Ethernet IP as well as with an Intel Quartus Prime generated Ethernet IP design example:

- Verifies the status of the Ethernet link.
- Reads and writes to status and configuration registers of the IP.
- Displays the values of TX/RX status and statistics registers.
- Ability to assert and deassert IP resets.
- Verifies the IPs error correction capability.

The Ethernet Toolkit also offers some additional features when used with an Intel Quartus Prime generated Ethernet IP design example:

- Provides access to the example design packet generator.
- Execute testing procedures to verify the functionality of Ethernet IPs.
- Enable and disable MAC loopback.
- Set source and destination MAC addresses.

Related Information

Ethernet Toolkit User Guide

10. Intel Stratix 10 Low Latency 40GbE IP Core User Guide Archives

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme. If an IP core version is not listed, the user guide for the previous IP core version applies.

Intel Quartus Prime Version	IP Core Version	User Guide
20.3	19.1.0	Low Latency 40-Gbps Ethernet Intel Stratix 10 IP Core User Guide
20.2	19.1.0	Low Latency 40-Gbps Ethernet Intel Stratix 10 IP Core User Guide
19.3	19.1.0	Low Latency 40-Gbps Ethernet Intel Stratix 10 IP Core User Guide
17.1 S10 ES	17.1 S10 ES	Low Latency 40-Gbps Ethernet IP Core User Guide 17.1 S10 ES

11. Differences Between Intel Stratix 10 LL 40GbE IP Core and Low Latency 40GbE IP Core That Targets an Arria 10 Device

The Intel Stratix 10 LL 40GbE targets an Intel Stratix 10 device. However, it is not a straightforward Intel Stratix 10 device targeted port of the Low Latency 40GbE IP core that targets an Intel Arria® 10 device. The signals, registers, and register fields are different: you cannot simply substitute the Intel Stratix 10 IP core for the Intel Arria 10 or Stratix V IP core in your design without additional design work.

Table 31. Major Differences Between the Intel Stratix 10 LL 40GbE IP Core and the Low Latency 40GbE IP Core

The comparison is defined relative to these versions:

- Intel Stratix 10 LL 40GbE IP core available with the Quartus Prime Pro 17.1 Stratix 10 ES Editions software.
- Low Latency 40GbE IP core for Intel Arria 10 devices, available with the Intel Quartus Prime software release v17.0.

This table does not list individual signal name and register differences.

Property	Intel Stratix 10 LL 40GbE IP Core	Low Latency 40GbE IP Core For Arria 10 Device
Device support	Supports Intel Stratix 10 device family.	Supports Intel Arria 10 device family.
Reset	Provides three asynchronous hard reset signals (general, RX-only, and TX-only) and three soft reset register bits.	Supports single asynchronous hard reset signal and three soft reset register bits.
Client interface width	Avalon streaming interface 128-bit data bus	Avalon streaming interface 256-bit data bus or custom streaming interface 128-bit data bus.
Avalon streaming TX client interface readyLatency	Avalon streaming TX interface readyLatency configurable at 0 or 3 (parameter).	Avalon streaming TX interface readyLatency is always 0.
Preamble passthrough	Available as a configuration option (parameter). When preamble passthrough is turned on, you must provide the preamble on a separate bus, `l2_tx_preamble[63:0]`, and the IP core provides the RX preamble on a separate bus, `l2_rx_preamble[63:0]`.	Available as a configuration option (parameter). When preamble passthrough is turned on, you must provide the preamble on the TX client interface bus (`l4_tx_data` or `din`), and the IP core provides the preamble on the RX client interface bus (`l4_rx_data` or `dout_d`).
Interface to transceiver TX PLL	You must instantiate a single TX PLL IP core to connect to the single `tx_serial_clk` input pin of the Intel Stratix 10 LL 40GbE IP core.	You can instantiate one to four TX PLL IP cores to connect to the four distinct `tx_serial_clk` input pins of the LL 40GbE IP core.
Statistics counters	Available as a configuration option (parameter).	RX and TX statistics counters available independently as two distinct configuration options (parameters).

continued...

Property	Intel Stratix 10 LL 40GbE IP Core	Low Latency 40GbE IP Core For Arria 10 Device
Statistics counter increment vectors	`l2_txstatus_data`, `l2_txstatus_error`, and `l2_rxstatus_data` signals available on client interface, whether or not statistics registers are enabled.	Individual `tx_inc_` and `rx_inc_` signals available per possible statistics registers, whether or not statistics registers are enabled.
40GBASE-KR4	Available as a configuration option. Configurable support for 40GBASE-KR4 or 40GBASE-CR4. Implements the *IEEE Backplane Ethernet Standard 802.3-2012*.	40GBASE-KR4 available as a configuration option. Implements the *IEEE Backplane Ethernet Standard 802.3ap-2007*.
Flow control	Not yet available in this release.	Available as a configuration option (parameter).
1588 PTP support	Not supported.	N/A
Enable alignment of EOP on FCS word	Always turned on.	Available as a configuration option (parameter).
Minimum average interpacket gap	Value is 12 bytes.	Values none (single byte), 8 bytes, and 12 bytes available as configuration options (parameter).

Related Information

Low Latency 40-Gbps Ethernet IP Core User Guide

12. Document Revision History for Low Latency 40-Gbps Ethernet Intel Stratix 10 IP Core

Date	Intel Quartus Prime Version	IP version	Changes
2021.03.08	20.3	19.1.0	Removed the `.sip` file type from section: *Generated File Structure*.
2020.10.05	20.3	19.1.0	• Corrected the width of the reconfiguration address from `reconfig_address[10:0]` to `reconfig_address[12:0]`. • Removed outdated **Use debug CPU** parameter from the *Intel Stratix 10 LL 40GbE IP Core Parameters: 40GBASE-KR4/CR4 Tab* table. • Revised the *Flow Control Signals* table to update the following signals description: — `pause_insert_tx0[(FCQN-1):0]` — `pause_insert_tx1[(FCQN-1):0]` — `pause_insert_rx[(FCQN-1):0]` • Added new section: *Ethernet Toolkit Overview*.
2020.06.22	20.2	19.1.0	• Updated the *Intel Stratix 10 LL 40GbE IP Core Parameters: Main Tab* table to include the following parameters: — **Enable MAC flow control** — **Number of queues in priority flow control** — **Enable JTAG to Avalon Master Bridge** • Updated the *Intel Stratix 10 LL 40GbE Signals and Interfaces* figure: — Added missing flow control signals — Removed undirectional support and link fault signals. • Added new section: *Flow Control Interface*.

continued...

Date	Intel Quartus Prime Version	IP version	Changes
			• Removed `undirectional_en` and `link_fault_gen_en` signals from the *Avalon Memory-Mapped Interface Interface* table. • Added `EIO_RX_SOFT_PURGE_S` register description in the *PHY Registers* table. • Revised `clk_status` frequency range in the *Avalon Memory-Mapped Management Interface* table. The frequency of this clock is 100-161 MHz.
2019.12.13	19.3	19.1.0	• Added note clarifying auto adaptation support in the *Transceiver Reconfiguration Signals* section. • Rebranded Qsys to Platform Designer (Standard).
2019.09.30	19.3	19.1.0	• Replaced **Altera Debug Master Endpoint (ADME)** with **Native PHY Debug Master Endpoint (NPDME)**. • Removed note from **Auto-Negotiation Master** parameter in the *Intel Stratix 10 LL 40 GbE IP Core Parameters: 40GBASE-KR4/CR4 Tab* table. • Added *Intel Stratix 10 Low Latency 40G Ethernet FPGA IP Core User Guide Archives*. • Added Ethernet Link Inspector support in the *Debugging the Link* section. • Remove mention of 1588 PTP support in the *Major Differences Between the Intel Stratix 10 LL 40GbE IP Core and the Low Latency 40GbE IP Core* table.

Date	Version	Changes
2017.05.08	Quartus Prime Pro 17.1 Stratix 10 ES Editions	• Updated for new Quartus Prime Pro 17.1 Stratix 10 ES Editions release. • Added option for Synchronous Ethernet support. Documented new **Enable SyncE** parameter and new `clk_rx_recover` output signal. Described expected usage in Clocks. Refer also to Intel Stratix 10 LL 40GbE IP Core Supported Features on page 4, and Intel Stratix 10 LL 40GbE IP Core Parameters on page 9. • Added option for 40GBASE-KR4/CR4 IP core variation. Documented new parameters to control this feature in Intel Stratix 10 LL 40GbE IP Core Parameters on page 9. Updated Intel Stratix 10 LL 40GbE IP Core Supported Features on page 4 to list the new feature. Added new sections Clock Requirements for 40GBASE-KR4/CR4 Variations on page 20, Intel Stratix 10Low Latency 40GBASE-KR4 IP Core Variations on page 30, and Intel Stratix 10 LL 40GBASE-KR4/CR4 Registers on page 45. • Added shadow feature for reading statistics registers. Replaced the `CLEAR_TX_STATS` and `CLEAR_RX_STATS` registers with new `CNTR_TX_CONFIG` and `CNTR_RX_CONFIG` registers at offsets 0x845 and 0x945. Added new `CNTR_TX_STATUS` and `CNTR_RX_STATUS` registers at offsets 0x846 and 0x946, respectively . Refer to Statistics Registers on page 66. • Added option for strict SFD checking. The feature adds two new fields in the `RX_MAC_CONTROL` register at offset 0x50A. Refer to IP Core Strict SFD Checking on page 26, RX MAC Registers on page 65, Intel Stratix 10 LL 40GbE IP Core Supported Features on page 4, and Intel Stratix 10 LL 40GbE IP Core Parameters on page 9. • Added malformed packet checking. Refer to IP Core Malformed Packet Handling, the updated description of `l2_rx_error[0]` in RX MAC Interface to User Logic on page 37, and Intel Stratix 10 LL 40GbE IP Core Supported Features on page 4.

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Date	Version	Changes
		• Added simulation optimization RTL parameter SIM_SHORT_RST. Refer to Simulating the IP Core on page 15. • Added auto-negotiation and link training simulation control RTL parameter ALTERA_RESERVED_XCVR_FULL_KR_TIMERS for 40GBASE-KR4/CR4 variations. Refer to Simulating the IP Core on page 15. • Clarified that the design example includes SDC files that you can modify for your own design. Refer to Compiling the Full Design and Programming the FPGA on page 21.
2016.09.09	Quartus Prime Pro-Stratix 10 Edition Beta	Initial release.