SmartVID Controller IP Core User Guide

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2014.12.15

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SmartVID Controller Overview

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The SmartVID Controller IP core computes Voltage Identification (VID) values determined through on-die fuse value and temperature-specific algorithm.

The VID computing algorithm is required by on-die temperature, die characteristics and settings.

Item		Description
Release Information	Version	14.1
	Release	December 2014
	Product ID	FFFF
IP Core Information	Core Features	• Enables computation delay and computed VID code magnitude adjustment. • • Lowers voltage according to the temperature obtained from the Temperature Sensor
	Device Family	Supports Arria 10 devices
	Device Tools	• Quartus II software for IP design instantiation and compilation • Temperature Sensor IP core

SmartVID Controller Getting Started 2

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The SmartVID Controller IP core is installed as part of the Quartus II installation process.

IP Catalog and Parameter Editor

The Quartus II IP Catalog (**Tools** > **IP Catalog**) and parameter editor help you easily customize and integrate IP cores into your project. You can use the IP Catalog and parameter editor to select, customize, and generate files representing your custom IP variation.

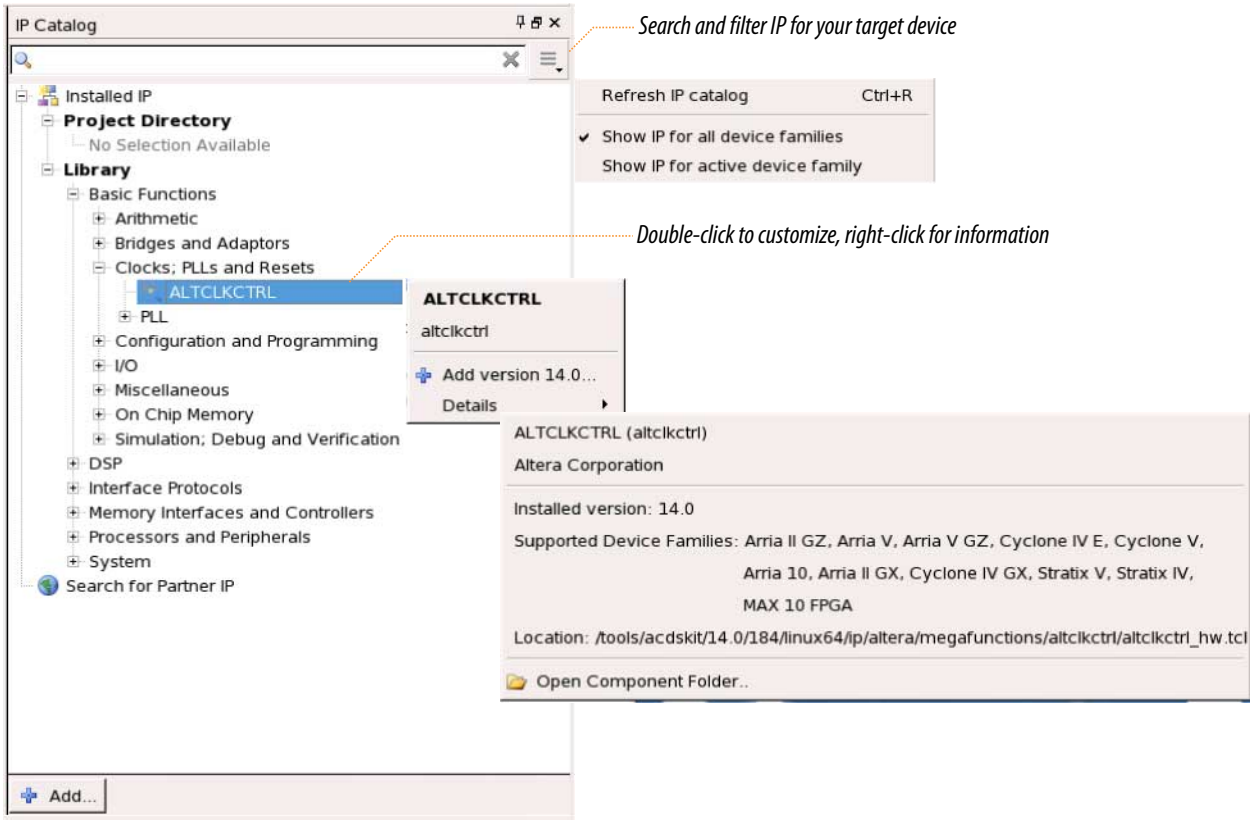
Note: The IP Catalog (**Tools** > **IP Catalog**) and parameter editor replace the MegaWizard™ Plug-In Manager for IP selection and parameterization, beginning in Quartus II software version 14.0. Use the IP Catalog and parameter editor to locate and paramaterize Altera IP cores.

The IP Catalog lists IP cores available for your design. Double-click any IP core to launch the parameter editor and generate files representing your IP variation. The parameter editor prompts you to specify an IP variation name, optional ports, and output file generation options. The parameter editor generates a top-level Qsys system file (**.qsys**) or Quartus II IP file (**.qip**) representing the IP core in your project. You can also parameterize an IP variation without an open project.

Use the following features to help you quickly locate and select an IP core:

- Filter IP Catalog to **Show IP for active device family** or **Show IP for all device families**.
- Search to locate any full or partial IP core name in IP Catalog. Click **Search for Partner IP**, to access partner IP information on the Altera website.
- Right-click an IP core name in IP Catalog to display details about supported devices, open the IP core's installation folder, andor view links to documentation.

Figure 2-1: Quartus II IP Catalog



Note: The IP Catalog is also available in Qsys (**View** > **IP Catalog**). The Qsys IP Catalog includes exclusive system interconnect, video and image processing, and other system-level IP that are not available in the Quartus II IP Catalog. For more information about using the Qsys IP Catalog, refer to *Creating a System with Qsys* in the *Quartus II Handbook*.

Specifying Parameters and Options

Follow these steps to specify the SmartVID Controller parameters and options.

1. Create a Quartus II project using the **New Project Wizard** available from the File menu.
2. On the **Tools** menu, click **IP Catalog**.
3. Under **Installed IP**, double-click **Library** > **Low Power** > **SmartVID Controller IP**. The parameter editor appears.
4. Specify a top-level name for your custom IP variation. This name identifies the IP core variation files in your project. If prompted, also specify the targeted Altera device family and output file HDL preference. Click **OK**.
5. Specify parameters and options in the SmartVID Controller parameter editor:

- Specify parameters defining the IP core functionality, port configurations, and device-specific features.
- Specify options for generation of a timing netlist, simulation model, testbench, or example design (where applicable).
- Specify options for processing the IP core files in other EDA tools.

6. Click **Generate** to generate the IP core and supporting files, including simulation models.
7. Click **Close** when file generation completes.
8. Click **Finish**.
9. If you generate the SmartVID Controller instance in a Quartus II project, you are prompted to add **Quartus II IP File (.qip)** and **Quartus II Simulation IP File (.sip)** to the current Quartus II project.

SmartVID Controller Parameters

You can use the GUI parameters to configure the SmartVID Controller IP core.

Table 2-1: SmartVID Controller Parameters

The table below lists the options in the SmartVID Controller parameter editor.

Parameters	Value	Description
Device family	Arria 10	This IP core is specifically for Arria 10 devices.
Core speed grade	–3, –2, or –1	Select the core fabric speed grade of the FPGA. **Note:** If you select –1, the AVS feature will not be enabled.
Enable AVS feature	**On** or Off	Turn on this option to enable the Adaptive Voltage Scaling (AVS) feature. **Note:** When you turn on the AVS feature, ensure that `ENABLE_SMART_VOLTAGE_ID` is set to `ON` in the **Quartus Setting File (QSF)**.
Bypass VID Controller configuration register programming	**On** or Off	• Turn on this option to allow the IP core to start operation after it is out of reset. The IP core will start operating immediately based on your settings. • Turn off this option if you do not want the IP core to start operation until the configuration registers are fully programmed.

If you use the parameter editor to configure the SmartVID Controller IP core, the following VID parameters have fixed values:

- Temperature-dependent VID: On
- VID computation delay: 0
- VID step size: 2 steps (5 mV per step)

Note: To configure these VID parameters, use the configuration registers.

Related Information

- **SmartVID Controller Registers** on page 5-1

SmartVID Functional Description

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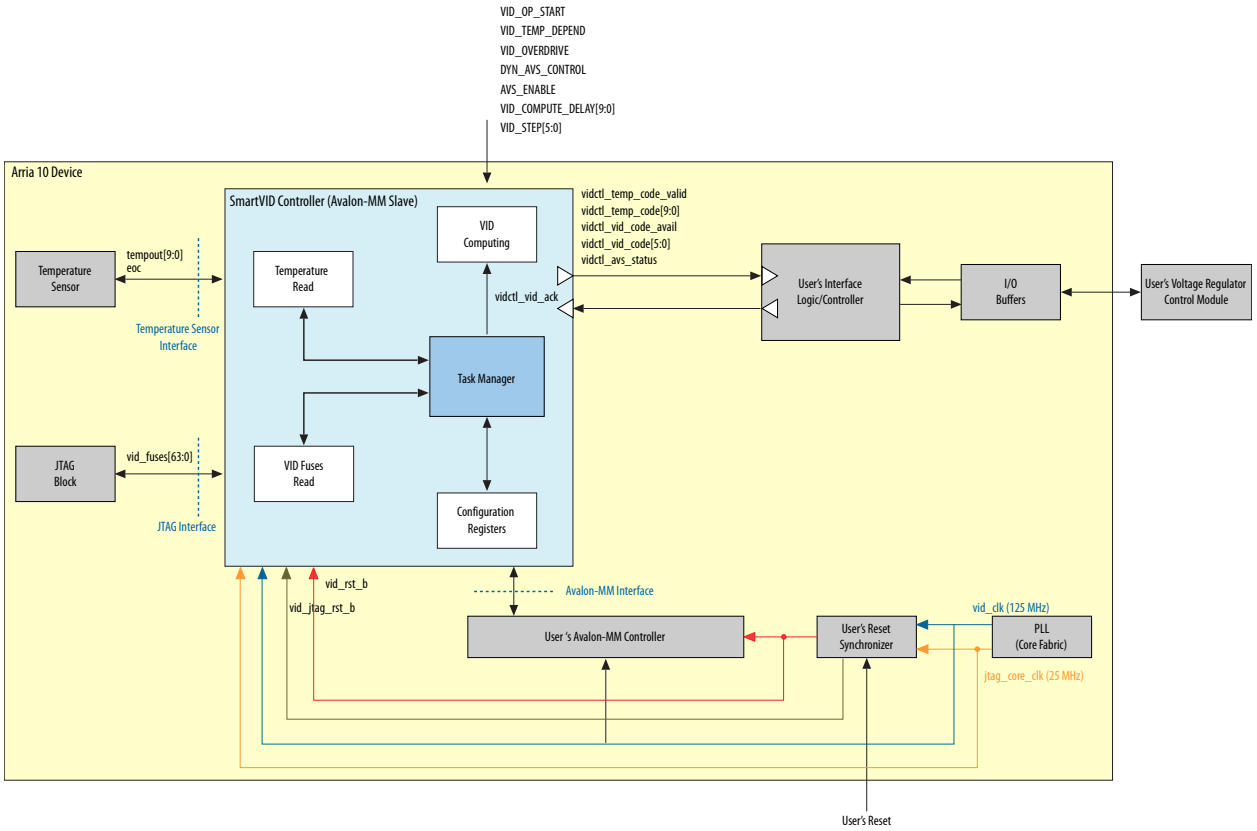
The SmartVID Controller IP core connects to the other sub-systems in a device.

Figure 3-1: SmartVID Controller System with Arria 10 Device

The figure below shows the system-level block diagram of Arria 10 SmartVID with the interfacing sub-systems.



Temperature Sensor

The Temperature Sensor IP core provides a 10-bit digital representation of the on-die temperature.

The SmartVID Controller IP core connects to the Temperature Sensor IP core. When you instantiate the Temperature Sensor IP core, it periodically produces a digitized on-die temperature value `tempout[9:0]` every 1024 clock cycles in the 1MHz clock domain.

The covered temperature range is –40°C to 125°C. The `eoc` signal asserts for 1 clock cycle to indicate a valid new `tempout[9:0]` value. The new value remains static until you assert the `eoc` signal again.

The SmartVID Controller IP core regularly samples valid `tempout[9:0]` for VID computation purposes. You can calculate the temperature from `tempout[9:0]` value using this formula:

```
Temperature = ((A×C)÷1024)–B
```

Where:

- A = 708
- B = 273
- C = decimal value of `tempout[9:0]`

Note: `tempout[9:0]` may not represent the hottest spot of the Arria10 device because the temperature sensor is located at the edge of the die.

tempout[9:0]	Decimal Value of tempout[9:0]	Temperature (°C)	Two's Complement
01 0101 0100	341	-40	11 1101 1000
10 0000 0000	512	78	00 0100 1110
10 0100 0100	580	125	00 0111 1101

Related Information

Temperature Sensor (ALTTEMP_SENSE) IP Core User Guide
Provides more information about the Temperature Sensor IP core.

JTAG Block

The SmartVID Controller IP core retrieves the required fuse values from the JTAG block in the Arria 10 device for its operation.

When retrieving the VID fuses, you must ensure that there are no other applications accessing these VID fuse banks at the same time.

Related Information

Power Management in Arria 10 Devices
Provides more information about the JTAG block in Arria 10 devices.

Clocks and Reset

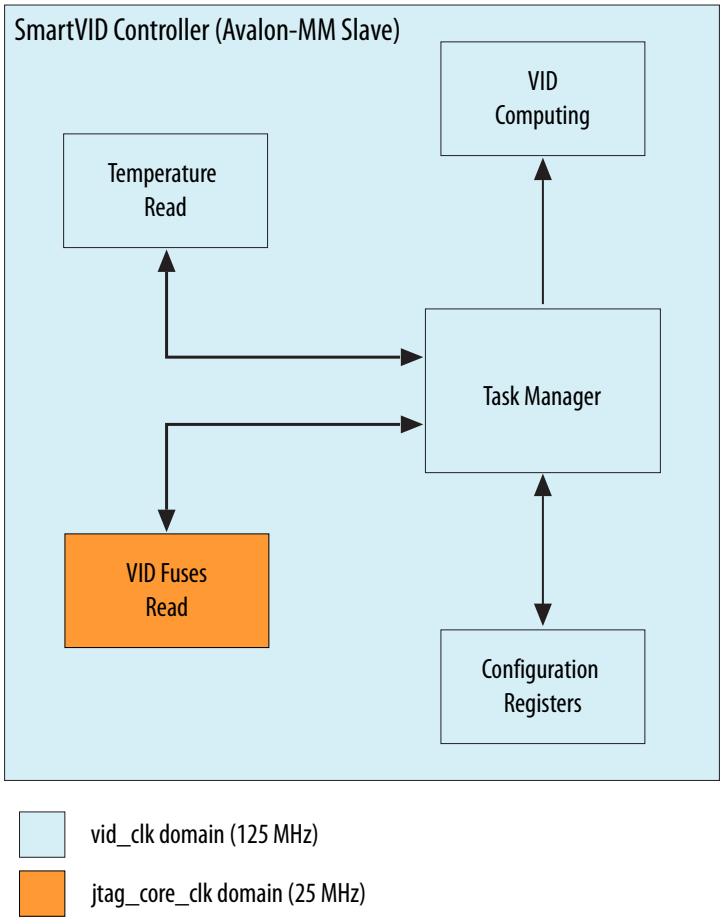
The core fabric phase-locked loop (PLL) supplies two clocks for the SmartVID Controller IP core.

Table 3-1: Clock Functions

Clock	Description
`vid_clk`	Asynchronous clock with frequency of 125 MHz.
`jtag_core_clk`	Asynchronous clock with frequency of 25 MHz.

The SmartVID Controller IP core synchronizes the `vid_clk` and `jtag_core_clk` domains in your design's sub-system to the external reset that you set.

Figure 3-2: Clock Connections



Ensure that you deassert the external reset only when these conditions are met:

- The Arria 10 device is in user mode.
- Both `vid_clk` and `jtag_core_clk` have at least toggled for 10 clock cycles each.

Also ensure that after you assert the external reset, both `vid_clk` and `jtag_core_clk` toggle at least for 10 clock cycles each.

System Power-On

You may set the SmartVID Controller IP core's configuration register `CC1[0]` after programming all other configuration registers.

Figure 3-3: Power-On Sequence

The figure below shows the power-on expected sequence of the SmartVID Controller IP core and external controllers, together with the relevant Arria 10 sub-systems.

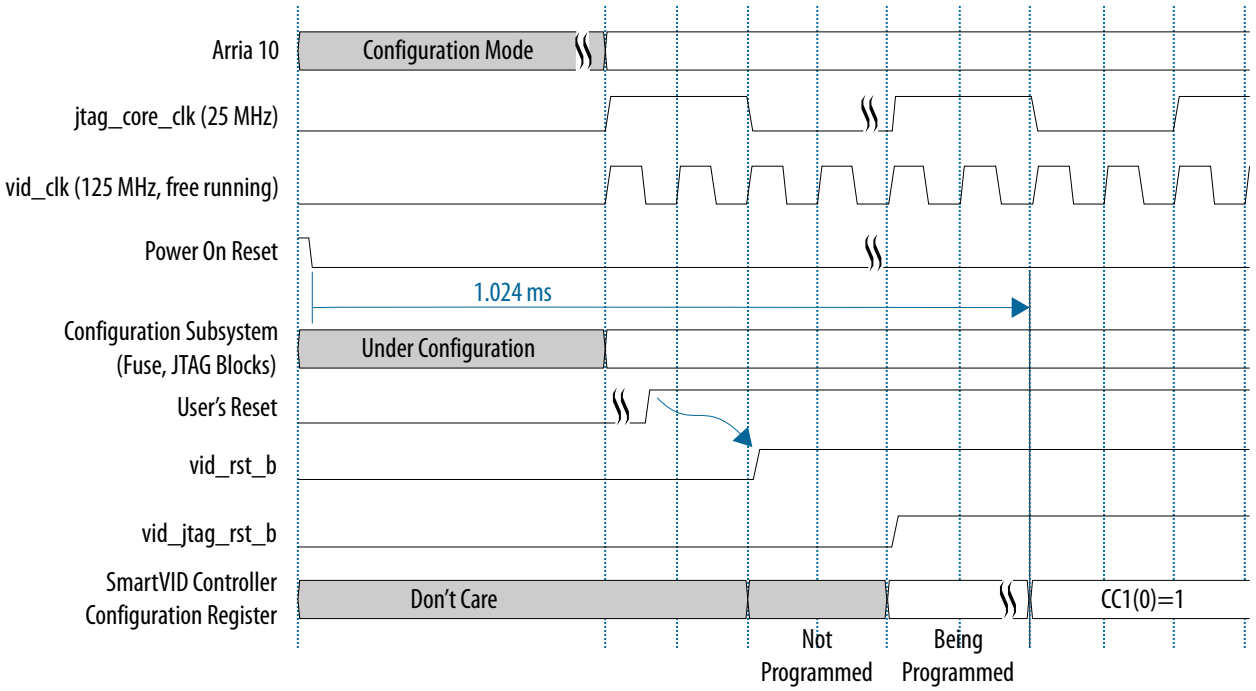
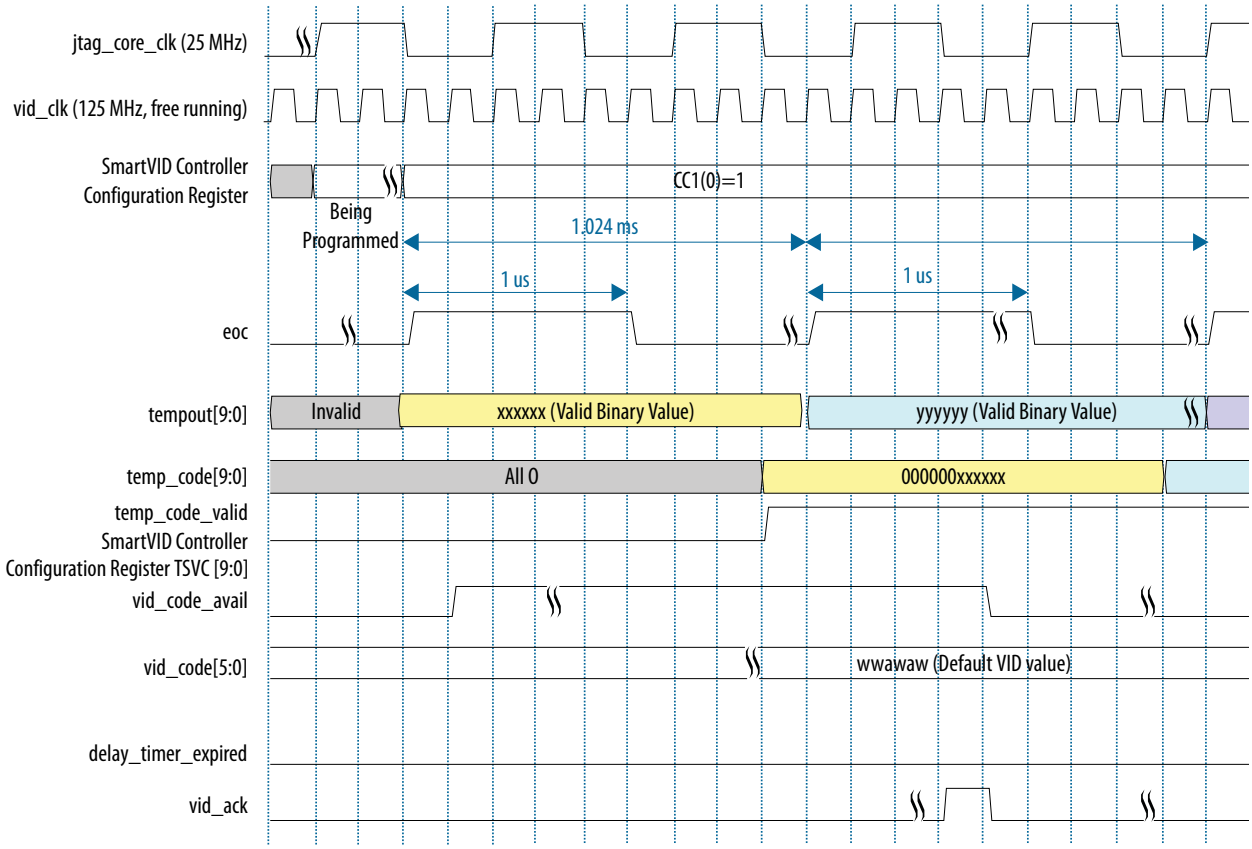


Figure 3-4: Operation Behavior

The figure below shows the operation behavior of the SmartVID Controller IP core with the relevant Arria 10 sub-systems.



The Temperature Sensor IP core starts operation after Power On Reset (POR) in the Arria 10 device deasserts in configuration mode. When the Arria 10 device is in user mode and you deassert the external reset, the SmartVID Controller IP core starts sampling for valid `tempout[9:0]`. When configuration register `CC1[0]` is 1, the IP core initiates VID fuse-read. The SmartVID Controller IP core then switches to AVS VID mode when the following conditions are met:

- AVS logic enabled.
- The external controller reads out the SVS-VID value and asserts `vidctl_vid_ack`.
- The duration specified in the configuration register `CC2[20:1]` elapses.

SmartVID Controller Interface Signals

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The SmartVID Controller IP core uses the interface signals to connect with the other sub-systems in the Arria 10 device.

Table 4-1: Input and Output Signals for the SmartVID Controller IP Core

Signal	Direction	Clock Domain	Description
`vid_clk`	Input	—	Requires 125MHz clock. Most of the functional blocks in the IP core use this clock.
`jtag_core_clk`	Input	—	Requires 25MHz clock. The fuse-read logic in the IP core uses this clock.
`vid_rst_b`	Input	vid_clk	An active-low reset synchronized to `vid_clk` domain. You provide the reset.
`vid_jtag_rst_b`	Input	jtag_core_clk	An active-low reset synchronized to `jtag_core_clk` domain. You provide the reset.
`vidctl_avmm_writedata[31:0]`	Input	vid_clk	Write data from the Avalon-MM Master to the SmartVID controller.
`vidctl_avmm_read`	Input	vid_clk	Read-transfer indication from the Avalon-MM Master to the SmartVID controller.
`vidctl_avmm_write`	Input	vid_clk	Write-transfer indication from the Avalon-MM Master to the SmartVID controller.
`vidctl_avmm_address[2:0]`	Input	vid_clk	The Avalon-MM Master address for data transfer to/from SmartVID controller (which is an AV-MM Slave). This is a word address.
`vidctl_avmm_readdata[31:0]`	Output	vid_clk	Read data from SmartVID controller to Avalon-MM Master.

Signal	Direction	Clock Domain	Description
vidctl_tdocore	Input	jtag_core_clk	Connect this signal to the tdocore port of the JTAG atom. • FPGA to HPS JTAG chaining FPGA core firewall TDI input –> TDO output from FPGA JTAG to core • FPGA to HPS JTAG chaining FPGA core firewall TDI input –> TDI input to HPS JTAG
vidctl_ntrstcore	Output	jtag_core_clk	Connect this signal to the ntrstcore port of the JTAG atom. • HPS JTAG Master FPGA core firewall NTRST output –> from core to FPGA JTAG
vidctl_tckcore	Output	jtag_core_clk	Connect this signal to the tckcore port of the JTAG atom. • HPS JTAG Master FPGA core firewall TCK output –> from core to FPGA JTAG
vidctl_corectl_jtag	Output	jtag_core_clk	Connect this signal to the corectl port of the JTAG atom. Dynamic FPGA core firewall enable.
vidctl_tmscore	Output	jtag_core_clk	Connect this signal to the tmscore port of the JTAG atom. • HPS JTAG Master FPGA core firewall TMS output –> from core to FPGA JTAG
vidctl_tdicore	Output	jtag_core_clk	Connect this signal to the tdicore port of the JTAG atom. • HPS JTAG Master FPGA core firewall TDI output –> from core to FPGA JTAG
vidctl_vid_ack	Input	vid_clk	Your controller should send a pulse to this signal when the vidctl_vid_code signal is sampled and sent to the voltage regulator.
vidctl_temp	Input	vid_clk	Connect this signal to the tempout port of the temperature sensor. This is the temperature code output from temperature sensor.

Signal	Direction	Clock Domain	Description
vidctl_eoc	Input	vid_clk	Connect this signal to the eoc port of the temperature sensor. This is the end of conversion signal from temperature sensor.
vidctl_temp_sense_enable	Output	vid_clk	Connect this signal to the corectl port of the temperature sensor. This is a core enable signal from the core to the temperature sensor.
vidctl_temp_sense_reset	Output	vid_clk	Connect this signal to the reset port of the temperature sensor. This is the reset signal from the core to the temperature sensor.
vidctl_vid_code_avail	Output	vid_clk	Your controller may sample the vid_code when this signal is asserted.
vidctl_avs_status	Output	vid_clk	When you assert this signal, the AVS mode is enabled.
vidctl_vid_code	Output	vid_clk	This is a 6-bit VID code from the SmartVID controller.
vidctl_temp_code	Output	vid_clk	This is a 10-bit temperature code from the SmartVID controller.
vidctl_temp_code_valid	Output	vid_clk	This signal indicates whether the temp_code value is valid.

SmartVID Controller Registers 5

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The SmartVID Controller IP core uses the Avalon Memory-Mapped (Avalon-MM) interface for read and write operations in a memory-mapped system.

The 32-bit non-bursting Avalon-MM slave interface allows upstream to access internal control and status register.

The SmartVID Controller IP supports a basic one clock cycle transaction bus. Avalon-MM slave interface does not support byte enable access. Avalon-MM slave read and write data width is 32 bits (DWORD access).

Note: The control data is read once at the start of each frame and is buffered inside the IP core, so the registers can be safely updated during the processing of a frame.

Table 5-1: SmartVID Controller Register Map

The table below lists the registers for the SmartVID Controller IP core.

Address Offset	Register	Description
0×0	`Capabilities and Control 1 (CC1)`	Configures the capabilities of SmartVID Controller IP core.
0×1	`Capabilities and Control 2 (CC2)`	
0×2	`Capabilities and Control 3 (CC3)`	
0×3	`VID Fuse1 (VF1)`	Stores VID fuse values [31:0]
0×4	`VID Fuse2 (VF2)`	Stores VID fuse values [63:32]
0×5	`Temperature and Computed VID Codes (TCVC)`	Stores a sampled temperature code, and a computed VID code.

Table 5-2: Capabilities and Control 1 (CC1) Register

Address	Register	RO/RW	Description
31:3	Reserved	RO	This register is reserved for future use.
2	Temperature-dependent AVS-VID computation (`VID_TEMP_DEPEND`)	RO	This register is reserved for future use.

Address	Register	RO/RW	Description
1	Temperature Sensor Enable	RW1	A policy bit that governs whether the temperature sensor of the Arria 10 device is enabled in user mode. • 0: Temperature sensor is disabled. • 1: Temperature sensor is enabled. **Note:** The temperature codes from the temperature sensor are also used by other Arria 10 sub-systems. Clear this bit only if enabling the temperature sensor may cause unexpected issues to the Arria 10 device.
0	SmartVID Controller Start Operations (`VID_OP_START`)	RW1	A policy bit that determines whether the IP core can start operating when it is out of reset. **Note:** Set this to 1 only after programming all other configuration registers for this IP core.

Table 5-3: Capabilities and Control 2 (CC2) Register

Address	Register	RO/RW	Description
31:17	Reserved	RO	This register is reserved for future use.
26:21	VID Step Size (`VID_STEP`)	RW	These bits determine the final adjustment magnitude of the computed VID code at the end of each computation, if applicable. Each step represents a 5 mV change. Value: 000001 — Adjustment Magnitude: 5 mV Value: 000010 — Adjustment Magnitude: 10 mV Value: 000011 — Adjustment Magnitude: 15 mV
20:1	VID Computation Delay (`VID_COMPUTE_DELAY`)	RW	These bits represent the duration that must elapse (in µs) before a new VID code is computed. Ensure that this computation delay is longer than the time required for the following tasks: **Note:** For optimum system considerations, you are recommended to program this computation delay to 1 ms, 10 ms, 100 ms, or 1 second interval, instead of at µs range.
0	Dynamic AVS Feature Control (`DYN_AVS_CONTROL`)	RW	This bit dynamically enables or disables the AVS feature. • 0: AVS feature is disabled. • 1: AVS feature is enabled. **Note:** The AVS logic in the SmartVID Controller IP core is only enabled when CC2[0], CC3[3], CC3[16], and VF1[4] bits are set to 1.

Table 5-4: Capabilities and Control 3 (CC3) Register

Address	Register	RO/RW	Description
31:17	Reserved	RO	This register is reserved for future use.
16	Device Supports AVS Feature (DEVICE_SUPPORTS_AVS)	RW	This policy bit determines if the AVS feature of the SmartVID Controller IP core can be enabled. • 0: AVS feature is disabled. • 1: AVS feature is enabled. **Note:** The AVS logic in the SmartVID Controller IP core is only enabled when CC2[0], CC3[3], CC3[16], and VF1[4] bits are set to 1.
15:10	Live VID Code (VID_DEFAULT)	RO	This bit indicates the live VID code produced by the SmartVID Controller IP core. This live code may be in either SVS or AVS mode.
9:4	Default VID Value (VID_DEFAULT)	RO	These bits indicate the default VID value.
3	AVS Feature Enable (AVS_ENABLE)	RO	This policy bit determines if the AVS feature of the SmartVID Controller IP core can be enabled. **Note:** The AVS logic in the SmartVID Controller IP core is only enabled when CC2[0], CC3[3], CC3[16], and VF1[4] bits are set to 1.
2:1	Core Speed Grade (CORE_SPEED_GRADE)	RO	These bits indicate the core fabric speed grade of the FPGA device. 00 –3 11 –2 10 –1 01 Reserved
0	Reserved	RO	This register is reserved for future use.

Table 5-5: VID Fuse1 (VF1) Register

Address	Register	RO/RW	Description
31	Reserved	RO	This register is reserved for future use.
30	VID Fuses Valid	RO	This bit indicates whether the non-reserved fields of this register have valid values or not. • 0: Values of non-reserved fields of this register are invalid. • 1: Values of non-reserved fields of this register are valid.

Address	Register	RO/RW	Description
29:24	VID For Dash –1 Core Speed Grade	RO	These bits are mapped to the retrieved VID Fuse[29:24], which represent the VID code for –1 core speed grade. Refer to Table 5. **Note:** The values of these bits are valid only if you set bit VF1[30] to 1.
23:22	Reserved	RO	This register is reserved for future use.
21:16	VID For Dash –2 Core Speed Grade	RO	These bits are mapped to the retrieved VID Fuse[21:16], which represent the VID code for –2 core speed grade. Refer to Table 5-6. **Note:** The values of these bits are valid only if you set bit VF1[30] to 1.
15:14	Reserved	RO	This register is reserved for future use.
13:8	VID For Dash –3 Core Speed Grade	RO	These bits are mapped to the retrieved VID Fuse[13:8], which represent the VID code for –3 core speed grade. Refer to Table 5-6. **Note:** The values of these bits are valid only if you set bit VF1[30] to 1.
7:5	Reserved	RO	This register is reserved for future use.
4	AVS Feature Enable Via Fuse	RO	This bit is mapped to the retrieved VID Fuse[4], which determines if the AVS feature of the SmartVID Controller IP core can be enabled. • 0: AVS feature is disabled. • 1: AVS feature is enabled. **Note:** The AVS logic in the SmartVID Controller IP core is only enabled when CC2[0], CC3[3], CC3[16], and VF1[4] bits are set to 1. **Note:** The value of this bit is valid only if you set bit VF1[30] to 1.
3:0	Reserved	RO	This register is reserved for future use.

Table 5-6: VID Codes for Arria 10 Speed Grades

VID Code (Binary)	Voltage (V)
011100	0.800
011101	0.805
011110	0.810
011111	0.815
100000	0.820
100001	0.825

VID Code (Binary)	Voltage (V)
100010	0.830
100011	0.835
100100	0.840
100101	0.845
100110	0.850
100111	0.855
101000	0.860
101001	0.865
101010	0.870
101011	0.875
101100	0.880
101101	0.885
101110	0.890
101111	0.895
110000	0.900
110001	0.905
110010	0.910
110011	0.915
110100	0.920
110101	0.925
110110	0.930
110111	0.935
111000	0.940
111001	0.945
111010	0.950
111011	0.955
111100	0.960
111101	0.965
111110	0.970
111111	0.975

Table 5-7: VID Fuse2 (VF2) Register

Address	Register	RO/RW	Description
31:0	Reserved	RO	This register is reserved for future use.

Table 5-8: Temperature and Computed VID Codes (TCVC) Register

Address	Register	RO/RW	Description
31:28	Reserved	RO	This register is reserved for future use.
27	AVS Status	RO	This bit indicates the operating state of the SmartVID Controller IP core AVS logic. • 0: AVS logic is fully deactivated. • 1: AVS logic is active.
26:17	Temperature Used In AVS VID Computation	RO	These bits capture the temperature code used in the latest computed VID code when AVS logic is active. This information is intended for correlation and debugging purposes. **Note:** These bits will be set to 0 if CC1[1] and CC1[2] bits are 0 and the AVS logic is fully deactivated.
16	Temperature Code Valid	RO	This bit indicates whether TCVC[9:0] has a valid temperature code. • 0: TCVC[9:0] value is invalid. • 1: TCVC[9:0] value is valid. **Note:** This bit is set to 0 if CC1[1] is 0.
15:10	Latest Computed VID Code in AVS mode	RO	These bits indicate the latest computed VID code when AVS logic is active. **Note:** Bit [27] of this register indicates whether the AVS logic is active or fully deactivated. **Note:** These bits will be set to 0 if the AVS logic is fully deactivated.
9:0	Temperature Code	RO	These bits indicate the periodically sampled temperature code output by the temperature sensor. **Note:** These bits are set to 0 if CC1[1] is 0.

Additional Information for SmartVID Controller IP Core User Guide

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Additional information about the document and Altera.

Document Revision History for SmartVID Controller User Guide

Date	Version	Changes
December 2014	2014.12.15	Initial release.

How to Contact Altera

Table A-1: Altera Contact Information

Contact[1]		Contact Method	Address
Technical support		Website	www.altera.com/support
Technical training		Website	www.altera.com/training
		Email	custrain@altera.com
Product literature		Website	www.altera.com/literature
Nontechnical support	General	Email	nacomp@altera.com
	Software licensing	Email	apgcs@altera.com

Related Information

- www.altera.com/support
- www.altera.com/training
- www.altera.com/literature

(1) You can also contact your local Altera sales office or sales representative.