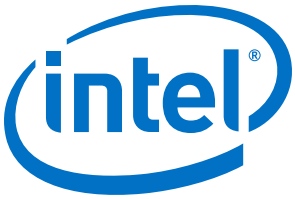

Stratix 10 Serial Flash Mailbox Client Intel FPGA IP Core User Guide

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Contents

Stratix 10 Serial Flash Mailbox Client Intel FPGA IP Core User Guide

The Stratix 10 Serial Flash Mailbox Client Intel FPGA IP core provides access to the low-voltage quad-serial configuration (EPCQ-L) device via Intel® Stratix® 10 devices.

Note: Contact your local Intel sales representative for more information about flash device support other than the EPCQ-L devices.

The Stratix 10 Serial Flash Mailbox Client Intel FPGA IP core supports:

- Direct flash access (write and read) through the Avalon-Memory Map (Avalon-MM) interface
- Control register for other operations through the control status register (CSR) interface in Avalon-MM
- 4 KB data for each write or read operation
- Supported operations (refer to the respective flash device datasheet for a complete list of supported operations):
  - Open
  - Close
  - Set chip select
  - Read data from flash
  - Write data to flash
  - Erase sector
  - Read device register
  - Write device register
  - Send device opcode

Related Information

Introduction to Intel FPGA IP Cores
Provides general information about all Intel FPGA IP cores, including parameterizing, generating, upgrading, and simulating IP cores.

Signals

Figure 1. Signal Block Diagram

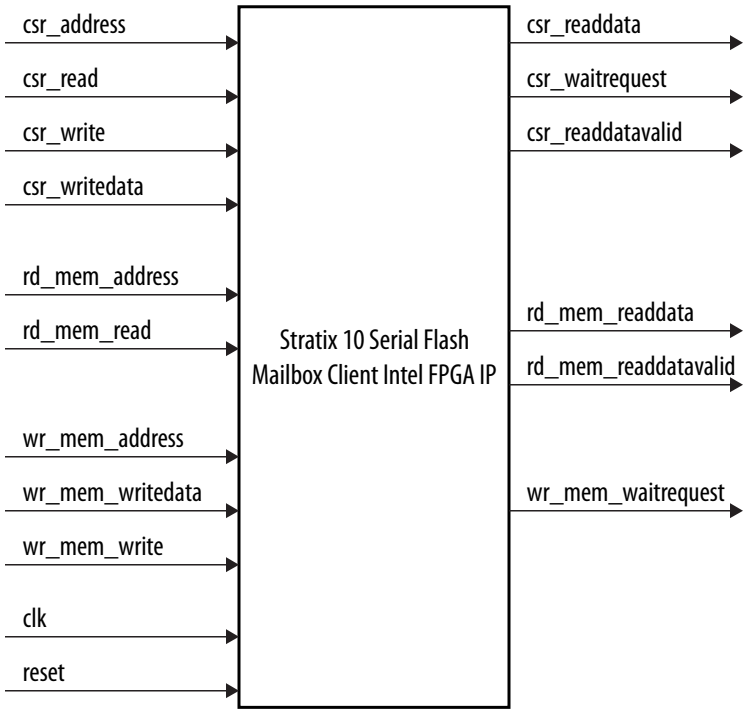


Table 1. Signal Description

Signal	Width	Direction	Description
Avalon®-MM Control Status Register Signals			
csr_address	7	Input	Avalon-MM address bus. The address bus is in word addressing.
csr_read	1	Input	Avalon-MM read control to the CSR.
csr_readdata	32	Output	Avalon-MM read data bus from the CSR.
csr_write	1	Input	Avalon-MM write control to the CSR.
csr_writedata	32	Input	Avalon-MM write data bus to CSR.
csr_waitrequest	1	Output	Avalon-MM waitrequest control from the CSR
csr_readdata_valid	1	Output	Avalon-MM read data valid that indicates the CSR read data is available.
Avalon-MM Write Data Signals			
wr_mem_write	1	Input	Avalon-MM write control to the memory
wr_mem_address	1	Input	Avalon-MM address.
wr_mem_writedata	32	Input	Avalon-MM write data bus to the memory
wr_mem_waitrequest	1	Output	Avalon-MM waitrequest control from the memory.
Avalon-MM Read Data Signals			

continued...

Signal	Width	Direction	Description
rd_mem_read	1	Input	Avalon-MM read control to the memory
rd_mem_readdata	32	Output	Avalon-MM read data bus from the memory.
rd_mem_readdata_valid	1	Output	Avalon-MM read data valid that indicates the memory read data is available.
rd_mem_address	1	Input	Avalon-MM address.
Clock and Reset			
clk	1	Input	Input clock to clock the IP core. The maximum frequency supported for this clock is 250 MHz.
reset	1	Input	Synchronous reset to reset the IP core.

Related Information

Using Stratix 10 Serial Flash Mailbox Client Intel FPGA IP on page 7

Register Map

Table 2. Register Map and Definitions

- Each address offset in the table represents one word of memory address space.
- All registers have a default value of 0x0 unless otherwise stated.

Offset	Name	Field Name	R/W	Width	Bit	Description
0	STATUS	Rsp_status	R	11	10:0	The status of executed commands.
1	ISR	Rddata valid	R	1	1	Interrupt status register. Value 1 indicates that readdata is in FIFO. You can read the fill level to check how many data are available and start reading out the data.
		Cmd_err1	R	1	0	Value 1 indicate that the command is not completed successfully. See STATUS.
2	IER(1)	Rdat_valid_en	R/W	1	1	Interrupt status register. Write 1 to enable read data valid.
		Cmd_err_en	R/W	1	0	Write 1 to enable command error response.
3	CHIP_SELECT	Chip_select	R/W	4	3:0	Write the value of the EPCQ-L device you want to select.
4	OPEN	Open	W	1	0	Request exclusive access to the EPCQ-L device. Write 1 to request exclusive access. The IP returns OK if SDM accepts request.
5	CLOSE	Close	W	1	0	Close exclusive access to the EPCQ-L device. Write 1 to close exclusive access. The IP returns OK if SDM accepts request.
6	WR_ENABLE	Wr_enable	W	1	0	Write 1 to perform write enable operation to the device.
7	WR_STATUS	Wr_status	W	8	7:0	Write a value to the status register of the device.

continued...

(1) Default value is 0x1.

Offset	Name	Field Name	R/W	Width	Bit	Description
8	RD_STATUS	Rd_status	R	8	7:0	Read the status register of the device. This field contains the information from read status register operation.(2)
9	SECTOR_ERASE	Sector_address	W	32	0:31	Erases one sector in the flash. The address of sector to be erase.
10	RD_DEVICE_ID	Device_id	R	32	0:31	Read this address to obtain the device ID.
11 - 12	Reserved					
13	CONTROL	Opcode	R/W	8	31:24	Opcode of the EPCQ-L device operation
		Reserved				
		Read_data_en	R/W	1	5	Value 1 indicates the command has read data.
		Write_data_en	R/W	1	4	Value 1 indicates the command has write data.
		Address_en	R/W	1	3	Value 1 indicates the command has address.
		Reserved				
		Execute	W	1	0	Write 1 to execute the command.
14	NUMB_BYTES	Number_bytes	R/W	4	3:0	The number of bytes to write or read to device register (maximum 8 bytes).
15	WRITEDATA_0	Writedata_0	W	32	31:0	The lower 4 bytes of write data.
16	WRITEDATA_1	Writedata_1	W	32	31:0	The upper 4 bytes of write data.
17	READDATA_0	Readdata_0	R	32	31:0	The lower 4 bytes of read data.
18	READDATA_1	Readdata_1	R	32	31:0	The upper 4 bytes of read data.
19	Reserved					
20	WRITE_OP	Write_op	W	2	1:0	Write 2'b01 to perform write operation with address provided in offset 21 and write data in FIFO. Write 2'b10 to flush out data inside write FIFO .
21	WRITE_ADDR	Write_addr	W	32	31:0	The device address for write operation.
22	WRITE_FIFO_LEVEL	Wr_fifo_level	R	32	31:0	Returns the fill level of the internal write data FIFO.
23	READ_OP	Read_op	W	2	1:0	Write 2'b01 to perform read operation with address provided in offset 24 Write 2'b10 to flush out data inside read FIFO.
24	READ_ADDR	Read_addr	R/W	32	31:0	The device address for read operation.
25	READ_WORDS	Read_words	R/W	32	31:0	Number of words to read from device (maximum is 4K bytes)
26	READ_FIFO_LEVEL	Read_fifo_level	R	32	31:0	Contains the fill level of the internal read data FIFO.

(2) To check the status of stacked devices, refer to the flag status register. You can access the flag status register using the CONTROL command.

Related Information

- Using Stratix 10 Serial Flash Mailbox Client Intel FPGA IP on page 7
- Response Codes on page 7

Response Codes

The Stratix 10 Serial Flash Mailbox Client Intel FPGA IP core returns response code for each command you execute together with read data, if applicable.

Table 3. Stratix 10 Serial Flash Mailbox Client Intel FPGA IP Response Codes

You must check the response to ensure that the Stratix 10 Serial Flash Mailbox Client Intel FPGA IP core receives the command.

Value	Name	Description
0	OK	Indicates that the command completed successfully.
1	INVALID_COMMAND	Indicates that the command is in an incorrect format.
2	UNKNOW_BR	Indicates that the command code is not understood. The device is running in the boot rom, load firmware for advanced command support.
3	UNKNOW	Indicates that the command code is not understood by the currently loaded firmware.
256	NOT_CONFIGURED	Indicates that the device is not configured.

Related Information

- Using Stratix 10 Serial Flash Mailbox Client Intel FPGA IP on page 7
- Summary of Operation Codes in EPCQ-A Serial Configuration Device Datasheet
- Register Map on page 5

Using Stratix 10 Serial Flash Mailbox Client Intel FPGA IP

The following guidelines list the flow of operations you must execute for CSR, write, and read operations using the Stratix 10 Serial Flash Mailbox Client Intel FPGA IP core.All interfaces are Avalon-MM compliant. Refer to the *Avalon Interface Specification* for more information.

Related Information

- Signals on page 4
- Register Map on page 5
- Response Codes on page 7

Control Status Register Operation

The following steps are guidelines to perform a read or write to a specific address offset using the Stratix 10 Serial Flash Mailbox Client Intel FPGA IP CSR.

1. Assert the `csr_write` or `csr_read` signals while the `csr_waitrequest` signal is low. If the `csr_waitrequest` signal is high, the `csr_write` or `csr_read` signals must be kept high until the `csr_waitrequest` signal goes low.
2. Depending on the operation, perform the following steps:

- For read operations, set the address value on the `csr_address` bus.
- For write operations, set the address value on the `csr_address` bus and the value data on the `csr_writedata` bus.

3. For read operations, you can retrieve the data after the `csr_readdatavalid` signal is high.

Write Operation

The following steps are guidelines to perform a write operation using Stratix 10 Serial Flash Mailbox Client Intel FPGA IP IP core.The maximum size of data for each read operation is limited to 4K byte.

1. *Note:* This step is required only if the flash device is filled.

   Erase the flash device using the SECTOR_ERASE command.
2. Flush out all the write data FIFO by writing `2b'10` to the `WRITE_OP` command.
3. Pre-store the data you want to write to the flash device in the write data FIFO via write data interfaces. Write the write data FIFO:

   Note: The interface backpressures when the write data FIFO is full.

   a. Assert the `wr_mem_write` signal while the `wr_mem_waitrequest` signal is low. If the `wr_mem_waitrequest` signal is high, the `wr_mem_write` signal must be kept high until the `wr_mem_waitrequest` signal goes low.)

   b. Write the address value at the `wr_mem_address` bus and write the data value to `wr_mem_writedata` bus.

      Note: Refer to the base address assigned to `wr_mem` bus for Stratix 10 Serial Flash Mailbox Client Intel FPGA IP in the Intel Quartus® Prime Platform Designer for list of address values that you can write into.

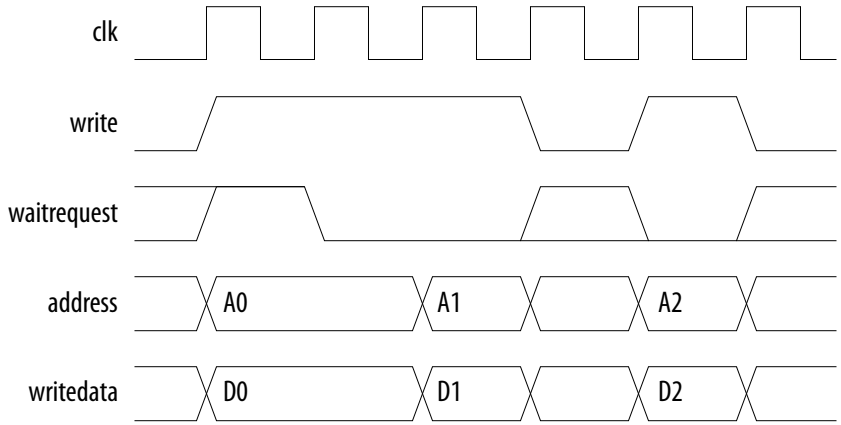
   c. Repeat step *a* to *b* to continuously pre-store the data into the write data FIFO.

   d. De-assert the `wr_mem_write` signal once you have completed writing the data into the write data FIFO.

   e. Optional: You can read the fill level of the internal write data FIFO using the `WRITE_FIFO_LEVEL` command to know if the write data FIFO is filled up.
4. Specify the start address of the location you want to write the data into the flash by using the `WRITE_ADDR` command.
5. Start the write operation by transferring the data from the write data FIFO into the flash device by writing `2'b01` to the `WRITE_OP` command.
6. Poll the `ISR` status to check the status of the write transaction. The `ISR` is triggered if the transaction is not successful.
7. Repeat step *1* to *6* to continue to perform the subsequent write operation.

   Note: You can poll the `CMD_STATUS` register each time you send a command ensure that the command is successfully executed.

Figure 2. Write Operation Example Timing Diagram



Note: You can use the Stratix 10 Serial Flash Mailbox Client Intel FPGA IP IP to write the raw programming data (`.rpd`) file into the EPCQ-L device. Refer to the *Generating Programming Files using Convert Programming Files* in the *Intel Stratix 10 Configuration User Guide* for more information about programming the EPCQ-L device.

Related Information

- Summary of Operation Codes in EPCQ-A Serial Configuration Device Datasheet
- Generating Programming Files using Convert Programming Files of the Intel Stratix 10 Configuration User Guide

Read Operation

The following steps are guidelines to perform a read operation using Stratix 10 Serial Flash Mailbox Client Intel FPGA IP IP core.The maximum size of data for each read operation is limited to 4K byte.

1. Specify the flash device address to read the data by using the READ_ADDR command
2. Specify the number of words to read by using the READ_WORDS command. The maximum number of words can be read per transaction is 1024 (`32'h00000400`).
3. Flush out all the read data FIFO before you perform any read operations by writing `2b'10` to the READ_OP command.
4. Start the read operation by transferring data from flash to read data FIFO by writing `2'b01` to the READ_OP command.
5. Poll the `ISR` register to check if the data stored in read data FIFO is ready to read. You can also read the fill level of the internal read data FIFO using the `READ_FIFO_LEVEL` command to know if there is any data stored inside the read data FIFO.
6. Read the data stored in read data FIFO via read data interfaces. Refer to the following steps to read the read data FIFO:
   a. Assert the `rd_mem_read` signal while the `rd_mem_waitrequest` signal is low. If the `rd_mem_waitrequest` signal is high, the `rd_mem_read` signal must be kept high until the `wr_mem_waitrequest` signal goes low.

b. Set the address value at the `rd_mem_address` bus.

Note: Refer to the base address assigned to `rd_mem` bus for Stratix 10 Serial Flash Mailbox Client Intel FPGA IP in the Intel Quartus Prime Platform Designer for list of address values that you can read into.

c. Read the `rd_mem_readdata` bus if `rd_mem_readdatavalid` signal is asserted high.

d. Repeat step *a* to *c* to continuously read the data from the read data FIFO.

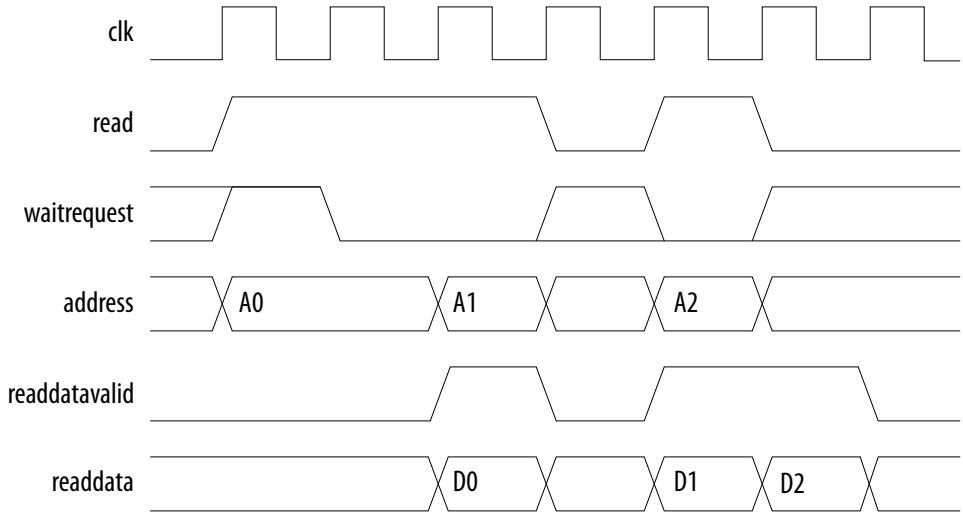
e. De-assert the `rd_mem_read` signal once you have completed reading the data from the read data FIFO.

f. Optional: You can read the fill level of the internal read data FIFO using the READ_FIFO_LEVEL command.

7. Repeat step *1* to *6* to continue to perform subsequent read operations.

Note: You can poll the CMD_STATUS register each time you send a command to ensure that the command is successfully executed.

Figure 3. Read Operation Example Timing Diagram



Related Information

Summary of Operation Codes in EPCQ-A Serial Configuration Device Datasheet

Revision History for Stratix 10 Serial Flash Mailbox Client Intel FPGA IP Core User Guide

Document Version	Intel Quartus Prime Version	Changes
2018.05.07	18.0	Initial release.