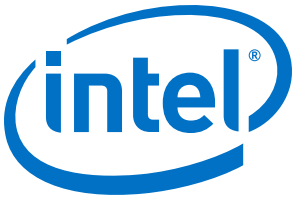

JESD204C Intel® Agilex™ FPGA IP Design Example User Guide

Updated for Intel® Quartus® Prime Design Suite: **19.3**

IP Version: **1.0.0**

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Contents

1. About the JESD204C Intel® Agilex™ FPGA IP Design Example User Guide

This user guide provides the features, usage guidelines, and detailed description about the design examples for the JESD204C Intel® FPGA IP using Intel Agilex™ devices.

Intended Audience

This document is intended for:

- Design architect to make IP selection during system level design planning phase
- Hardware designers when integrating the IP into their system level design
- Validation engineers during system level simulation and hardware validation phase

Related Documents

The following table lists other reference documents which are related to the JESD204C Intel FPGA IP.

Table 1. Related Documents

Reference	Description
JESD204C Intel FPGA IP User Guide	Provides information about the JESD204C Intel FPGA IP.
Intel Agilex Device Data Sheet	This document describes the electrical characteristics, switching characteristics, configuration specifications, and timing for Intel Agilex devices.

Acronyms and Glossary

Table 2. Acronym List

Acronym	Expansion
LEMC	Local Extended Multiblock Clock
FC	Frame clock rate
ADC	Analog to Digital Converter
DAC	Digital to Analog Converter
DSP	Digital Signal Processor
TX	Transmitter
RX	Receiver
DLL	Data link layer
CSR	Control and status register
CRU	Clock and Reset Unit

continued...

Acronym	Expansion
ISR	Interrupt Service Routine
FIFO	First-In-First-Out
SERDES	Serializer Deserializer
ECC	Error Correcting Code
FEC	Forward Error Correction
SERR	Single Error Detection (in ECC, correctable)
DERR	Double Error Detection (in ECC, fatal)
PRBS	Pseudorandom binary sequence
MAC	Media Access Controller. MAC includes protocol sublayer, transport layer, and data link layer.
PHY	Physical Layer. PHY typically includes the physical layer, SERDES, drivers, receivers and CDR.
PCS	Physical Coding Sub-layer
PMA	Physical Medium Attachment
RBD	RX Buffer Delay
UI	Unit Interval = duration of serial bit
RBD count	RX Buffer Delay latest lane arrival
RBD offset	RX Buffer Delay release opportunity
SH	Sync header
TL	Transport layer

Table 3. Glossary List

Term	Description
Converter Device	ADC or DAC converter
Logic Device	FPGA or ASIC
Octet	A group of 8 bits, serving as input to 64/66 encoder and output from the decoder
Nibble	A set of 4 bits which is the base working unit of JESD204C specifications
Block	A 66-bit symbol generated by the 64/66 encoding scheme
Line Rate	Effective data rate of serial link Lane Line Rate = (Mx Sx N'x 66/64 x FC) / L
Link Clock	The associated parallel data will be 128 bit/132 bit instead of 64 bit/66 bit. Link Clock = Lane Line Rate/132.
Frame	A set of consecutive octets in which the position of each octet can be identified by reference to a frame alignment signal.
Frame Clock	A system clock which runs at the frame's rate, that must be 1x, 2x, or 4x link clock.
Samples per frame clock	Samples per clock, the total samples in frame clock for the converter device.
LEMC	Internal clock used to align the boundary of the extended multiblocks between lanes and into the external references (SYSREF or Subclass 1).

continued...

Term	Description
Subclass 0	No support for deterministic latency. Data should be immediately released upon lane to lane deskew on receiver.
Subclass 1	Deterministic latency using SYSREF.
Multipoint Link	Inter-device links with 2 or more converter devices.
64B/66B Encoding	Line code that maps 64-bit data to 66 bits to form a block. The base level data structure is a block that starts with 2-bit sync header.

Table 4. Symbols

Term	Description
L	Number of lanes per converter device
M	Number of converters per device
F	Number of octets per frame on a single lane
S	Number of samples transmitted per single converter per frame cycle
N	Converter resolution
N’	Total number of bits per sample in the user data format
CS	Number of control bits per conversion sample
CF	Number of control words per frame clock period per link
HD	High Density user data format
E	Number of multiblocks in an extended multiblock

2. JESD204C Intel FPGA IP Design Example Quick Start Guide

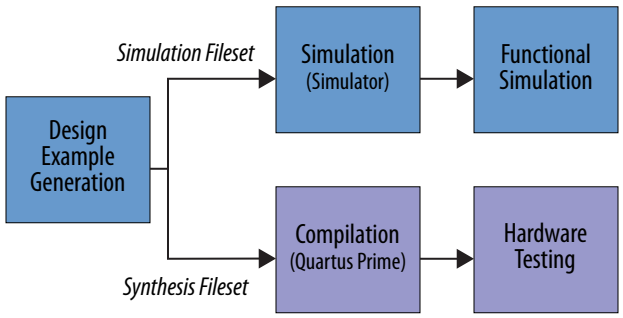
The JESD204C Intel FPGA IP design examples for Intel Agilex devices features a simulating testbench and a hardware design that supports compilation.

The JESD204C Intel FPGA IP provides two preset settings for Intel Agilex devices in duplex mode.

- JESD204C design example for L=2, M=8, F=12, with data rate of 24.333 Gbps
- JESD204C design example for L=4, M=8, F=4, with data rate of 16.222 Gbps

You can generate the JESD204C design examples through the IP catalog in the Intel Quartus® Prime Pro Edition software.

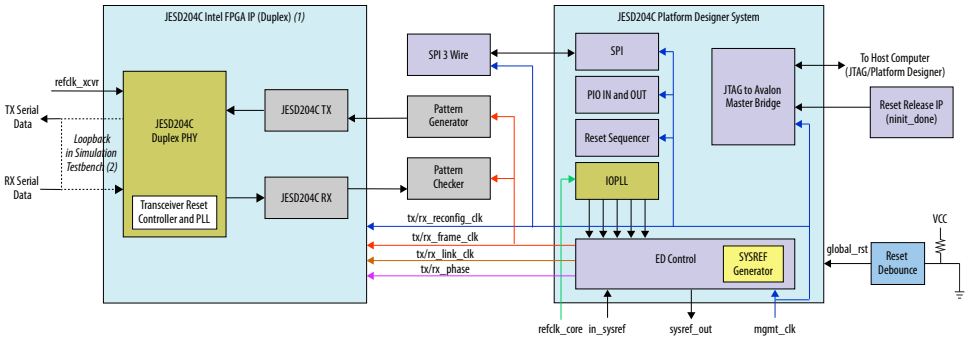
Figure 1. Development Stages for the Design Example



Note: Hardware testing will only be available for Intel Agilex design examples in a future release of the Intel Quartus Prime Pro Edition software.

2.1. Design Example Block Diagram

Figure 2. JESD204C Design Example High-level Block Diagram



The design example consists of the following modules:

- Platform Designer system
  - JESD204C Intel FPGA IP
  - JTAG to Avalon master bridge
  - Parallel I/O (PIO) controller
  - Serial Port Interface (SPI)—master module
  - Core PLL
  - SYSREF generator
- Pattern generator
- Pattern checker
- IOPLL

Table 5. Design Example Modules

Components	Description
Platform Designer system	The Platform Designer system instantiates the JESD204C IP data path and supporting peripherals.
JESD204C Intel FPGA IP	This Platform Designer subsystem contains the TX and RX JESD204C IPs instantiated together with the duplex PHY.
JTAG to Avalon Master bridge	This bridge provides system console host access to the memory-mapped IP in the design through the JTAG interface.
Parallel I/O (PIO) controller	This controller provides a memory-mapped interface for sampling and driving general purpose I/O ports.
SPI master	This module handles the serial transfer of configuration data to the SPI interface on the converter end.
SYSREF generator	The SYSREF generator uses the link clock as a reference clock and generates SYSREF pulses for the JESD204C IP. *Note:* This design example uses the SYSREF generator to demonstrate the duplex JESD204C IP link initialization. In the JESD204C subclass 1 system level application, you must generate the SYSREF from the same source as the device clock.

continued...

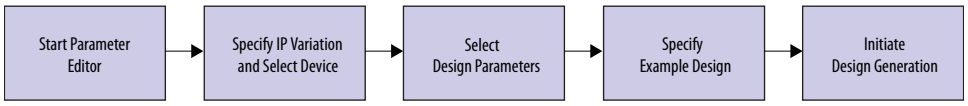
Components	Description
Pattern generator	The pattern generator generates a PRBS or ramp pattern.
Pattern checker	The pattern checker verifies the PRBS or ramp pattern received, and flags an error when it finds a mismatch of data sample.
IOPLL	This design example uses an IOPLL to generate a user clock for transmitting data into the JESD204C IP.

2.2. Hardware and Software Requirements

Intel uses the following hardware and software to test the design examples in a Linux system:

- Intel Quartus Prime Pro Edition software version 19.3
- ModelSim*, Xcelium*, NCSim (Verilog only), or VCS*/VCS MX simulator

2.3. Generating the Design



To generate the design example from the IP parameter editor:

1. Create a project targeting Intel Agilex device family and select the desired device.
2. In the IP Catalog, **Tools ➤ IP Catalog**, select **JESD204C Intel FPGA IP**.
3. Specify a top-level name and the folder for your custom IP variation. Click **OK**.
4. Select a design from the **Presets** library and click **Apply**. When you select a design, the system automatically populates the IP parameters for the design.

   Note: If you select another design, the settings of the IP parameters change accordingly. Alternatively, you can also specify your own settings and generate the design.
5. Under the **Example Design** tab, specify the design example parameters as described in *Design Example Parameters*.
6. Click **Generate Example Design**.

The software generates all design files in the sub-directories. These files are required to run simulation and compilation.

2.3.1. Design Example Parameters

The JESD204C Intel FPGA IP parameter editor includes a **Example Design** tab for you to specify certain parameters before generating the design example.

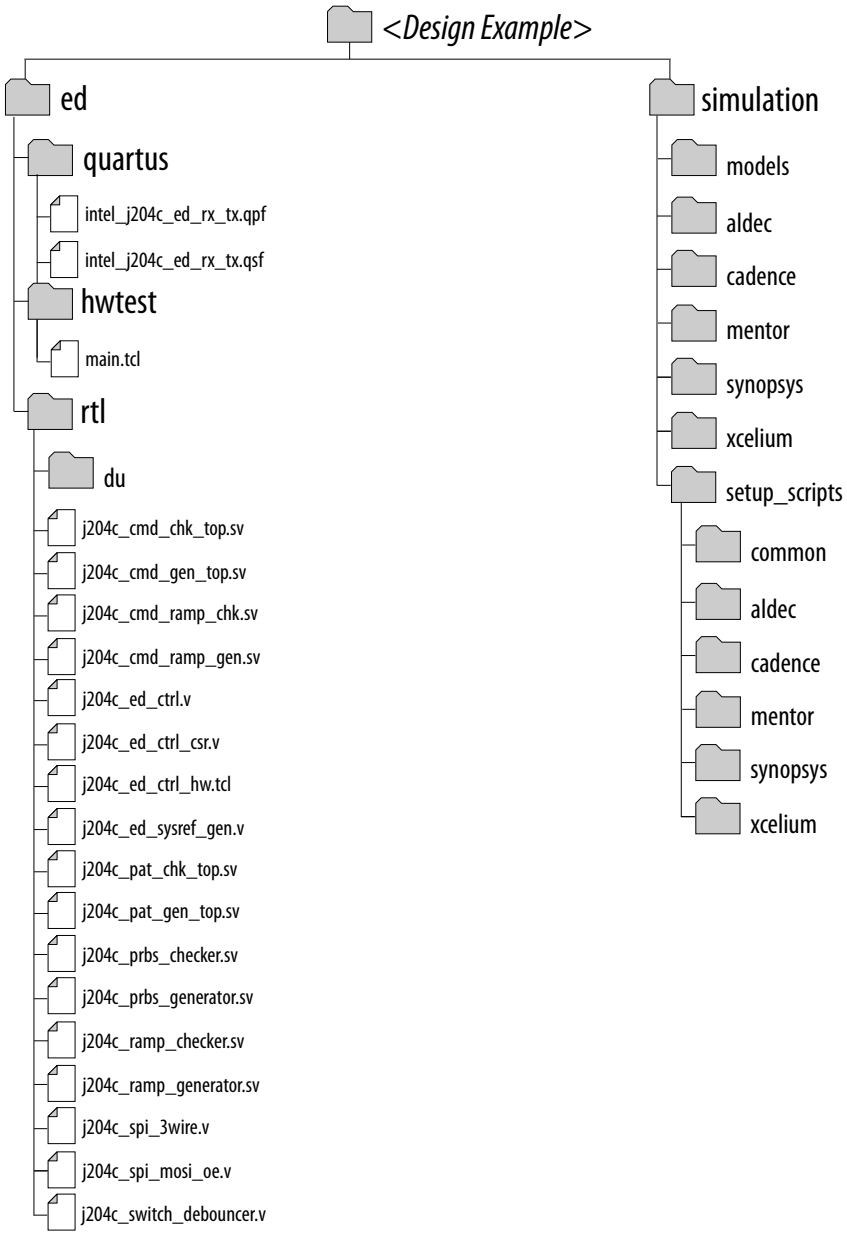
Table 6. Parameters in the Example Design Tab

Parameter	Options	Description
Select Design	• System Console Control • None	Select the system console control to access the design example data path through the system console.
Simulation	On, Off	Turn on for the IP to generate the necessary files for simulating the design example.
Synthesis	On, Off	Turn on for the IP to generate the necessary files for Intel Quartus Prime compilation.
HDL format (for simulation)	Verilog only	Select the HDL format of the RTL files for simulation.
HDL format (for synthesis)	Verilog only	Select the HDL format of the RTL files for synthesis.
Generate 3-wire SPI module	On, Off	Turn on to enable 3-wire SPI interface instead of 4-wire.
Sysref mode	• One-shot • Periodic • Gapped periodic	Select whether you want the SYSREF alignment to be a one-shot pulse mode, periodic, or gapped periodic, based on your design requirements and timing flexibility. • One-shot: Select this option to enable SYSREF to be a one-shot pulse mode. The `sysref_ctrl[17]` register bit's value is 0. After the JESD204C IP reset deasserts, change the `sysref_ctrl[17]` register's value from 0 to 1, then to 0, for a one-shot SYSREF pulse. • Periodic: SYSREF in periodic mode has 50:50 duty cycle. SYSREF period is E*SYSREF_MULP. • Gapped periodic: SYSREF has programmable duty cycle of granularity of 1 link clock cycle. SYSREF period is E*SYSREF_MULP. For out-of-range duty cycle setting, the SYSREF generation block should automatically infer 50:50 duty cycle. Refer to SYSREF Generator on page 16 for more information about the SYSREF period.
Select board	• None	Select the board for the design example. • None: This option excludes hardware aspects for the design example. All the pin assignments will be set to virtual pins.
Test pattern	• PRBS-7 • PRBS-9 • PRBS-15 • PRBS-23 • Ramp	Select the patten generator and checker test pattern to either ramp or one of the PRBS pattern options. The PRBS options are some of the commonly used degree of polynomials. If you select PRBS pattern, the pattern checker expects the scrambling seed to be self-synchronized when the deskew alignment is achieved by the JESD204C RX IP. If you select ramp pattern, the first valid data sample for each converter (M) is loaded as the initial value. Subsequent data sample values must increase by 1 in each clock cycle up to the maximum and then roll over to 0. For example, when S=1, N=16 and WIDTH_MULP = 2, the data width per converter is S*WIDTH_MULP*N=32. The maximum data sample value is 0xFFFF. The ramp pattern checker verifies that identical patterns are received across all converters.
Enable internal serial loopback (Simulation)	On, Off	Turn on to enable internal serial loopback. If you turn on this option, the RX path takes the serial input from the TX path internally in the FPGA.
Enable command channel pattern (Simulation)	On, Off	Turn on to enable command channel pattern.

2.3.2. Directory Structure

The JESD204C design example directories contain generated files for the design examples.

Figure 3. Directory Structure for JESD204C Intel Agilex Design Example



Note: Intel Agilex E-tile devices do not support Aldec Riviera-PRO* simulators.

Table 7. Directory Files

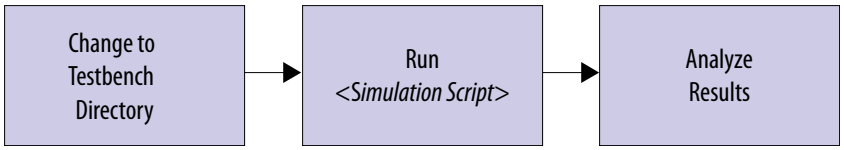
Folders	Files
ed/rtl	• du — intel_j204c_ed_rx_tx.sv (top-level HDL file) — intel_j204c_ed_rx_tx.sdc — J204c_rx_tx_ip.qsys — j204c_rx_tx_ss.qsys — altera_s10_user_rst_clkgate_0.ip — intel_j204c_se_outbuf_1bit.ip • rx — intel_j204c_ed_rx.sv (top-level HDL file) — intel_j204c_ed_rx.sdc — j204c_rx_ip.qsys — j204c_rx_ss.qsys — altera_s10_user_rst_clkgate_0.ip — intel_j204c_se_outbuf_1bit.ip • tx — intel_j204c_ed_tx.sv (top-level HDL file) — intel_j204c_ed_tx.sdc — j204c_tx_ip.qsys — j204c_tx_ss.qsys — altera_s10_user_rst_clkgate_0.ip — intel_j204c_se_outbuf_1bit.ip
simulation/models	• tb_top.sv
simulation/cadence	• cadence_sim.sh • tb_top_wave.tcl
simulation/mentor	• modelsim_sim.tcl • tb_top_waveform.do
simulation/synopsys	• vcs — vcs_sim.sh — tb_top_wave_ed.do • vcsmx — vcsmx_sim.sh — tb_top_wave_ed.do
simulation/xcelium	• xcelium_sim.sh • tb_top_wave.tcl
simulation/setup_scripts/common	• modelsim_files.tcl • ncsim_files.tcl • vcs_files.tcl • vcsmx_files.tcl • xcelium_files.tcl
simulation/setup_scripts/cadence	• cds.lib • hdl.var • ncsim_setup.sh • *<cds_libs folder>*

continued...

Folders	Files
simulation/setup_scripts/mentor	• msim_setup.tcl
simulation/setup_scripts/synopsys	• vcs — vcs_setup.sh • vcsmx — vcsmx_setup.sh — synopsys_sim.setup
simulation/setup_scripts/xcelium	• xcelium_setup.sh • cds.lib • hdl.var • *<cds_libs folder>*

2.4. Compiling and Simulating the Design

The design example testbench simulates your generated design.



To simulate the design, perform the following steps:

1. Change the working directory to `<example_design_directory>/simulation/<Simulator>`.
2. In the command line, run the simulation script. The table below shows the commands to run the supported simulators.

Simulator	Command
NCSim	`sh cadence_sim.sh`
ModelSim	`vsim -do modelsim_sim.tcl`
	`vsim -c -do modelsim_sim.tcl` (without ModelSim GUI)
VCS	`sh vcs_sim.sh`
VCS MX	`sh vcsmx_sim.sh`
Xcelium Parallel	`sh xcelium_sim.sh`

The simulation ends with messages that indicate whether the run was successful or not.

Figure 4. Successful Simulation

The average simulation run time including design elaboration is approximately 8 minutes on VCS, and 26 minutes on ModelSim - Intel FPGA Starter Edition for preset with L=2, M=8, and F=12.

```
# INFO: (time=12880000) Finished loading serdes
'tb_top.u_intel_j204c_ed_rx_tx.u_j204c_rx_tx_ss.j204c_rx_tx_ip.intel_jesd204c.intel_jesd204c.j204c_
phy_hip_inst.inst_xcvr.g_xcvr_native_insts[0].ct3_xcvr_native_inst.inst_ct3_xcvr_channel.inst_ct3_h
ssi_xcvr.<protected>.<protected>.<protected>.<protected>.<protected>.<protected>.<protected>'
imem from file 'serdes.firmware.rom'
# INFO: tx_ready asserted
# INFO: rx_ready asserted
# Running JESD204C Simulation: L=2, M=8, F=12, DATARATE/L=24333.000000Mbps FCLK_MULP=2
WIDTH_MULP=2
# Pattern Checker(s): OK!
# Command Channel Pattern Checker(s): OK!
# JESD204C Rx Core(s): SH Locked!
# JESD204C Rx Core(s): EMB Locked!
# JESD204C Tx Core(s): OK!
# JESD204C Rx Core(s): OK!
# TESTBENCH_PASSED: SIM PASSED!
# Break in Module tb_top at ../models/tb_top.sv line 399
# Stopped at ../models/tb_top.sv line 399
```

3. Detailed Description for the JESD204C Design Example

The JESD204C design example demonstrates the functionality of data streaming using loopback mode.

You can specify the parameters settings of your choice and generate the design example.

The design example is available only in duplex mode for both Base and PHY variant. You can choose Base only or PHY only variant but the IP would generate the design example for both Base and PHY.

Note: Some high data rate configurations may fail timing. To avoid timing failure, consider specifying lower frame clock frequency multiplier (**FCLK_MULP**) value in the **Configurations** tab of the JESD204C Intel FPGA IP parameter editor.

3.1. System Components

The JESD204C design example provides a software-based control flow that uses the hard control unit with or without system console support.

The design example enables an auto link up in internal and external loopback modes.

You can either configure your own settings or use one of the two presets provided.

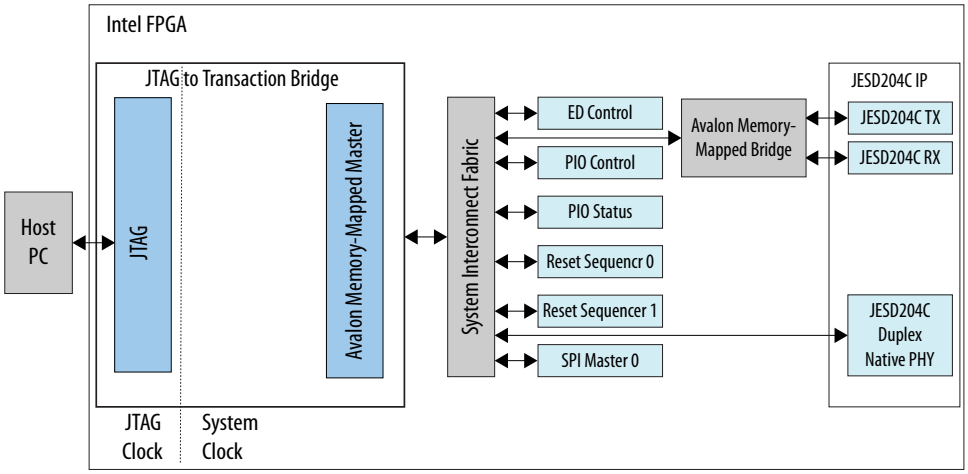
- L=2, M=8, F=12, with data rate of 24.333 Gbps
- L=4, M=8, F=4, with data rate of 16.222 Gbps

3.1.1. JTAG to Avalon® Master Bridge

The JTAG to Avalon® Master Bridge provides a connection between the host system to access the memory-mapped JESD204C IP and the peripheral IP control and status registers through the JTAG interface.

Figure 5. System with a JTAG to Avalon Master Bridge Core

Note: System clock must be at least 2X faster than the JTAG clock. The system clock is `mgmt_clk` (100MHz) in this design example.

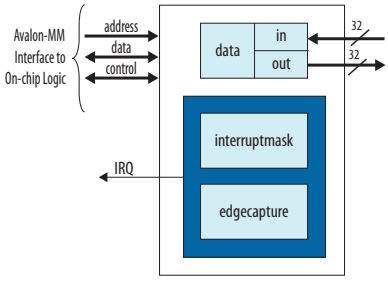


3.1.2. Parallel I/O (PIO) Core

The parallel input/output (PIO) core with Avalon interface provides a memory-mapped interface between an Avalon Memory-Mapped slave port and general purpose I/O ports. The I/O ports connect either to on-chip user logic, or to I/O pins that connect to devices external to the FPGA.

Figure 6. PIO Core with Input Ports, Output Ports, and IRQ Support

By default, the Platform Designer component disables the Interrupt Service Line (IRQ).



The PIO I/O ports are assigned at the top level HDL file (`io_status` for input ports, `io_control` for output ports).

The table below describes the signal connectivity for the status and control I/O ports to the DIP switch and LED on the development kit.

Table 8. PIO Core I/O Ports

Port	Bit	Signal
Out_port	0	USER_LED SPI programming done
	31:1	Reserved
In_port	0	USER_DIP internal serial loopback enable Off = 1 On = 0
	1	USER_DIP FPGA-generated SYSREF enable Off = 1 On = 0
	31:2	Reserved.

3.1.3. SPI Master

The SPI master module is a standard Platform Designer component in the **IP Catalog** standard library. This module uses the SPI protocol to facilitate the configuration of external converters (for example, ADC, DAC, and external clock generators) via a structured register space inside these devices. The SPI master has an Avalon memory-mapped interface that connects to the Avalon master (JTAG to Avalon master bridge) via the Avalon-MM interconnect. The SPI master receives configuration instructions from the Avalon master.

The SPI master module controls up to 32 independent SPI slaves. The SCLK baud rate is configured to 20 MHz (divisible by 5).

This module is configured to a 4-wire, 24-bit width interface. If the **Generate 3-Wire SPI Module** option is selected, an additional module is instantiated to convert the 4-wire output of the SPI master to 3-wire.

3.1.4. SYSREF Generator

SYSREF is a critical timing signal for data converters with JESD204C interface.

The SYSREF generator in the design example is used for the duplex JESD204C IP link initialization demonstration purpose only. In the JESD204C subclass 1 system level application,you must generate SYSREF from the same source as the device clock.

For the JESD204C IP, the SYSREF multiplier (SYSREF_MULP) of the SYSREF control register defines the SYSREF period, which is n-integer multiple of the E parameter.

You must ensure E*SYSREF_MULP ≤16. For example, if E=1, the legal setting for SYSREF_MULP must be within 1–16, and if E=3, the legal setting for SYSREF_MULP must be within 1–5.

Note: If you set an out-of-range SYSREF_MULP, the SYSREF generator will fix the setting to SYSREF_MULP=1.

You can select whether you want the SYSREF type to be a one-shot pulse, periodic, or gapped periodic through the **Example Design** tab in the JESD204C Intel FPGA IP parameter editor.

Table 9. Examples of Periodic and Gapped Periodic SYSREF Counter

E	SYSREF_MULP	SYSREF PERIOD (E*SYSREF_MULP*16)	Programmable Duty Cycle	Description
1	1	16	1..15	Gapped Periodic
1	1	16	Auto (8)	Periodic
1	2	32	1..31	Gapped Periodic
1	2	32	16	Periodic
1	3	48	1..47	Gapped Periodic
1	3	48	Auto (24)	Periodic
1	16	256	1..255	Gapped Periodic
1	16	256	Auto (128)	Periodic
2	1	32	1..31	Gapped Periodic
2	1	32	16	Periodic
2	2	64	1..31	Gapped Periodic
2	2	64	Auto (32)	Periodic
2	3	96	1..95	Gapped Periodic
2	3	96	Auto (48)	Periodic
2	8	256	1..255	Gapped Periodic E*SYSREF_MULP <=16
2	8 (Illegal<9..16>)	256	Auto (128)	Periodic *Note:* If you assign an illegal SYSREF_MULP value, the the SYSREF period defaults to 32.
16	1 Illegal<2..16>	256	1..255	Gapped Periodic E*SYSREF_MULP <=16

Table 10. SYSREF Control Registers

You can dynamically reconfigure the SYSREF control registers if the register setting is different than the setting you specified when you generated the design example. Configure the SYSREF registers before the JESD204C Intel FPGA IP is out of reset. If you select the external SYSREF generator through the `sysref_ctrl[7]` register bit, you can ignore the settings for SYSREF type, multiplier, duty cycle and phase.

Bits	Default Value	Description
`sysref_ctrl[1:0]`	• 2'b00: One-shot • 2'b01: Periodic • 2'b10: Gapped periodic	SYSREF type. The default value depends on the SYSREF mode setting in the **Example Design** tab in the JESD204C Intel FPGA IP parameter editor.
`sysref_ctrl[6:2]`	5'b00000	SYSREF multiplier. This SYSREF_MULP field is applicable to periodic and gapped-periodic SYSREF type. You must configure the multiplier value to ensure the E*SYSREF_MULP value is between 1 to 16 before the JESD204C IP is out of reset. If the E*SYSREF_MULP value is out of this range, the multiplier value defaults to 5'b00001.

continued...

Bits	Default Value	Description
		For example: If E =1, write 5'b10000 to `sysref_ctrl[6:2]` to set the SYSREF_MULP decimal value of 16.
`sysref_ctrl[7]`	• Duplex datapath: 1'b1 • Simplex TX or RX datapath: 1'b0	SYSREF select. The default value depends on the SYSREF mode setting in the **Example Design** tab in the JESD204C Intel FPGA IP parameter editor. • 0: External SYSREF • 1: Internal SYSREF
`sysref_ctrl[15:8]`	8'h00	SYSREF duty cycle when SYSREF type is periodic or gapped periodic. You must configure the duty cycle before the JESD204C IP is out of reset. Maximum value = (E*SYSREF_MULP*16)-1 For example: 50% duty cycle = (E*SYSREF_MULP*16)/2 If you do not configure this register field, the duty cycle defaults to 50%.
`sysref_ctrl[16]`	1'b0	SYSREF phase (for `sysref_out` output port). • 0: Positive edge • 1: Negative edge
`sysref_ctrl[17]`	1'b0	Manual control when SYSREF type is one-shot. • Write 1 to set the SYSREF signal to high. • Write 0 to set the SYSREF signal to low. You need to write a 1 then a 0 to create a SYSREF pulse in one-shot mode.
`sysref_ctrl[31:18]`	*Don't Care*	Reserved.

3.1.5. Pattern Generator and Checker

The pattern generator and checker are useful for creating data samples and monitoring for testing purposes.

Table 11. Supported Pattern Generator

Pattern Generator	Description
PRBS pattern generator	The JESD204C design example PRBS pattern generator supports the following degree of polynomials: • PRBS23: $X^{23}+X^{18}+1$ • PRBS15: $X^{15}+X^{14}+1$ • PRBS9: $X^{9}+X^{5}+1$ • PRBS7: $X^{7}+X^{6}+1$
Ramp pattern generator	The ramp pattern value increments by 1 for every subsequent sample with the generator width of N, and rolls over to 0 when all bits in the sample are 1. Enable the ramp pattern generator by writing a 1 to bit 2 of the `tst_ctl` register of the ED control block.
Command channel ramp pattern generator	The JESD204C design example supports command channel ramp pattern generator per lane. The ramp pattern value increments by 1 per 6 bits of command words. The starting seed is an increment pattern across all lanes.

Table 12. Supported Pattern Checker

Pattern Checker	Description
PRBS pattern checker	The scrambling seed in the pattern checker is self-synchronized when the JESD204C IP achieves deskew alignment. The pattern checker requires 8 octets for the scrambling seed to self-synchonize.
Ramp pattern checker	The first valid data sample for each converter (M) is loaded as the initial value of the ramp pattern. Subsequent data samples values must increase by 1 in each clock cycle up to the maximum and then roll over to 0. For example, when S=1, N=16 and WIDTH_MULP = 2, the data width per converter is S * WIDTH_MULP * N = 32. The maximum data sample value is 0xFFFF. The ramp pattern checker verifies that identical patterns are received across all converters.
Command channel ramp pattern checker	The JESD204C deisgn example supports command channel ramp pattern checker. The first command word (6 bits) received is loaded as the initial value. Subsequent command words in the same lane must increment up to 0x3F and roll over to 0x00. The command channel ramp pattern checker checks for ramp patterns across all lanes.

3.2. Design Example Clock and Reset

The JESD204C design example has a set of clock and reset signals.

Table 13. Design Example Clocks

Clock Signal	Direction	Description
`mgmt_clk`	Input	LVDS differential clock with frequency of 100 MHz.
`refclk_xcvr`	Input	Transceiver reference clock with frequency of data rate/ factor of 33.
`refclk_core`	Input	Core reference clock with the same frequency as `refclk_xcvr`.
`in_sysref`	Input	SYSREF signal. Maximum SYSREF frequency is data rate/ (66x32xE).
`sysref_out`	Output	
`txlink_clk` `rxlink_clk`	Internal	TX and RX link clock with frequency of data rate/ 132.
`txframe_clk` `rxframe_clk`	Internal	• TX and RX frame clock with frequency of data rate/33 (FCLK_MULP=4) • TX and RX frame clock with frequency of data rate/66 (FCLK_MULP=2) • TX and RX frame clock with frequency of data rate/132 (FCLK_MULP=1)
`tx_fclk` `rx_fclk`	Internal	• TX and RX phase clock with frequency of data rate/132, duty cycle 25% (FCLK_MULP=4) • TX and RX phase clock with frequency of data rate/132 (FCLK_MULP=2) • TX and RX phase clock is always high (1'b1) when FCLK_MULP=1
`spi_SCLK`	Output	SPI baud rate clock with frequency of 20 MHz

When you load the design example into an FPGA device, an internal `ninit_done` event ensures that the JTAG to Avalon Master bridge is in reset as well as all the other blocks.

The SYSREF generator has its independent reset to inject intentional asynchronous relationship for the `txlink_clk` and `rxlink_clk` clocks. This method is more comprehensive in emulating the SYSREF signal from an external clock chip.

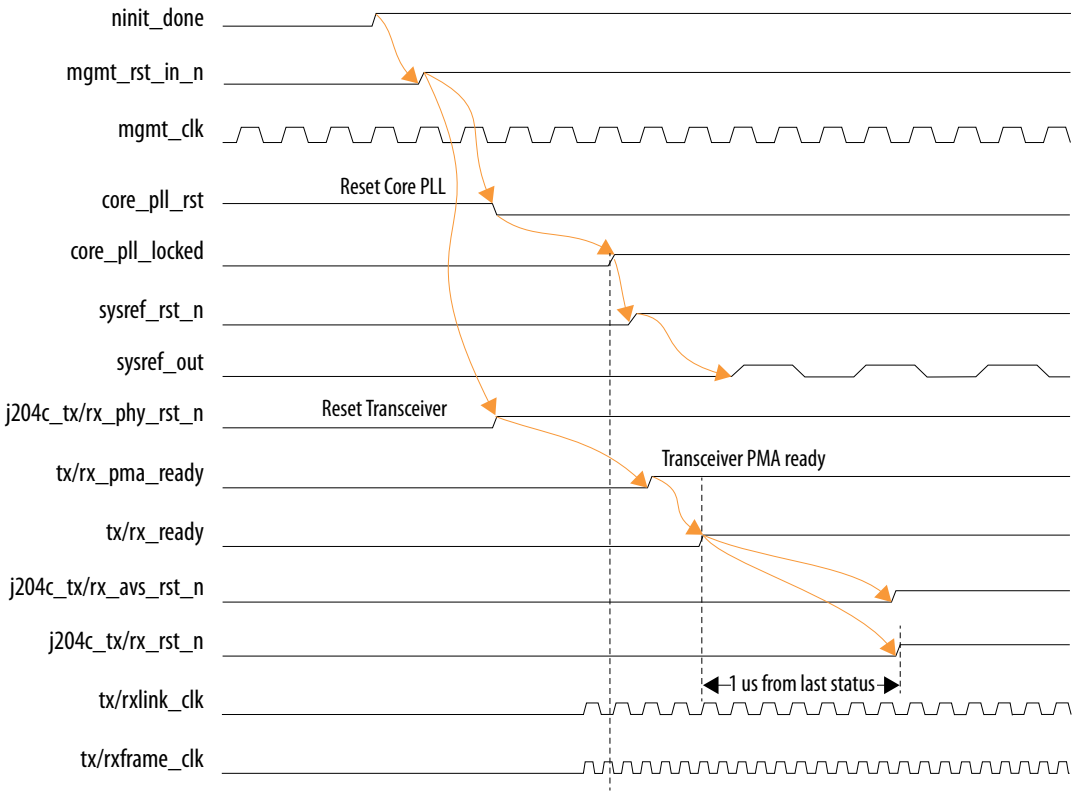
Table 14. Design Example Resets

Reset Signal	Direction	Description
`global_rst_n`	Input	Push button global reset for all blocks, except the JTAG to Avalon Master bridge.
`ninit_done`	Internal	Output from Reset Release IP for the JTAG to Avalon Master bridge.
`mgmt_rst_in_n`	Internal	Reset for Avalon memory-mapped interfaces of various IPs and inputs of reset sequencers: • `j20c_reconfig_reset for JESD204C IP duplex Native PHY` • `spi_rst_n` for SPI master • `pio_rst_n` for PIO status and control • `reset_in0` port of reset sequencer 0 and 1 The `global_rst_n`, `hw_rst`, or `edctl_rst_n` port asserts reset on `mgmt_rst_in_n`.
`j20c_tx_avs_rst_n` `j20c_tx_avs_rst_n`	Internal	Reset the JESD204C TX and RX IP Avalon memory-mapped interfaces through the reset sequencer 0 `reset_out0` port. These interfaces are reset when `mgmt_rst_in_n` reset is asserted.
`edctl_rst_n`	Internal	The ED Control block is reset by JTAG to Avalon Master bridge. The `hw_rst` and `global_rst_n` ports do not reset the ED Control block.
`sysref_rst_n`	Internal	Reset for SYSREF generator block in the ED Control block using the reset sequencer 0 `reset_out2` port. The reset sequencer 0 `reset_out2` port deasserts the reset if the core PLL is locked.
`j204c_tx_phy_rst_n` `j204c_rx_phy_rst_n`	Internal	Reset transceiver PHY in the JESD204C IP by asserting `mgmt_rst_in_n`. • The reset sequencer 0 `reset_out1` port resets `j204c_tx_phy_rst_n` • The reset sequencer 1 `reset_out0` port resets `j204c_rx_phy_rst_n`
`core_pll_rst`	Internal	Resets the core PLL through the reset sequencer 0 `reset_out0` port. The core PLL resets when `mgmt_rst_in_n` reset is asserted.
`j204c_tx_rst_n` `j204c_rx_rst_n`	Internal	Resets the JESD204C link and transport layers in `txlink_clk`, `rxlink_clk`, `txframe_clk`, and `rxframe_clk` domains.

continued...

Reset Signal	Direction	Description
		• The reset sequencer 0 `reset_out5` port resets `j204c_tx_rst_n`. This reset deasserts if the core PLL is locked, and the `tx_pma_ready` and `tx_ready` signals are asserted. • The reset sequencer 1 `reset_out4` port resets `j204c_rx_rst_n`. This reset deasserts if the core PLL is locked, and the `rx_pma_ready` and `rx_ready` signals are asserted.
`hw_rst`	Internal	Assert and deassert `hw_rst` by writing to the `rst_ctl` register of the ED Control block. `mgmt_rst_in_n` asserts when `hw_rst` is asserted.

Figure 7. Timing Diagram for the Design Example Resets



3.3. Design Example Signals

Table 15. System Interface Signals

Signal	Direction	Description
Clocks and Resets		
`mgmt_clk`	Input	100 MHz clock for system management.
`refclk_xcvr`	Input	PLL/CDR reference clock for transceiver PHY.
		continued...

Signal	Direction	Description
refclk_core	Input	Core PLL reference clock. Applies the same clock frequency as refclk_xcvr.
global_rst_n	Input	Global reset signal from the push button. This reset is an active low signal and the deassertion of this signal is synchronous to the rising-edge of mgmt_clk.
in_sysref	Input	SYSREF signal from external SYSREF generator for JESD204C Subclass 1 implementation.
sysref_out	Output	SYSREF signal for JESD204C Subclass 1 implementation generated by the FPGA device for design example link initialization purpose only.

Signal	Direction	Description
SPI		
spi_SS_n[2:0]	Output	Active low, SPI slave select signal.
spi_SCLK	Output	SPI serial clock.
spi_sdio *Note:* When **Generate 3-Wire SPI Module** option is enabled.	Input/Output	Output data from the master to external slave. Input data from external slave to master.
spi_MISO *Note:* When **Generate 3-Wire SPI Module** option is not enabled.	Input	Input data from external slave to the SPI master.
spi_MOSI *Note:* When **Generate 3-Wire SPI Module** option is not enabled.	Output	Output data from SPI master to the external slave.

Signal	Direction	Description
ADC/DAC		
tx_serial_data[LINK*L-1:0]	Output	Differential high speed serial output data to DAC. The clock is embedded in the serial data stream.
tx_serial_data_n[LINK*L-1:0]		
rx_serial_data[LINK*L-1:0]	Input	Differential high speed serial input data from ADC. The clock is recovered from the serial data stream.
rx_serial_data_n[LINK*L-1:0]		

Signal	Direction	Description
General Purpose I/O		
user_led[3:0]	Output	Indicates the status for the following conditions: • [0]: SPI programming done • [1]: TX link error • [2]: RX link error • [3]: Pattern checker error for Avalon streaming data
user_dip[3:0]	Input	User mode DIP switch input: • [0]: Internal serial loopback enable • [1]: FPGA-generated SYSREF enable • [3:2]: Reserved

Signal	Direction	Description
Out-of-band (OOB) and Status		
rx_patchk_data_error[LINK-1:0]	Output	When this signal is asserted, it indicates pattern checker has detected error.
rx_link_error[LINK-1:0]	Output	When this signal is asserted, it indicates JESD204C RX IP has asserted interrupt.
tx_link_error[LINK-1:0]	Output	When this signal is asserted, it indicates JESD204C TX IP has asserted interrupt.
emb_lock_out	Output	When this signal is asserted, it indicates JESD204C RX IP has achieved EMB lock.
sh_lock_out	Output	When this signal is asserted, it indicates JESD204C RX IP sync header is locked.

Signal	Direction	Description
Avalon Streaming		
rx_avst_valid[LINK-1:0]	Input	Indicates whether the converter sample data to the application layer is valid or invalid. • 0: Data is invalid • 1: Data is valid
rx_avst_data[LINK-1:0] [(TOTAL_SAMPLE*N)-1:0]	Input	Converter sample data to the application layer.

3.4. JESD204C Design Example Control Registers

The JESD204C design example registers in the ED Control block use byte-addressing (32 bits).

Table 16. Design Example Address Map

These 32-bit ED Control block registers are in the mgmt_clk domain.

Component	Address
ED Control	0x0102_0400 – 0x0102_04FF
MM Bridge	0x0000_0000 – 0x007F_FFFF
PIO Control	0x0102_0020 – 0x0102_002F
PIO Status	0x0102_0040 – 0x0102_004F
Reset Sequencer 0	0x0102_0100 – 0x0102_01FF
Reset Sequencer 1	0x0102_0200 – 0x0102_02FF
SPI Control	0x0102_0000 – 0x0102_001F
JESD204C IP transceiver PHY Reconfig	0x0200_0000 – 0x020F_FFFF (2-lane transceiver PHY)
	0x0200_0000 – 0x021F_FFFF (4-lane transceiver PHY)
JESD204C TX IP (Link 0)	0x000C_0000 – 0x000C_03FF
JESD204C RX IP (Link 0)	0x000D_0000 – 0x000D_03FF

Table 17. Register Access Type and Definition

This table describes the register access type for Intel FPGA IPs.

Access Type	Definition
RO/V	Software read-only (no effect on write). The value may vary.
RW	• Software reads and returns the current bit value. • Software writes and sets the bit to the desired value.
RW1C	• Software reads and returns the current bit value. • Software writes 0 and has no effect. • Software writes 1 and clears the bit to 0 if the bit has been set to 1 by hardware. • Hardware sets the bit to 1. • Software clear has higher priority than hardware set.

Table 18. ED Control Block Control and Status Registers

Byte Offset	Register	Name	Access	Reset	Description
0x00	rst_ctl	rst_assert	RW	0x0	Reset control. [0]: Assert software global reset at mgmt_rst_in_n by writing 1 to this bit. Write 0 to this bit to deassert global reset.. [31:1]: Reserved.
0x04	rst_sts0	rst_status	RO/V	0x0	Reset status. [0]: Core PLL locked status. [31:1]: Reserved.
0x08	rst_sts1		RO/V	0x0	Reset status. [15:0]: tx_pma_ready status for TX lane 0 to lane 15. LSB for TX lane 0. [31:16]: rx_pma_ready status for RX lane 0 to lane 15. Bit 16 for RX lane 0.
0x0c	rst_sts2		RO/V	0x0	Reserved.
0x10	rst_sts_detected0	rst_sts_set	RW1C	0x0	SYSREF edge detection status for internal or external SYSREF generator. [0]: Value of 1 Indicates a SYSREF rising edge is detected for subclass 1 operation. Software may write 1 to clear this bit to enable new SYSREF edge detection. [31:1]: Reserved.
0x14	rst_sts_detected1		RW1C	0x0	Reserved.
0x40	sysref_ctl	sysref_control	RW	Duplex datapath • One-shot: 0x00080 • Periodic: 0x00081 • Gapped-periodic: 0x00082	SYSREF control. Refer to Table 10 on page 17 for more information about the usage of this register. *Note:* The reset value depends on the SYSREF type and JESD204C IP data path parameter settings.

continued...

Byte Offset	Register	Name	Access	Reset	Description
				TX or RX data path • One-shot: 0x00000 • Periodic: 0x00001 • Gapped-periodic: 0x00002	
0x44	sysref_sts	sysref_status	RO/V	0x0	SYSREF status. This register contains the latest SYSREF period and duty cycle settings of the internal SYSREF generator. Refer to Table 9 on page 17 for the legal value of the SYSREF period and duty cycle. [7:0]: SYSREF period. • When the value is 0xFF, the SYSREF period = 255. • When the value if 0x00, the SYSREF period = 256. [15:8]: SYSREF duty cycle. [31:16]: Reserved.
0x80	tst_ctl	tst_control	RW	0x0	Test control. Use this register to enable different test patterns for the pattern generator and checker. [1:0] = prbs_test_ctl • 2'b00 = PRBS23 • 2'b01 = PRBS15 • 2'b10 = PRBS9 • 2'b11 = PRBS7 [2] = ramp_test_ctl • 1'b0 = Enable PRBS pattern • 1'b1 = Enable ramp pattern [31:3]: Reserved.
0x84	tst_sts0	tst_status	RW1C	0x0	Reserved.
0x88	tst_sts1		RW1C	0x0	Reserved.
0x8c	tst_err0	tst_error	RW1C	0x0	Error flag for Link 0. When the bit is 1'b1, it indicates an error has happened. You should resolve the error before writing 1'b1 to the respective bit to clear the error flag. [0] = Pattern checker error [1] = tx_link_error [2] = rx_link_error [3] = Command pattern checker error [31:4]: Reserved.
0x90	tst_err1		RW1C	0x0	Reserved.

4. Document Revision History for the JESD204C Intel Agilex FPGA IP Design Example User Guide

Document Version	Intel Quartus Prime Version	IP Version	Changes
2019.10.23	19.3	1.0.0	Initial release.