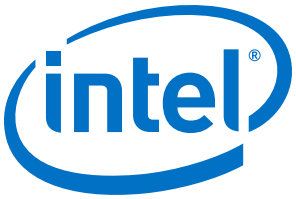

Altera ASMI Parallel II IP Core User Guide

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Contents

1 Altera ASMI Parallel II IP Core User Guide

The Altera ASMI Parallel II IP core provides access to the Intel FPGA configuration devices which are the quad-serial configuration (EPCQ) and low-voltage quad-serial configuration (EPCQ-L) device.

Other than features supported by *Altera ASMI Parallel IP core*, the Altera ASMI Parallel II IP core additionally supports:

- Direct flash access (write/read) through the Avalon-Memory Map (Avalon-MM) interface.
- Control register for other operations through the control status register (CSR) interface in Avalon-MM.

The Altera ASMI Parallel II IP core is available for all Intel FPGA device families except the MAX® series.

Note: The Altera ASMI Parallel II IP core is supported in Quartus® Prime version 17.0 or later

Related Links

- Introduction to Intel FPGA IP Cores
  Provides general information about all Intel FPGA IP cores, including parameterizing, generating, upgrading, and simulating IP cores.
- Creating Version-Independent IP and Qsys Simulation Scripts
  Create simulation scripts that do not require manual updates for software or IP version upgrades.
- Project Management Best Practices
  Guidelines for efficient management and portability of your project and IP files.
- Altera ASMI Parallel IP Core User Guide
- AN-720: Simulating the ASMI Block in Your Design

1.1 Ports

Figure 1. Ports Block Diagram

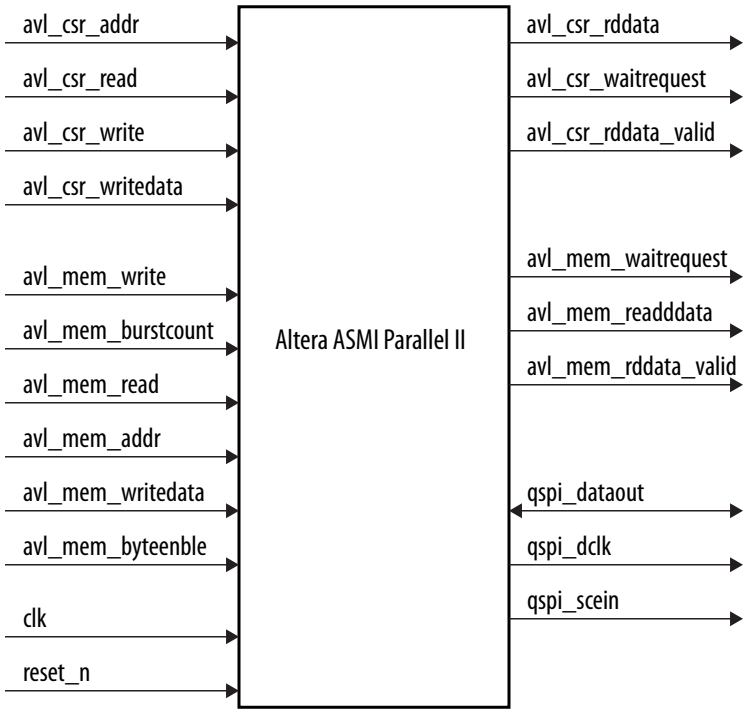


Table 1. Ports Description

Signal	Width	Direction	Description
Avalon-MM slave interface for CSR (avl_csr)			
avl_csr_addr	6	Input	Avalon-MM address bus. The address bus is in word addressing.
avl_csr_read	1	Input	Avalon-MM read control to the CSR.
avl_csr_rddata	32	Output	Avalon-MM read data bus from the CSR.
avl_csr_write	1	Input	Avalon-MM write control to the CSR.
avl_csr_writedata	32	Input	Avalon-MM write data bus to CSR.
avl_csr_waitrequest	1	Output	Avalon-MM waitrequest control from the CSR
avl_csr_rddata_valid	1	Output	Avalon-MM read data valid that indicates the CSR read data is available.
Avalon-MM slave interface for memory access (avl_ mem)			
avl_mem_write	1	Input	Avalon-MM write control to the memory
avl_mem_burstcount	7	Input	Avalon-MM burst count for the memory. The value range from 1 to 64 (Max page size).
avl_mem_waitrequest	1	Output	Avalon-MM waitrequest control from the memory.
avl_mem_read	1	Input	Avalon-MM read control to the memory

continued...

Signal	Width	Direction	Description
avl_mem_addr	N	Input	Avalon-MM address bus. The address bus is in word addressing. The width of the address depends on the flash memory density minus 2. If you are using Arria® 10, then the MSB bits will be used for chip select information. You can select the number of chip select needed in the parameter setting. • If you select 1 chip select in the parameter setting, there will be no extra bit added to avl_mem_addr. • If you select 2 chip selects, there will be one extra bit added to avl_mem_addr: — Chip 1— b'0 — Chip 2—b'1 • If user select 3 chip selects, there will be two extra bits added to avl_mem_addr: — Chip 1—b'00 — Chip 2—b'01 — Chip 3—b'10
avl_mem_writedata	32	Input	Avalon-MM write data bus to the memory
avl_mem_readddata	32	Output	Avalon-MM read data bus from the memory.
avl_mem_rddata_valid	1	Output	Avalon-MM read data valid that indicates the memory read data is available.
avl_mem_byteenble	4	Input	Avalon-MM write data enable bus to memory. During bursting mode, byteenable bus will be logic high, 4'b1111.
Clock and Reset			
clk	1	Input	Input clock to clock the IP core.
reset_n	1	Input	Asynchronous reset to reset the IP core.[1]
Conduit Interface[2]			
fqspi_dataout	4	Bidirectional	Input or output port to feed data from the flash device.
qspi_dclk	1	Output	Provides clock signal to the flash device.
qspi_scein	1/3	Output	Provides the ncs signal to the flash device.

Related Links

- Quad-Serial Configuration (EPCQ) Devices Datasheet
- EPCQ-L Serial Configuration Devices Datasheet

1.2 Parameters

Table 2. Parameter Settings

Parameter	Legal Values	Descriptions
Configuration device type	EPCQ16, EPCQ32, EPCQ64,	Specifies the EPCQ or EPCQ-L type you want to use.

continued...

1 Hold the signal for at least one clock cycle to reset the IP.

2 Available when you enable the **Disable dedicated Active Serial interface** parameter.

Parameter	Legal Values	Descriptions
	EPCQ128, EPCQ256, EPCQ512, EPCQ-L256, EPCQ-L512, EPCQ-L1024	
Choose I/O mode	NORMAL STANDARD DUAL QUAD	Selects extended data width when you enable the Fast Read operation.
Disable dedicated Active Serial interface	—	Routes the ASMIBLOCK signals to the top level of your design.
Enable SPI pins interface	—	Translates the ASMIBLOCK signals to the SPI pin interface.
Enable flash simulation model	—	Uses the flash inside the device for simulation model.
Number of Chip Select used	1 2[3] 3[3]	Selects the number of chip select connected to the flash.

Related Links

- Quad-Serial Configuration (EPCQ) Devices Datasheet
- EPCQ-L Serial Configuration Devices Datasheet
- AN-720: Simulating the ASMI Block in Your Design

1.3 Register Map

Table 3. Register Map

- Each address offset in the following table represents 1 word of memory address space.
- All registers have a default value of 0x0.

Offset	Register Name	R/W	Field Name	Bit	Width	Description
0	WR_ENABLE	W	WR_ENABLE	0	1	Write 1 to perform write enable.
1	WR_DISABLE	W	WR_DISABLE	0	1	Write 1 to perform write disable.
2	WR_STATUS	W	WR_STATUS	7:0	8	Contains the information to write to the status register.
3	RD_STATUS	R	RD_STATUS	7:0	8	Contains the information from read status register operation.
4	SECTOR_ERASE	W	Sector Value	9:0	10	Contain the sector address to be erased.[4]

continued...

3 Only supported in Arria 10 devices and other devices with **Enable SPI pins interface** enabled.

Offset	Register Name	R/W	Field Name	Bit	Width	Description
5	SUBSECTOR_ERASE	W	Subsector Value	14:0	15	Contains the subsector address to be erased.[5]
6 - 7	Reserved					
8	CONTROL	W/R	CHIP SELECT	7:4	4	Select chip select in binary value. To select first device, set the value to 1, to select second device, set the value to 2.
		Reserved				
		W/R	DISABLE	0	1	Set this to 1 to disable the SPI signals of the IP by putting all output signal to high-Z state. This can be used to share bus with other devices.
9 - 12	Reserved					
13	WR_NON_VOLATILE_CONF_REG	W	NVCR value	15:0	16	Writes value to non-volatile configuration register.
14	RD_NON_VOLATILE_CONF_REG	R	NVCR value	15:0	16	Reads value from non-volatile configuration register
15	RD_ FLAG_ STATUS_REG	R	RD_ FLAG_ STATUS_REG	8	8	Reads flag status register
16	CLR_FLAG_ STATUS REG	W	CLR_FLAG_ STATUS REG	8	8	Clears flag status register
17	BULK_ERASE	W	BULK_ERASE	0	1	Write 1 to erase entire chip (for single-die device).[6]
18	DIE_ERASE	W	DIE_ERASE	0	1	Write 1 to erase entire die (for stack-die device).[6]
19	4BYTES_ADDR_EN	W	4BYTES_ADDR_EN	0	1	Write 1 to enter 4 bytes address mode
20	4BYTES_ADDR_EX	W	4BYTES_ADDR_EX	0	1	Write 1 to exit 4 bytes address mode

continued...

4 You only need to specify the sector address. The IP core will automatically construct the full address and send to the device.

5 You only need to specify the subsector address. The IP core will automatically construct the full address and send to the device.

6 Refer to the EPCQ-L Device Datasheet for information about single or stack-die device.

Offset	Register Name	R/W	Field Name	Bit	Width	Description
21	SECTOR_PROTECT	W	Sector protect value	4:0	5	Value to write to status register to protect a sector.
22	RD_MEMORY_CAPACITY_ID	R	Memory capacity value	7:0	8	Contains the information of memory capacity ID.
23 - 32	Reserved					

Related Links

- Quad-Serial Configuration (EPCQ) Devices Datasheet
- EPCQ-L Serial Configuration Devices Datasheet
- Avalon Interface Specifications

1.4 Operations

The Altera ASMI Parallel II IP core interfaces are Avalon-MM compliant. For more details, please refer to the Avalon specification.

Related Links

Avalon Interface Specifications

1.4.1 Control Status Register Operations

You can perform a read or write to a specific address offset using the Control Status Register (CSR).

To execute the read or read operation for the control status register, perform the following steps:

1. Assert the `avl_csr_write` or `avl_csr_read` signal while the `avl_csr_waitrequest` signal is low (if the `waitrequest` signal is high, the `avl_csr_write` or `avl_csr_read` signal must to be kept high until the `waitrequest` signal goes low.)
2. At the same time, set address value on `avl_csr_address` bus. If it is a write operation, set value data on the `avl_csr_writedata` bus together with the address.
3. If it is a read transaction, wait until `avl_csr_readdatavalid` signal is asserted high to retrieve the read data.

- For operations that require write value to flash, you must perform write enable operation first.
- You must read the flag status register every time you issue a write or erase command.
- In case of support multiples flash devices, you must write chip select register to select the correct chip select before performing any operation to the specific flash device.

Figure 2. Read Memory Capacity Register Waveform Example

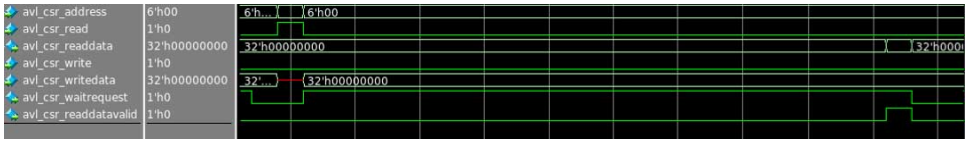
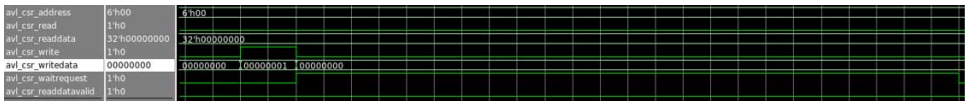


Figure 3. Write Enable Register Waveform Example



1.4.2 Memory Operations

The ASMI Parallel II IP core memory interface supports bursting and direct flash memory access. During direct flash memory access, the IP core performs the following steps to allow you to perform any direct read or write operation:

- Write enable for write operation
- Check flag status register to make sure the operation has been completed at the flash
- Release `waitrequest` signal when operation completed

Memory operations are similar to the Avalon-MM operations. You must set the correct value at address bus, write data if it is write transaction, drive burst count bus 1 if single transaction or desired burst count value and trigger the write or read signal.

Figure 4. 8-Word Write Burst Waveform Example

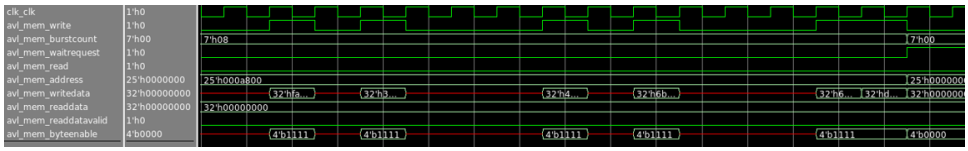


Figure 5. 8-Word Reading Burst Waveform Example

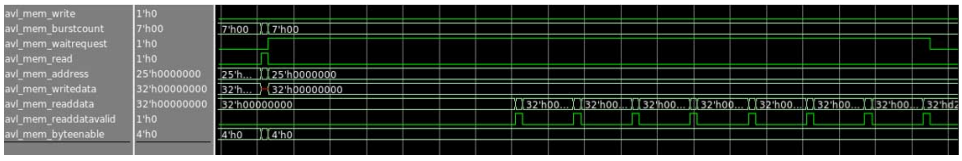
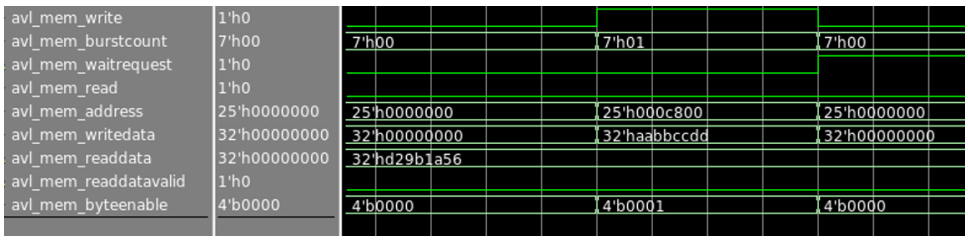


Figure 6. 1-Byte Write `byteenable = 4'b0001` Waveform Example



1.5 Document Revision History

Date	Version	Changes
May 2017	2017.05.08	Initial release.