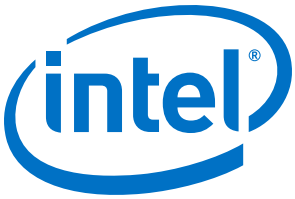

Chip ID Intel FPGA IP Cores User Guide

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Chip ID Intel® FPGA IP Cores User Guide

Each supported Intel® FPGA has a unique 64-bit chip ID. Chip ID Intel FPGA IP cores allow you to read out this chip ID for device identification.

Related Information

- Introduction to Altera IP Cores
  Provides general information about all Intel FPGA IP cores, including parameterizing, generating, upgrading, and simulating IP cores.
- Creating Version-Independent IP and Qsys Simulation Scripts
  Create simulation scripts that do not require manual updates for software or IP version upgrades.
- Project Management Best Practices
  Guidelines for efficient management and portability of your project and IP files.

Device Support

Table 1. IP Cores and the Supported Devices

IP Cores	Supported Devices
Chip ID Intel Stratix 10 FPGA IP core	Intel Stratix® 10
Unique Chip ID Intel Arria 10 FPGA IP core	Intel Arria® 10
Unique Chip ID Intel Cyclone 10 GX FPGA IP core	Intel Cyclone® 10 GX
Altera Unique Chip ID IP core	Stratix V Arria V Cyclone V

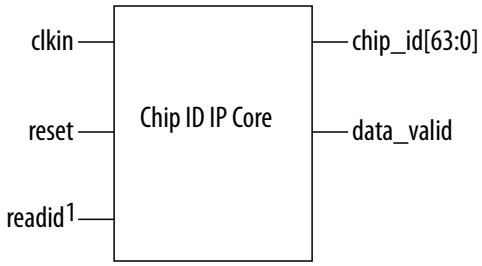
Functional Description

The `data_valid` signal starts low in the initial state where no data is being read from the device. After feeding a clock signal to the `clkin` input port, the chip ID IP core reads the unique chip ID. After reading, the IP core asserts the `data_valid` signal to indicate that the unique chip ID value at the output port is ready for retrieval. The operation repeats only when you reset the IP core.

The `chip_id[63:0]` output port holds the value of the unique chip ID until you reconfigure the device or reset the IP core.

Ports

Figure 1. Chip ID Ports



Note:

1. Applicable in Intel Stratix 10 devices only.

Table 2. Chip ID Ports

Port	I/O	Size (Bit)	Description
`clkin`	Input	1	Feeds clock signal to the chip ID block. The maximum supported frequencies are • For Intel Stratix 10: Equivalent to your system clock. • For Intel Arria 10 and Intel Cyclone 10 GX: 30 MHz. • For Stratix V, Arria V and Cyclone V: 100 MHz. When you provide a clock signal, the IP core reads the value of the unique chip ID and sends the value to the `chip_id` output port.
`reset`	Input	1	Synchronous reset that resets the IP core. For devices other than the Intel Stratix 10, to reset the IP core, assert the `reset` signal high for at least 10 `clkin` cycles. The `chip_id [63:0]`output port holds the value of the unique chip ID until you reconfigure the device or reset the IP core.
`data_valid`	Output	1	Indicates that the unique chip ID is ready for retrieval. If the signal is low, the IP core is in initial state or in progress to load data from a fuse ID. After the IP core asserts the signal, the data is ready for retrieval at the `chip_id[63..0]` output port.
`chip_id`	Output	64	Indicates the unique chip ID according to its respective fuse ID location. The data is only valid after the IP core asserts the `data_valid` signal. The value at power-up resets to `0`.
`readid`	Input	1	Applicable to Intel Stratix 10 devices only. Reads the device ID. To read the device ID, drive the signal high for at least 10 `clkin` cycles, then pull the signal low.

Accessing Intel Arria 10 and Intel Cyclone 10 GX Chip ID through JTAG

Note: The Intel Arria 10 and Intel Cyclone 10 GX chip ID is inaccessible if you have other systems or IP cores accessing the JTAG simultaneously. For example, the SignalTap II Logic Analyzer, Transceiver Toolkit, in-system signals or probes, and the SmartVID Controller IP core.

When you toggle the reset signal, the chip ID IP core starts reading the chip ID from the Intel Arria 10 or Intel Cyclone 10 GX device. When the chip ID is ready, the chip ID IP core asserts the `data_valid` signal and ends the JTAG access.

Note: Allow a delay equivalent to t_{CD2UM} after full chip configuration before attempting to read the unique chip ID. Refer the respective device datasheet for t_{CD2UM} value.

Resetting the IP Core

To reset the IP core, you must assert the reset signal for at least ten clock cycles. After you deassert the reset signal, the IP core rereads the unique chip ID from the fuse ID block. The IP core asserts the `data_valid` signal after completing the operation.

Note: For Intel Arria 10, Stratix V, Arria V, and Cyclone V devices, do not reset the IP core until at least t_{CD2UM} after full chip initialization. Refer the respective device datasheet for t_{CD2UM} value.

Document Revision History for Chip ID Intel FPGA IP Cores User Guide

Document Version	Intel Quartus® Prime Version	Changes
2018.06.08	18.0	• Updated the `readid` port description. • Updated the `reset` port description.
2018.05.07	18.0	Added `readid` port for Chip ID Intel Stratix 10 FPGA IP core.

Date	Version	Changes
December 2017	2017.12.11	• Updated document title from *Altera Unique Chip ID IP Core User Guide*. • Added *Device Support* section. • Combined and added information from *Altera Arria 10 Unique Chip ID IP Core User Guide* and *Stratix 10 Unique Chip ID IP Core User Guide*. • Rebranded to Intel. • Updated *Functional Description*. • Added Intel Cyclone 10 GX device support.
May 2016	2016.05.02	• Removed standard IP core information and added link to Quartus Prime Handbook. • Updated note about Arria 10 device support.
September, 2014	2014.09.02	• Updated document title to reflect new name of "Altera Unique Chip ID" IP core.
August, 2014	2014.08.18	• Updated parameterization steps for legacy parameter editor. • Added note that this IP core does not support Arria 10 designs.

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Date	Version	Changes
June, 2014	2014.06.30	• Replaced MegaWizard Plug-In Manager information with IP Catalog. • Added standard information about upgrading IP cores. • Added standard installation and licensing information. • Removed outdated device support level information. IP core device support is now available in IP Catalog and parameter editor.
September, 2013	2013.09.20	Updated to reword "Acquiring the chip ID of an FPGA device" to "Acquiring the unique chip ID of an FPGA device"
May, 2013	1.0	Initial release.