

## High-Speed Board Design Advisor *Hardware Integration, Test, and Debug*

### Introduction

This document contains a step-by-step guide to help designers with hardware integration, testing, and debugging of their high-speed channel design with Altera® Stratix® II GX FPGAs. Familiarity with the following tools and support collateral is assumed:

- *Stratix II GX Handbook:*  
[www.altera.com/literature/lit-s2gx.jsp](http://www.altera.com/literature/lit-s2gx.jsp)
- *Quartus® II Development Software Handbook:*  
[www.altera.com/literature/lit-qts.jsp](http://www.altera.com/literature/lit-qts.jsp)

Altera also offers Stratix II GX FPGA-based development kits, which deliver high-quality, proven implementations with board schematics, layout files, and board-specific guidelines that can be used as a starting point for user designs:


- Transceiver Signal Integrity Development Kit, Stratix II GX Edition:  
[www.altera.com/products/devkits/altera/kit-signal\\_integrity\\_s2gx.html](http://www.altera.com/products/devkits/altera/kit-signal_integrity_s2gx.html)
- PCI Express Development Kit, Stratix II GX Edition:  
[www.altera.com/products/devkits/altera/kit-pciexpress\\_s2gx.html](http://www.altera.com/products/devkits/altera/kit-pciexpress_s2gx.html)
- Audio Video Development Kit, Stratix II GX Edition:  
[www.altera.com/products/devkits/altera/kit-dsp-professional.html](http://www.altera.com/products/devkits/altera/kit-dsp-professional.html)

### Stratix II GX High-Speed Channel Design Test and Debug Guidelines


#### *Identify Design Goals*

Before debugging the high-speed channel, identify the design goals of the high-speed channel to help evaluate the scope of the problem:


- What are the data rates and edge rates?
- How many channels are required?
- What are the lengths of the high-speed channels?
- What are the  $V_{OD}$ , equalization, and pre-emphasis values?

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 Refer to the Stratix II GX Transceiver User Guide section of the *Stratix II GX Handbook* for further information about transceivers modes and features:  
[www.altera.com/literature/hb/stx2gx/stxiigx\\_sii5v2\\_01.pdf](http://www.altera.com/literature/hb/stx2gx/stxiigx_sii5v2_01.pdf)


#### *Verify Basic Transceiver Settings*

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 For settings, specifications, and requirements, please refer to the *Stratix II GX Handbook*. Keywords that can be used to search the document are indicated in *italic*.

- Verify the connectivity of the high-speed channels (cables, connectors, internal loopbacks).
- Verify the basic settings of the transceiver blocks (ALT2GXB) from the Altera MegaWizard® Plug-In. (Keyword: *ALT2GXB*)
- Verify the termination scheme for the receiver and transmitter. (Keywords: *Programmable Termination, Calibration Blocks*)
  - If on-chip termination (OCT) is used, make sure it is turned on.
  - Make sure the calibration block is turned on and configured correctly.
  - If external termination is used, make sure that external termination resistors are in the schematic or used in the connectors (e.g., SFP modules with integrated termination resistors).

- ❑ Verify the compatibility of I/O standards and voltage levels for transceiver I/Os. Stratix II GX FPGAs offer 1.2-V and 1.5-V pseudo current mode logic (PCML). (Keyword: *PCML*)
  - ❑ Verify the coupling scheme. (Keywords: *Coupling*,  $V_{CM}$ )
    - Make sure the coupling schemes of receiver and transmitter match.
    - AC coupling:
  - ❑ Check the values of decoupling capacitors (Altera recommends  $C > 1$  nF).
  - ❑ Check the size (small form factor recommended, 0402 and smaller).
  - ❑ Check the position and the differential skew (it should be near Rx or Tx, it does not matter unless the differential lines are skew-balanced).
  - ❑ Check layout and design for impedance matching.
    - DC coupling:
  - ❑ Check the compatibility of common-mode voltage ( $V_{CM}$ ). (Keyword:  $V_{CM}$ )
  - ❑ Check external resistor network for  $V_{CM}$  adoption, if applicable. (Keywords: *External Termination and Biasing Circuit*)
  - ❑ Verify that the data rates match between transmitters and receivers.
  - ❑ Verify the settings of the transceiver reference clocks “refclk.” (Keywords: *Stratix II GX Transceiver Block AC Specification*, *REFCLK*)
    - Connectivity (refclk1 and refclk0)
    - I/O standard, voltage levels, and clock rate
    - Termination scheme
    - Input jitter
    - Matching clock rate and data rate settings
    - Reference clock distribution between transceiver blocks
  - ❑ Verify the compatibility of the parts per million (PPM) difference settings between transmitters and receivers. (Keyword: *PPM Difference*)
    - Debug the PPM difference problems by changing from automatic lock mode to manual lock mode. This change allows manual switching between lock-to-reference mode and lock-to-data modes while bypassing the PPM check in automatic mode. (Keywords: *Lock-to-Reference*, *Lock-to-Data Modes*)
  - ❑ Verify the phase-locked loop (PLL) bandwidth settings. (Keyword: *PLL Bandwidth*)
  - ❑ Verify the pre-emphasis and equalization setting.
-  Refer to the techniques described in “Signal Integrity Optimization Techniques,” in the *Stratix II GX Handbook* (Keywords: *Programmable Equalization*, *Programmable Pre-Emphasis*)
- ❑ Verify RREFB pin.
    - Verify the use of the RREFB reference resistor ports. (Keyword: *RREFB*)
    - Check that they are  $2.00K\Omega \pm 1\%$  and that they are not shared between different pins.
    - Capture the noise on these ports. They should be as clean as possible.

### Verify Clocking Scheme

- ❑ Refer to the systems clock concept diagram, and verify the reference clock and system clock sources and modes.
-  For clocking schemes of the transceivers (ALT2GXB), refer to the following *Stratix II GX Handbook* sections:
- Transceivers: “Stratix II GX Transceiver Clocking”
  - PLLs and clock networks: “Global & Hierarchical Clocking,” “PLL Specifications”

### Verify Reset and Power-Down Scheme and Sequence

- ❑ Check the reset and power-down design and sequence.

- Refer to the “Reset Control & Power-Down” section in the Stratix II GX Transceiver Architecture Overview, *Stratix II GX Handbook*. Keywords:
  - *User Resets, Enable Signals*
  - *Blocks Affected by Reset and Power-Down Signals*
  - *Reset and Power-Down Signal Timing Waveform*
  - For PCI Express: *PIPE Mode Reset Sequence*
- Altera recommends that a proper reset sequence is followed during and after channel reconfiguration. (Keyword: *Reset Recommendations*)

### Verify Differential Signals

Verify with both transmitter (Tx) and receiver (Rx) measurements.

#### Transmitter Measurements

- Check basic signal characteristics: amplitude, timing, and jitter generation.
- Tx amplitude measurements:
  - Minimum differential peak-to-peak voltage
  - Pre-/de-emphasis
  - Common-mode voltage (AC, DC)
  - Waveform eye-height, measured at the 0.5 unit interval (UI) point where the UI timing reference is determined by the recovered clock.
- Tx timing measurements:
  - Unit interval and bitrate
  - Rise/fall time
  - Waveform eye width
- Tx jitter measurements
- Tx eye diagram and mask testing


#### Receiver Measurements

- Check basic signal characteristics: amplitude, timing, and jitter tolerance.
- Put the device under test in a loopback mode.
- Insert a test pattern. Depending on the protocol standard, training packets, pseudo-random bitstream (PRBS), or logic and analog waveforms (AWG) will be used.
- Rx amplitude sensitivity measurements:
  - Using a data generator, adjust the amplitude to nominal value.
  - Decrease or increase amplitude until the unit fails to respond correctly.
  - Verify amplitude is outside specification when the failure occurs.
- Rx jitter tolerance measurements:
  - Check the ability to recover data successfully in the presence of jitter.
  - Insert jitter from a jitter generator to make sure the clock data recovery (CDR) can track the input.
- Rx timing skew measurements:
  - Vary the timing skew between differential pairs to allow for tolerances in board layout and cabling.
- Receiver PLL loop bandwidth measurements:
  - Ensure that DUT receives a modulated reference clock (Gaussian noise source).
  - Measure the ratio of the output jitter to the input jitter in the frequency domain.
- Receiver pre-/de-emphasis generation and testing.

### Verify the High-Speed Channel Layout


- Impedance matching
- Impedance discontinuities:
  - BGA breakout

- Differential vias
- DC blocking capacitors
- Connectors
- Differential skew
- Measurements: PCB transmission line characterization via time-domain reflectometry (TDR)
  - Measure characteristic impedance and uniformity of a transmission line.
  - Measure time delay of a transmission line.
  - Build a high-bandwidth model of a component (S parameters).
  - Simulate with HSPICE. Contact Altera support for HSPICE models of the transceivers:  
[www.altera.com/corporate/contact/con-index.html](http://www.altera.com/corporate/contact/con-index.html).

 Refer to *High-Speed Board Design Advisor: High-Speed Channel Design and Layout* for further guidance:  
[www.altera.com/literature/tb/tb-095.pdf](http://www.altera.com/literature/tb/tb-095.pdf).

### Verify the Power Distribution Network (PDN) Design

- Examine power rails.
  - Verify all voltage connections around the transceivers.
  - Verify voltage levels and planes.
- Check for noise on these rails (ripple tolerance).
- Replace on-board supplies with bench supply for comparison.
- Take low impedance measurements of the PDN.

 Refer to *High-Speed Board Design Advisor: Power Distribution Network* for further guidance:  
[www.altera.com/literature/tb/tb-092.pdf](http://www.altera.com/literature/tb/tb-092.pdf).

## Debug and Optimize Design

Use the techniques described here to further debug and optimize the design.

### General Debug Techniques

- Put in simple PRBS design to see if errors are board related or design related.
- Disable memory interfaces or large logic portions and check for improvement.
- Slow down the interface and check for improvement.
- Use the in-system debugging tools provided with the Quartus II development software, such as the SignalTap® II logic analyzers, SignalProbe feature, and Logic Analyzer Interface.
- Use in-system debugging tools, such as Tektronix FPGAView™ software for configuring and debugging Altera FPGAs with Tektronix Logic Analyzers:  
[www.tektronix.com](http://www.tektronix.com).

### Signal Integrity Optimization Techniques

Stratix II GX transceivers provide highly configurable pre-emphasis and equalization circuitry to compensate for transmission line losses. Various tools and techniques are available to help optimize the high-speed channel and get the bit error rate (BER) required for the system performance:

- Stratix II GX Eye Diagram Viewer for online characterization:  
[www.altera.com/technology/signal/devices/stratix2gx/character/sgl-s2gx-character.html#siigxviewer](http://www.altera.com/technology/signal/devices/stratix2gx/character/sgl-s2gx-character.html#siigxviewer)
- Altera's pre-emphasis and equalization link estimator (PELE) technology:  
[www.altera.com/technology/signal/devices/stratix2gx/character/sgl-s2gx-tools.html](http://www.altera.com/technology/signal/devices/stratix2gx/character/sgl-s2gx-tools.html)
- Plug and Play Signal Integrity featuring Altera's adaptive dispersion compensation engine (ADCE) technology and hot-socketable transceivers:  
[www.altera.com/technology/signal/ppsi/sgl-plugin-and-play-si.html](http://www.altera.com/technology/signal/ppsi/sgl-plugin-and-play-si.html)

- Stratix II GX signal integrity:  
[www.altera.com/technology/signal/devices/stratix2gx/features/sgl-s2gx-features.html](http://www.altera.com/technology/signal/devices/stratix2gx/features/sgl-s2gx-features.html)

For more information about Stratix II GX signal integrity features, pre-emphasis, and equalization, refer to the *Stratix II GX Handbook*. (Keywords: *Pre-Emphasis, Equalization*)

### In-System Debugging

Quartus II development software offers a number of tools for in-system debugging, including the SignalProbe feature, SignalTap II logic analyzer, Logic Analyzer Interface, Chip Planner, and In-System Memory Content Editor, described below,

For detailed information on in-system debugging using these tools, refer to Section V, “In-System Design Debugging,” in the *Quartus II Handbook*, Volume 3.

### Chapter 12: Quick Design Debugging Using SignalProbe

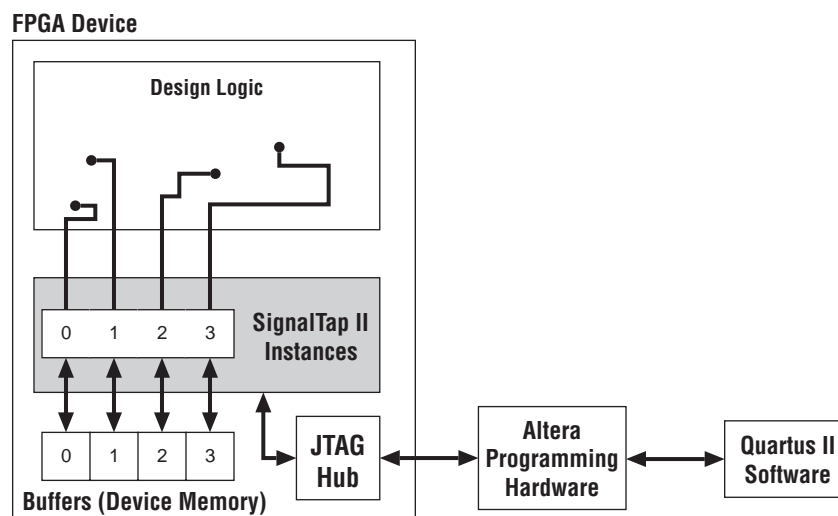
The SignalProbe feature enables easy access to internal device signals for debugging purposes. This allows quick routing of internal signals to either previously reserved or currently unused I/O pins without affecting the design.

### Chapter 13: Design Debugging Using the SignalTap II Embedded Logic Analyzer

The SignalTap II Embedded Logic Analyzer, shown in Figure 1, enables designers to examine the behavior of internal signals, without using extra I/O pins, while the design is running at full speed on the FPGA. It offers the following advantages:

- External equipment or external probes are not required.
- Changes to the design files to capture the state of the internal nodes or I/O pins in the design are not required.
- Custom trigger-condition logic provides greater accuracy and improves the ability to isolate problems in the device.
- All captured signal data is conveniently stored in device memory and can be read out and analyzed by the Quartus II software via JTAG.

Figure 1. SignalTap II Logic Analyzer Block Diagram



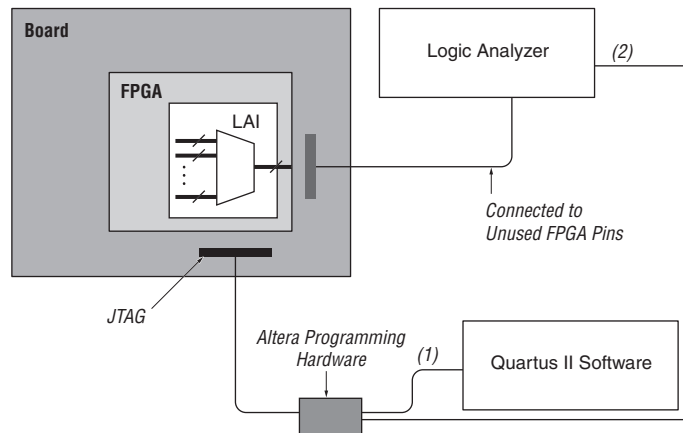
#### Note to Figure 1:

- (1) This diagram assumes that the SignalTap II Logic Analyzer was compiled with the design as a separate design partition using the Quartus II Incremental Compilation feature. This is the default setting for new projects in the Quartus II software. If incremental compilation is disabled or not used, the SignalTap II logic is integrated with the design.

## Chapter 14: In-System Debugging Using External Logic Analyzers

The Logic Analyzer Interface, shown in Figure 2, is an application within the Quartus II software used to connect a large set of internal device signals to a small number of output pins. These output pins can be connected to an external logic analyzer for debugging purposes. Internal signals are grouped together, distributed to a user-configurable multiplexer that can be controlled via JTAG, and then output to available I/O pins on the FPGA.

Figure 2. Logic Analyzer Interface and Hardware Setup



### Notes to Figure 2:

- (1) Configuration and control of the Logic Analyzer Interface using a computer loaded with Quartus II software via the JTAG port.
- (2) Configuration and control of the Logic Analyzer Interface using a third-party vendor logic analyzer via the JTAG port. Support varies by vendor.

## Chapter 15: Design Analysis and Engineering Change Management With Chip Planner

The Chip Planner (Floorplan and Chip Editor) is a powerful tool within the Quartus II software to perform design analysis, create a design floorplan, and implement engineering change orders (ECOs) in the design. For ECOs and design analysis, Chip Planner works directly on the post place-and-route database of the design so design changes can be implemented in minutes without performing a full compilation.

## Chapter 16: In-System Updating of Memory and Constants

The Quartus II In-System Memory Content Editor gives access to device memories and constants via JTAG. The ability to read data from memories and constants allows the quick identification of the source of problems. In addition, the write capabilities allow the bypassing of functional issues by writing expected data. To use this feature, the selected memory or constant needs to be configured as run-time modifiable when created using the MegaWizard Plug-In Manager.

## Additional Information

- Tektronix offers application notes and primers on specific topics and serial standards, how to test them, and what equipment to use:
  - Jitter: [www.tek.com/Masurement/applications/serial\\_data/jitter.html](http://www.tek.com/Masurement/applications/serial_data/jitter.html)
  - Signal Integrity: [www.tek.com/Masurement/applications/design\\_analysis/signal\\_integrity.html](http://www.tek.com/Masurement/applications/design_analysis/signal_integrity.html)
  - TDR and S-Parameters: [www.tek.com/Masurement/applications/design\\_analysis/tdr.html](http://www.tek.com/Masurement/applications/design_analysis/tdr.html)
  - Optical: [www.tek.com/Masurement/applications/serial\\_data/optical/](http://www.tek.com/Masurement/applications/serial_data/optical/)

- Agilent:  
**[www.agilent.com](http://www.agilent.com)**
- LeCroy:  
**[www.lecroy.com](http://www.lecroy.com)**
- Wavecrest:  
**[www.wavecrest.com](http://www.wavecrest.com)**
- *High-Speed Board Design Advisor: Power Distribution Network:*  
**[www.altera.com/literature/tb/tb-092.pdf](http://www.altera.com/literature/tb/tb-092.pdf)**
- *High-Speed Board Design Advisor: Thermal Management:*  
**[www.altera.com/literature/tb/tb-093.pdf](http://www.altera.com/literature/tb/tb-093.pdf)**
- *High-Speed Board Design Advisor: Pinout Definition:*  
**[www.altera.com/literature/tb/tb-094.pdf](http://www.altera.com/literature/tb/tb-094.pdf)**
- *High-Speed Board Design Advisor: High-Speed Channel Design and Layout:*  
**[www.altera.com/literature/tb/tb-095.pdf](http://www.altera.com/literature/tb/tb-095.pdf)**



101 Innovation Drive  
San Jose, CA 95134  
[www.altera.com](http://www.altera.com)

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