Technical Brief

High-Speed Board Design Advisor
Pinout Definition

Introduction

This document contains a checklist with a best practice set of step-by-step guidelines to support users to design and review their pinout definition. It should guide users to a first-time-right pinout design with the Altera® high-speed Stratix® II GX transceiver family.

This document assumes familiarity with the following tools and support collateral:

- Stratix II GX Handbook:
  www.altera.com/literature/lit-s2gx.jsp
- Stratix II GX Pinouts:
  www.altera.com/literature/lit-dp.jsp
- Quartus® II Handbook:
  www.altera.com/literature/lit-qts.jsp
- Simulation Models:
  www.altera.com/support/software/download/hspice/hsp-index.html

Altera's Stratix II GX FPGA-based development kits deliver quality-proven implementations and comprise board schematics, layout files, and board-specific guidelines documents that can be used as a starting point for user designs:

- Transceiver Signal Integrity Development Kit, Stratix II GX Edition:
  www.altera.com/products/devkits/altera/kit-signal_integrity_s2gx.html
- PCI Express Development Kit, Stratix II GX Edition:
  www.altera.com/products/devkits/altera/kit-pciexpress_s2gx.html
- Audio Video Development Kit, Stratix II GX Edition:
  www.altera.com/products/devkits/altera/kit-dsp-professional.html

Early Pinout and I/O Analysis

A common design flow requires a plan for the top-level FPGA pinout to develop the PCB schematic and layout early. Quartus II software and the Pin Planner tool allow the creation of a top-level design file, performance of I/O analysis, and validation of the I/O assignments.

Refer to Section II, "I/O and PCB Tools," of the Quartus II Handbook, Volume 2 for more information: **www.altera.com/literature/hb/qts/qts_qii5v2_02.pdf**.

- Create a system- or board-level diagram showing all standard I/O interfaces (memory and bus interfaces) and high-speed interfaces (source-synchronous LVDS or transceivers).
- Create a system clock diagram showing the systems clock concept, the reference clocks, and system clock sources and modes. The diagram should include the FPGA clock domains and input and output clock pins.
- Plan the pinout based on the placement of the other devices on the board. Pay special attention to the location of the high-speed transceivers since their pinout is fixed to edge and locations.
- Plan the pinout with the placement of the HDL design modules in mind in case of a modular or incremental design approach.

A complete pinout check can be performed using the Quartus II I/O Assignment Analysis tool even if without any or with incomplete design files. To allow I/O analysis and I/O rule checking for high-speed interfaces and phase-locked loops (PLLs), a top-level design file with HDL for these functions must be created.

- While the Pin Planner is the recommended tool in Quartus II software for creating and editing pin-related assignments and creating the top-level design file, Assignment Editor provides a spreadsheet-like interface that allows creation and changing of all pin-related assignments. Setting up the top-level design file and I/O analysis can also be performed manually.

Create/Import Megafunction

In Pin Planner, create, import, or edit megafunctions or IP MegaCore® functions using the command: "Create/Import Megafunction."

- Create all PLLs and assign clock I/Os. Internal PLL outputs can be left open or can be connected to other top-level modules.
- Create high-speed protocol IP or transceiver megafunctions and assign I/Os.
- Create source-synchronous LVDS high-speed interfaces and assign I/Os.
- Create external memory interfaces and assign I/Os.
- Assign any other external nodes to I/Os.
- If some design files are missing, create reserved pins to temporarily represent the top-level design I/O pins (requires a unique pin name and a pin location).

Set Up Top-Level Design File

In Pin Planner, set-up the top-level design file using the command: "Set Up Top-Level Design File."

- The columns in the dialog box provide information about megafunctions created in the Pin Planner, allow adjustments, and connect megafunctions together.
- This is especially useful for clock networks that typically are attached to multiple megafunctions or IP MegaCore functions.
- For any open internal nodes, the Pin Planner will assign virtual pins to the node to prevent mapping to I/O pins.

Create Top-Level Design File

In Pin Planner, create a top-level design file using the command: "Create Top-Level Design File."

- Here, the assumption is that the design files are not complete. Although I/O assignments will be checked during a full compile, with I/O assignment analysis compile times can be significantly reduced.
- The accuracy and completeness of the pin-related assignments determines the accuracy of the I/O assignment analysis.
- Make sure the following pin properties are defined:
  - Assign pin name (node name) to a pin location.
  - Assign reserved pins as placeholders for undefined pins.
  - Assign I/O standard to pin name and location.
  - Assign current strength.
  - Assign output pin load.
  - Assign toggle rate if applicable. Allows maximum frequency rule checks.
  - Use edge or bank assignment for general purpose I/Os. The Quartus II software will place the pins automatically while checking the I/O rules. Back-annotate assignments later.
  - Define the V_{CCIO} I/O bank voltage requirements for general purpose I/Os. Assign the I/Os per V_{CCIO} group and to banks.
  - Use specific locations for clock pin or high-speed I/O assignments based on the system requirements.
  - Assign Stratix II GX termination (source synchronous and transceiver I/Os).

Refer to "Understanding the I/O Assignment Analysis Report and Messages" in the Quartus II Handbook, Volume II, Chapter 5:
www.altera.com/literature/hb/qts/qts_qii52013.pdf.

- I/O Assignment Analysis will check I/O and SSN related rules.

For more information about I/O design considerations, refer to the Stratix II GX Handbook, Volume 2, Section IV, "I/O Standards" (*Keywords: I/O Termination, I/O Banks Restrictions, I/O Placement Guidelines, and DC Guidelines*):
www.altera.com/literature/hb/stx2gx/stxiigx_sii5v2_04.pdf.

Start I/O Assignment Analysis

In Pin Planner, perform I/O Assignment Analysis using the command: "Start I/O Assignment Analysis."

- Analyze the report for assignments and I/O rules violations and make changes as needed.
- Use assignments in existing project or create the rest of a new project based on the assignments.
- Get a pinout file (ASCII text file containing pin location results and other pin information) and validate the assignments.
- Display and accept fitter placements for the unassigned or partly assigned nodes by back-annotating I/O pin assignments.

Pin Definitions and Connection Guidelines

For more information about pin definitions and specifications, refer to the Stratix II GX Handbook, Volume 1, Chapter 4, "DC and Switching Characteristics" (Keywords: *Device Absolute Maximum Ratings, Device Recommended Operating Conditions, Supported I/O Standards*):
www.altera.com/literature/hb/stx2gx/stxiigx_sii51006.pdf.

Note that, depending on the device family member, not all pins and banks are available.

Supply and Reference Pins

- All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before `VCCINT`, `VCCPD`, and `VCCIO` are powered.

For more information about recommended rise times for `VCCINT`, `VCCIO`, `VCCPD` refer to the Stratix II GX Handbook, Volume 1, Chapter 4, "DC and Switching Characteristics" (Keywords: *Device Recommended Operating Conditions*)
www.altera.com/literature/hb/stx2gx/stxiigx_sii51006.pdf.

- `VCCINT` (Power)
  - 1.2V internal logic array voltage supply
  - Supplies LVDS, LVPECL, single-ended and differential HSTL and SSTL input buffers
  - Supplies top and bottom clock input differential buffers in I/O banks 3, 4, 7, and 8 (not `VCCIO`)
  - Input pins are 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V tolerant
  - Pins powered by `VCCINT`, `VCCSEL`, PORSEL, nIO_PULLUP, MSEL[3..0]
- `VCCIO[1..4,7,8]` (Power)
  - I/O supply voltage for banks 1, 2, 3, 4, 7, and 8. Each bank can support a different voltage level
  - Supplies output buffers for all I/O standards
  - Supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5V, 1.8V, 2.5V, 3.3V PCI, and 3.3V PCI-X I/O standards
  - Each I/O bank has its own `VCCIO` pins which can support a different voltage level independently. Each bank also has dedicated `VREF` pins to support the voltage-referenced standards.

For more information about I/O specifications and maximum operating conditions, refer to the Stratix II GX Handbook, Volume 1, Chapter 4, “DC and Switching Characteristics” (Keywords: *I/O Specifications, Operating Conditions*):
www.altera.com/literature/hb/stx2gx/stxiigx_sii51006.pdf.

- VCCPD (Power)
  - 3.3V pre-driver voltage supply to the output buffers (performance increase)
  - Supplies configuration pins nCONFIG, DCLK (when used as an input), nIO_Pullup, DATA[7…0], RUnLU, nCE, nWS, nRS, CS, nCS, and CLKUSR and JTAG input pins TCK, TMS, TDI, and TRST (TDO buffer is powered by VCCIO)
  - VCCPD pins must ramp up from 0V to 3.3V within 100 ms to ensure successful configuration
- VCCSEL will determine the voltage supply for certain input buffers and pins
  - nSTATUS (when used as an input), nCONFIG, CONF_DONE (when used as an input), DATA[7..0], nCE, DCLK (when used as an input), CS, nWS, nRS, nCS, CLKUSR, DEV_OE, DEV_CLRn, RUnLU, PLL_ENA
  - VCCSEL connected to GND: 3.3V/2.5V input buffer is selected, pins are powered by V_{CCPD}
  - VCCSEL connected to VCCIO of the I/O bank: 1.V8/1.5V input buffer is selected, pins are powered by VCCIO of that bank
- VREFB[1..4,7,8][4..0] (Power)

Note that VREFB is referred to as VREF in the Stratix II GX handbook.

  - Input reference voltage for each I/O bank (used, if a bank is used for a voltage-referenced I/O standard)
  - All of the VREFB pins within a bank are shorted together, that is, each bank can support only one VREFB voltage level.
  - If VREFB pins are not used, designers should connect them to either the VCCIO in the bank in which the pin resides or GND. They cannot be used as generic I/Os.
  - Banks 9 through 12 are enhanced PLL external clock output banks. These PLL banks utilize the adjacent VREFB group when voltage-referenced standards are implemented.

For more information about VREFB specification for the differential I/O standards, refer to the Stratix II GX Handbook, Volume 2, Section IV, “I/O Standards” (Keywords: *I/O Standards and Voltage Levels*):
www.altera.com/literature/hb/stx2gx/stxiigx_sii5v2_04.pdf.

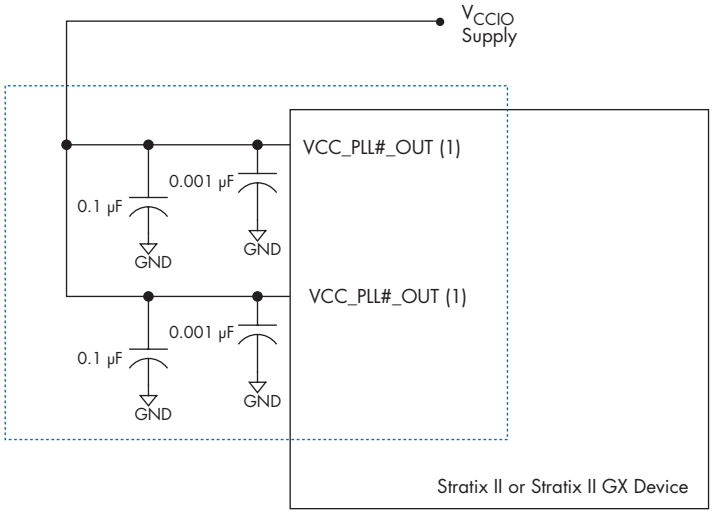
  - Typically, the VREFB voltages are derived from that bank's VCCIO source using a simple voltage divider to achieve half the voltage. Other options include reference outputs, such as memory termination voltage regulators. Refer to the Stratix II GX development kits for examples.

For more information about VREFB pin placement guidelines, refer to the Stratix II GX Handbook, Volume 2, Section IV, “I/O Standards” (Keywords: *VREF Pin Placement Restrictions*):
www.altera.com/literature/hb/stx2gx/stxiigx_sii5v2_04.pdf.

- VCC_PLL5_OUT, VCC_PLL6_OUT, VCC_PLL11_OUT, VCC_PLL12_OUT
  - I/O supply voltage (VCCIO) for Enhanced PLL5,6,11,12 clock outputs PLL[5,6,11,12]_OUT[1..0]p, PLL[5,6,11,12]_OUT[1..0]n, PLL[5,6,11,12]_FBp/OUT2p, and PLL[5,6,11,12]_FBn/OUT2n
  - Connected to the voltage level of the target device which PLL 5,6,11,12 is driving
  - Less susceptible to noise since it is powered by separate power pins
  - Reduced overall jitter of the output clock by providing improved isolation from switching I/O pins
  - I/O pins in banks 5, 6, 11, and 12 are powered by these pins
  - The VCC_PLL_OUT pins can by powered by 3.3V, 2.5V, 1.8V, or 1.5V

- The PLL clock output/feedback differential buffers are powered by VCC_PLL_OUT. For 3.3V LVDS and LVPECL differential clock output/feedback operation, connect VCC_PLL_OUT to 3.3V.
- Filter each isolated power pin with a decoupling circuit. Decouple the isolated power pins with parallel combination of 0.1Ω and 0.001Ω ceramic capacitors located as close as possible to the Stratix II GX device.

Figure 1. Decoupling Scheme for External Enhanced PLL Clock Output Power Supplies

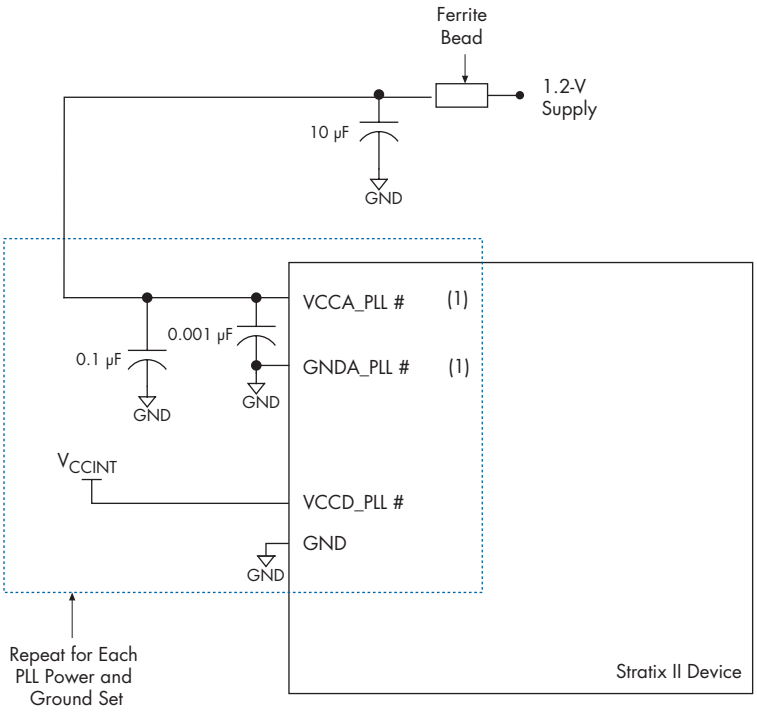


Note to Figure 1:
(1) Applies only to enhanced PLLs 5, 6, 11, and 12.

- Guidelines to improve jitter for multiple clock outputs and frequencies:
  - Use phase shift to ensure edges are not coincident on all the clock outputs.
  - Use phase shift to skew clock edges with respect to each other for best jitter performance.
  - If drive multiple clocks of different frequencies and phase shifts or isolate banks are not possible, then control the drive capability on the lower-frequency clock. Reducing how much current the output buffer has to supply can reduce the noise. Minimize capacitive load on the slower frequency output and configure the output buffer to lower current strength. The higher-frequency output should have an improved performance, but this may degrade the performance of the lower frequency clock output.
- VCCA_PLL[1,2,5..8,11,12]
  - 1.2V analog power for PLLs[1,2,5..8,11,12]
  - Connect these pins to 1.2V, even if the PLL is not used. Use an isolated linear supply. Power on the PLLs operating at the same frequency should be decoupled.

For more information about PLL board layout guidelines, refer to the Stratix II GX Handbook, Volume 2, Section II, “Clock Management” (Keywords: *VCCA and GNDA*): **www.altera.com/literature/hb/stx2gx/stxiigx_sii5v2_02.pdf**.

Figure 2. Decoupling Scheme for PLLs Power Supplies



Note to Figure 2:
(1) Applies to PLLs 1 through 12.

- `GNDA_PLL[1,2,5..8,11,12]`
  - Analog ground for PLLs[1,2,5..8,11,12].
  - Connect this pin to the `GND` plane on the board. Connect the `GNDA_PLL` pins directly to the same ground plane as the device's digital ground. Avoid excessive noise levels on this plane.
- `VCCD_PLL[1,2,5..8,11,12]`
  - 1.2V digital power for PLLs[1,2,5..8,11,12]. The designer must connect these pins to 1.2V, even if the PLL is not used. Power on the PLLs operating at the same frequency should be decoupled.
  - The `VCCD` pin supplies the power for the digital circuitry in the PLL. Connect these `VCCD` pins to the quietest 1.2V digital supply on the board. In most systems, this is `VCCINT`. Connect the PLL `GND` pins directly to the same ground plane as the device's digital ground.
- `RUP4, RDN4/RUP7, RDN7` (I/O, Input)
  - Reference pin for banks 3 and 4 or 7 and 8 for on-chip termination (OCT) calibration.
  - If not required, these pins can be used as a regular I/O pin.
  - If not used at all, connect pins to `VCCIO/GND: RUP4/7 = VCCIO4/7, RDN4/7 = GND`.

For more information about OCT, refer to the Stratix II GX Handbook (Keywords: *On-Chip Termination, Calibration*):
www.altera.com/literature/lit-s2gx.jsp.

- Calibration circuits rely on the external pull-up reference resistor (RUP) and pull-down reference resistor (RDN) to achieve accurate on-chip series and parallel termination.
- The two banks—3 and 4 or 7 and 8—share the same calibration circuitry, so they must have the same V_{CCIO} voltage if both banks enable on-chip series or parallel termination with calibration.

- If banks 3 and 4 have different V_{CCIO} voltages, only bank 4 can enable on-chip series or parallel termination with calibration because the RUP and RDN pins are located in bank 4. Bank 3 still can use on-chip series or parallel termination, but without calibration. The same rule applies to banks 7 and 8.
- When used for calibration, the RUP pins are connected to VCCIO through an external 25Ω or 50Ω resistor for an on-chip series termination value of 25Ω or 50Ω, respectively. The RDN pin is connected to GND through an external 25Ω or 50Ω resistor for an on-chip series termination value of 25Ω or 50Ω, respectively. For on-chip parallel termination, the RUP pin is connected to VCCIO through an external 50Ω resistor, and RDN is connected to GND through an external 50Ω resistor.

❒ TEMPDIODEp, TEMPDIODEn (Input)

- This pin is used in conjunction with the temperature-sensing diode (bias-high input) inside the Stratix II GX device.
- If the temperature-sensing diode is not used, then connect this pin to GND.

For more information about the temperature sensing diode, refer to the Stratix II GX Handbook (Keywords: *Temperature Sensing Diode*):
www.altera.com/literature/lit-s2gx.jsp.

Dedicated Configuration/JTAG Pins

❒ nIO_PULLUP, VCCSEL, DCLK, MSEL[3..0], nCE, nCONFIG, CONF_DONE, nCEO, nSTATUS

For more information about the Stratix II GX configuration pin summary, refer to the Stratix II GX Handbook (Keywords: *Configuration Pin Summary*):
www.altera.com/literature/lit-s2gx.jsp.
Refer to the Stratix II Handbook, Volume 2, Section V, "Configuration and Remote System Upgrades," for more information:
www.altera.com/literature/hb/stx2/stx2_sii5v2_05.pdf.
Refer to the Stratix II GX pinouts for more information:
www.altera.com/literature/lit-dp.jsp.

Optional/Dual-Purpose Configuration Pins

❒ PORSEL, nCSO, ASDO, CRC_ERROR, DEV_CLRn, DEV_OE, DATA0, DATA[6..1], DATA7, INIT_DONE, nCS, CS, nRS, nWS, CLKUSR, RDYnBSY, PGM[2..0], RUnLU, TCK, TMS, TDI, TDO, TRST

Refer to the Stratix II Handbook, Volume 2, Section V, "Configuration and Remote System Upgrades," for more information:
www.altera.com/literature/hb/stx2/stx2_sii5v2_05.pdf.

Clock and PLL Pins

- Dedicated clock and PLL input pins CLK[1,3], CLK[2,0], and CLK[4-7,12-15]

Table 1. Clock and PLL Input Pin Definition

Clock Input Pin	Pin Description	When Pin Unused
CLK[1,3]p	• Single-ended clock inputs • Differential (p) clock inputs • User inputs	Connect to VCCIO where the pin resides
CLK[1,3]n	• Differential (n) clock inputs • User inputs	Connect to GND
CLK[2,0]p/DIFFIO_RX_C[1,0]p	• Single-ended clock inputs • Differential (p) clock inputs • User I/Os • Differential (p) receiver inputs	Connect to GND
CLK[2,0]n/DIFFIO_RX_C[1,0]n	• Single-ended clock input • Differential (n) clock input • User I/O • Differential (n) receiver inputs	Connect to GND
CLK[4-7,12-15]p	• Single-ended clock inputs • Differential (p) clock inputs • User I/Os	Connect to GND
CLK[4-7,12-15]n	• Single-ended clock inputs • Differential (n) clock inputs • User I/Os	Connect to GND
CLK[11..8]	Not available in Stratix II GX devices	N/A
FPLL[8..7]CLKp	• Single-ended clock inputs • Differential (p) clock inputs • User inputs	Connect to VCCIO where the pin resides
FPLL[8..7]CLKn	• Single-ended clock inputs • Differential (p) clock inputs • User inputs	Connect to GND

- Clock pins CLK1 and CLK3 do not support differential on-chip termination.
- Clock pins CLK0 and CLK2 do support differential on-chip termination.
- Clock pins CLK[4..7, 12..15] in the top and bottom banks do not support differential on-chip termination.
- FPLL[7..8]CLK do not support differential on-chip termination.
- The clock input pins CLK[15..0] are also used for high fan-out control signals, such as asynchronous clears, presets, clock enables, or protocol signals such as TRDY and IRDY for PCI through global or regional clock networks.

For more information on clock source for PLLs (Keyword: *Stratix II GX Device PLLs and PLL Clock Pin Drivers*), clock input capacitance (Keyword: *Pin Capacitance*), and global and regional clocking (Keyword: *Clocking*), refer to the Stratix II GX Handbook: **www.altera.com/literature/lit-s2gx.jsp**.

- PLL_ENA (Input)
  - Dedicated input pin that drives the optional PLL_ENA port of all or a set of PLLs
  - If a PLL uses the pllena port, drive the PLL_ENA pin low to reset all PLLs including the counters to their default state.
  - If VCCSEL = 0, then drive the PLL_ENA with a 3.3V/2.5V signal to enable the PLLs. If VCCSEL = 1, connect PLL_ENA to 1.8V/1.5V to enable the PLL.
- Dedicated clock and PLL output pins

Table 2. Clock and PLL Output Pin Definition

Clock Output Pin	Pin Description	When Pin Unused
PLL5_OUT[1,0]p (from PLL5)	• Single-ended clock outputs • Differential (p) clock outputs	Can be left floating
PLL5_OUT[1,0]n (from PLL5)	• Single-ended clock outputs • Differential (n) clock outputs	Can be left floating
PLL6_OUT[1,0]p (from PLL6)	• Single-ended clock outputs • Differential (p) clock outputs	Can be left floating
PLL6_OUT[1,0]n (from PLL6)	• Single-ended clock outputs • Differential (n) clock outputs	Can be left floating
PLL11_OUT[1,0]p (from PLL 11)	• Single-ended clock outputs • Differential (p) clock outputs	Can be left floating
PLL11_OUT[1,0]n (from PLL 11)	• Single-ended clock outputs • Differential (n) clock outputs	Can be left floating
PLL12_OUT[1,0]p (from PLL 12)	• Single-ended clock outputs • Differential (p) clock outputs	Can be left floating
PLL12_OUT[1,0]n (from PLL 12)	• Single-ended clock outputs • Differential (n) clock outputs	Can be left floating
PLL[6..5]_FBp/OUT2p (from/to PLLs 5 or 6)	• Single-ended or differential (p) clock outputs • Single-ended or differential (p) clock feedback input • User I/Os	Connect to GND
PLL[6..5]_FBn/OUT2n (from/to PLLs 5 or 6)	• Single-ended or differential (p) clock outputs • Single-ended or differential (p) clock feedback input • User I/Os	Connect to GND
PLL[12..11]_FBp/OUT2p (from/to PLLs 11 or 12)	• Single-ended or differential (p) clock outputs • Single-ended or differential (p) clock feedback input • User I/Os	Connect to GND
PLL[12..11]_FBp/OUT2n (from/to PLLs 11 or 12)	• Single-ended or differential (p) clock outputs • Single-ended or differential (p) clock feedback input • User I/Os	Connect to GND

Dual-Purpose Differential and External Memory Interface Pins

- Dual-purpose differential receiver channels DIFFIO_RX[76..1]p, DIFFIO_RX[76..1]n
- Dual-purpose differential transmitter channels DIFFIO_TX[77..0]p, DIFFIO_TX[77..0]n
- Optional data strobe signal for use in external memory interfacing DQS[17..0][T,B], DQSn[17..0][T,B]
- Optional data signal for use in external memory interfacing DQ[17..0][T,B][3..0]
- Optional data valid signal for use in external memory interfacing DQVLD[8..0][T,B]

For more information about external memory interfaces, refer to "Further Information" and the Stratix II GX Pinouts:
www.altera.com/literature/lit-dp.jsp.
Refer to the Stratix II GX Handbook for more information:
www.altera.com/literature/lit-s2gx.jsp.

Transceiver (I/O Banks) Pins

For more information about the Stratix II GX transceiver block absolute maximum ratings, refer to the Stratix II GX Handbook (Keywords: *Transceiver Block Absolute Maximum Ratings*):
www.altera.com/literature/lit-s2gx.jsp.

- VCCP
  - Transceiver block (PCS) power supply of banks [17..13] (1.2V)
  - Connect VCCP to an isolated 1.2V linear regulator.
  - These pins need to be isolated from noisy digital voltage planes.

- VCCR
  - Transceiver block receiver analog power supply of banks [17..13] (1.2V)
  - Connect VCCR to a 1.2V linear regulator.
  - These pins may be tied to the same 1.2V plane as VCCT_B[] and/or VCCL_B[].
- VCCT_B[17..13]
  - Transceiver block transmitter analog power supply of banks [17..13] (1.2V)
  - Connect VCCT_B[] to a 1.2V linear regulator.
  - These pins may be tied to the same 1.2V plane as VCCR and/or VCCL_B[].
- VCCA
  - Transceiver block analog power supply of banks [17..13] (3.3V)
  - Connect VCCA to a 3.3V linear regulator.
- VCCH_B[17..13]
  - Transceiver block transmitter driver analog power of banks [17..13]. This power is connected to 1.2V or 1.5V.
  - Supply 1.2V for 3.125-Gbps maximum data rate, and for lower power. 1.5V can be used for all data rates.
  - Connect VCCH_B[] to a 1.2V or 1.5V linear regulator.
- VCCL_B[17..13]
  - Transceiver block VCO analog power and general transceiver clock circuitry of banks [17..13] (1.2V)
  - Connect VCCL_B[] to a 1.2V linear regulator.
  - These pins may be tied to the same 1.2V plane as VCCT_B[] and/or VCCR.
- GXB_RX[19..0]p, GXB_RX[19..0]n
  - High-speed differential (p/n) receiver channels
  - Connect the unused RXp pins to the VCCR 1.2V plane through a 10KΩ resistor or tie all unused pins together through a single 10KΩ resistor.
  - Connect the unused RXn pins to GND through a 10KΩ resistor or tie all unused pins together through a single 10KΩ resistor.
  - Ensure that the trace from the pins to the resistor(s) are as short as possible.
- GXB_TX[19..0]p, GXB_TX[19..0]n
  - High-speed differential (p/n) transmitter channel
  - Connect the unused TXp pins to the VCCT_B[] or VCCR (if tied together with VCCT_B[]) 1.2V plane through a 10KΩ resistor or tie all unused pins together through a single 10KΩ resistor.
  - Connect the unused TXn pins to GND through a 10KΩ resistor or tie all unused pins together through a single 10KΩ resistor.
  - Ensure that the trace from the pins to the resistor(s) are as short as possible.
- REFCLK[0,1]_B[17..13]p, REFCLK[0,1]_B[17..13]n
  - High-speed differential I/O (p/n) reference clock
  - Connect the unused REFCLKp pins to the VCCT_B[] or VCCR (if tied together with VCCT_B[]) 1.2V plane through a 10KΩ resistor or tie all unused pins together through a single 10KΩ resistor.
  - Connect the unused REFCLKn pins to GND through a 10KΩ resistor or tie all unused pins together through a single 10KΩ resistor.
  - Ensure that the trace from the pins to the resistor(s) are as short as possible.
- RREFB[17..13]
  - Reference resistor for transceiver block banks [17..13]
  - These pins should be connected to a 2.00KΩ 1% resistor to GND.
  - The DC signal on this pin must be as clean as possible. Ensure that no noise is coupled to this pin. Therefore, the trace from this pin to the resistor needs to be routed in a way to avoid coupling from any aggressor signals.

Further Information

- *High-Speed Board Design Advisor: Power Distribution Network*:
  www.altera.com/literature/tb/tb-092.pdf
- *High-Speed Board Design Advisor: Thermal Management*:
  www.altera.com/literature/tb/tb-093.pdf
- *High-Speed Board Design Advisor: High-Speed Channel Design and Layout*:
  www.altera.com/literature/tb/tb-095.pdf
- *High-Speed Board Design Advisor: Hardware Integration, Test, and Debug*:
  www.altera.com/literature/tb/tb-096.pdf
- AN 411: Understanding PLL Timing for Stratix II Devices
  www.altera.com/literature/an/an411.pdf
  - Design Example 1 (279 KB)
    www.altera.com/literature/an/Example1.zip
  - Design Example 2 (232 KB)
    www.altera.com/literature/an/Example2.zip
- *AN 449: Design Guidelines for Implementing External Memory Interfaces in Stratix II and Stratix II GX Devices*
  www.altera.com/literature/an/an449.pdf
- *AN 408: DDR2 Memory Interface Termination, Drive Strength and Loading Design Guidelines*
  www.altera.com/literature/an/an408.pdf
  - Simulation Example (2 KB)
    www.altera.com/literature/an/an408_example.zip
- *AN 392: Multiple DDR and DDR2 SDRAM Controllers On One Device*
  www.altera.com/literature/an/an392.pdf
- *AN 328: Interfacing DDR2 SDRAM with Stratix II Devices*
  www.altera.com/literature/an/an328.pdf
- *AN 327: Interfacing DDR SDRAM with Stratix II Devices*
  www.altera.com/literature/an/an327.pdf
- *AN 326: Interfacing QDRII and QDRII+ SRAM with Stratix II, Stratix, and Stratix GX Devices*
  www.altera.com/literature/an/an326.pdf
- *AN 325: Interfacing RLDRAM II with Stratix II, Stratix, and Stratix GX Devices*
  www.altera.com/literature/an/an325.pdf
- *Calibration Techniques for High-Bandwidth Source-Synchronous Interfaces* (presented at DesignCon 2007)
  www.altera.com/literature/cp/cp-01024.pdf

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