Technical Brief

External Memory Interface Options for Stratix II Devices

Introduction

This document is intended to help users select the appropriate external memory interface solution for Altera® Stratix® II, Stratix II GX, and HardCopy® II devices when implementing a DDR or DDR2 SDRAM interface.

Fundamentally, there are two options:

- The new altmemphy megafunction (with Altera's high-performance DDR/DDR2 SDRAM controller or user controllers)
- Legacy integrated static data path and controller (e.g., DDR and DDR2 SDRAM Controller MegaCore® functions)

Before discussing these options in full, Table 1 briefly highlights support for the new altmemphy megafunction and the legacy MegaCore function in other Altera FPGA families.

Table 1. Other FPGA Families

Device Family	Altmemphy Support
Cyclone II FPGAs	Legacy core only; Cyclone II FPGAs do not support altmemphy because it does not have a reconfigurable phase-locked loop (PLL).
Cyclone III FPGAs	Cyclone III FPGAs do not support the legacy core because it does not use DQS delay elements.
Stratix III FPGAs	All new Stratix III designs are required to use the new altmemphy megafunction with the high-performance controller (or custom controller). Migration from Stratix II FPGAs is possible but not recommended (see migration section).

Altmemphy + Controller vs. Legacy Static-Timing Combined Data Path and Controller IP

Legacy cores provide an integrated data path and controller solution using static timing analysis, but are limited to 267-MHz (533-Mbps) operation.

The new altmemphy megafunction takes a split PHY and controller approach. The PHY automatically calibrates, then tracks voltage and temperature variations, allowing operation up to 333 MHz (667 Mbps) in Stratix II devices (400 MHz in Stratix III devices). A well-defined controller interface allows specialist controller development. Altera recommends that all new Stratix II designs use the new autocalibrated PHY via the altmemphy megafunction with the high-performance controller (or a separate custom controller) where possible.

Benefits of New Autocalibrated PHY

The autocalibrated PHY is significantly more powerful than the legacy memory interface controller MegaCore functions. The autocalibrated PHY is able to compensate for process variations in the FPGA and the external memory via calibration at startup. Further, the autocalibrated PHY is capable of tracking and eliminating voltage and temperature variations in the FPGA, maintaining the maximum setup and hold margin across process, voltage, and temperature. For interfaces operating above 200 MHz (400 Mbps), the autocalibrated PHY uses fewer PLLs than the legacy solution.

Above 200 MHz (Fedback PLL Designs)

Though the legacy core is capable of supporting 267-MHz (533-Mbps) operation, Altera strongly recommends using altmemphy. To get performance greater than 200 MHz with a legacy core, the DDR2 SDRAM interface must use the fedback-PLL mode, a 2-PLL solution requiring manual set-up and compile iterations. The new autocalibrated PHY frees up one PLL and automatically selects the resynchronization and postamble phases.

Moving From Old to New

The external memory interface (DDR/DDR2 SDRAM) pins do not change between solutions. There are changes between the old and new solution for internal pins. Of particular note is that currently altmemphy is available only in the half-rate solution (see below for an explanation of "half rate"). In practice, this means the use-side read and write bus are twice as wide as the legacy core. The full-rate solution will be available in Quartus® II software version 7.1. Moving to the new autocalibrated PHY will require some changes to existing system logic, but the benefits outweigh the required minor changes to system level logic.

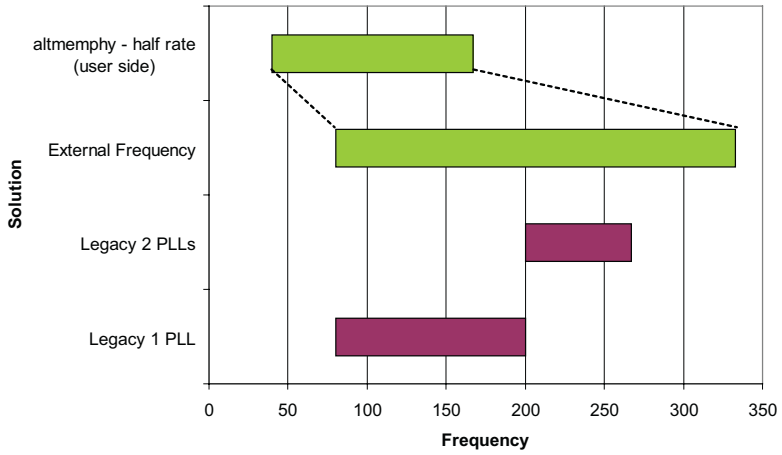
Migration

Migrating an existing memory interface design from Stratix II to Stratix III devices is possible. However, Altera strongly recommends upgrading. If for any reason you cannot use the new autocalibrated PHY and wish to migrate an existing design, please contact your local sales representative for more information. If you are using your own controller, you can upgrade the legacy data path to the autocalibrated PHY using the altmemphy megafunction.

Frequency of Operation

Figure 1 shows the operational frequency for both the new altmemphy (external and user side) and legacy core solutions.

Figure 1. Stratix II Solutions vs. Operational Frequency



Half Rate vs. Full Rate

Figure 2 shows the differences in the datapath width and the frequency at which the data is handled between full-rate and half-rate controllers. The example shows a 200-MHz (400-Mbps) DDR interface.

Figure 2. Full-Rate and Half-Rate Controller Description

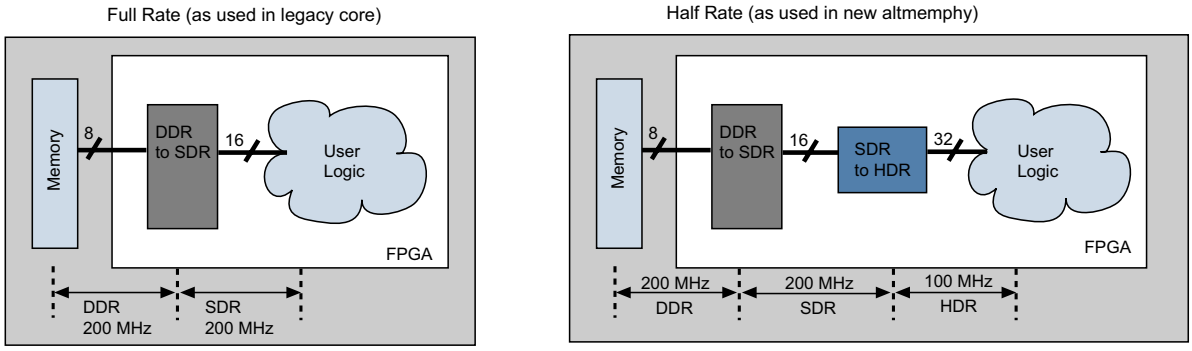


Table 2 highlights the definitions of half and full rate.

Table 2. What Do Half Rate and Full Rate Mean?

Rate	Definition
Double Data Rate (DDR)	Prior to data capture, data is said to be DDR—occurring on both clock edges.
Single Data Rate (SDR)	After data capture, the data is SDR—occurring on the positive edge only (but on the same frequency as DDR).
Half Data Rate (HDR)	HDR is data on the single positive edge of clock. It runs at half the frequency but twice the data width of SDR.
Full Rate	Refers to the DDR to SDR transition when the data width is doubled but the frequency remains constant at the full (external DDR) rate.

Table 3 shows some of the important differences between the legacy, half rate, and full rate solutions.

Table 3. Comparison of Solutions

	Legacy	Half Rate	Full Rate
IP Available	Quartus II software v.6.1	Quartus II software v.6.1	Quartus II software v.7.1
	Now	Now	May 2007
Internal Logic Frequency	Same as DDRx interface	Half DDRx interface	Same as DDRx interface
Maximum Frequency	267 MHz	333 MHz external 167 MHz internal	267 MHz (Stratix II FPGAs)
Data bit to DQ Pin Ratio	2:1	4:1	2:1
Number of PLLs for Interface >200 MHz	2	1	1
Timing Methodology	Static	Dynamic	Dynamic
Set Up	Manual	Automatic	Automatic
PVT Tracking	No	Yes	Yes

Half rate simplifies internal design by only requiring the logic to be at half the external memory interface frequency. However, the latency of the half-rate solution is greater than that of the legacy and full-rate solutions. Half rate also requires an internal data bus twice that of the legacy or full-rate internal data busses.

An example of when to apply the half-rate solution is when the pins can toggle at a greater rate than the internal logic design. Imagine a Nios® II processor running at 32 bits at 100 MHz. Using full-rate or the legacy solution, the DDR interface would have to run at 100 MHz with a data width of 16 bits. With the half-rate solution, the DDR interface could run 8 bits wide at 200 MHz, maintaining the same bandwidth as above and still feeding 16 bits at 100 MHz to the Nios II processor.

Alternatively, the width of the external DQ memory interface could be maintained, in this example, at 16 bits wide, and then the internal width would become 64 bits at 100 MHz (for the same number of DQ pins as the full-rate solution). That is, the half-rate solution allows a doubling of bandwidth for a given number of external pins when the internal logic is frequency limited.

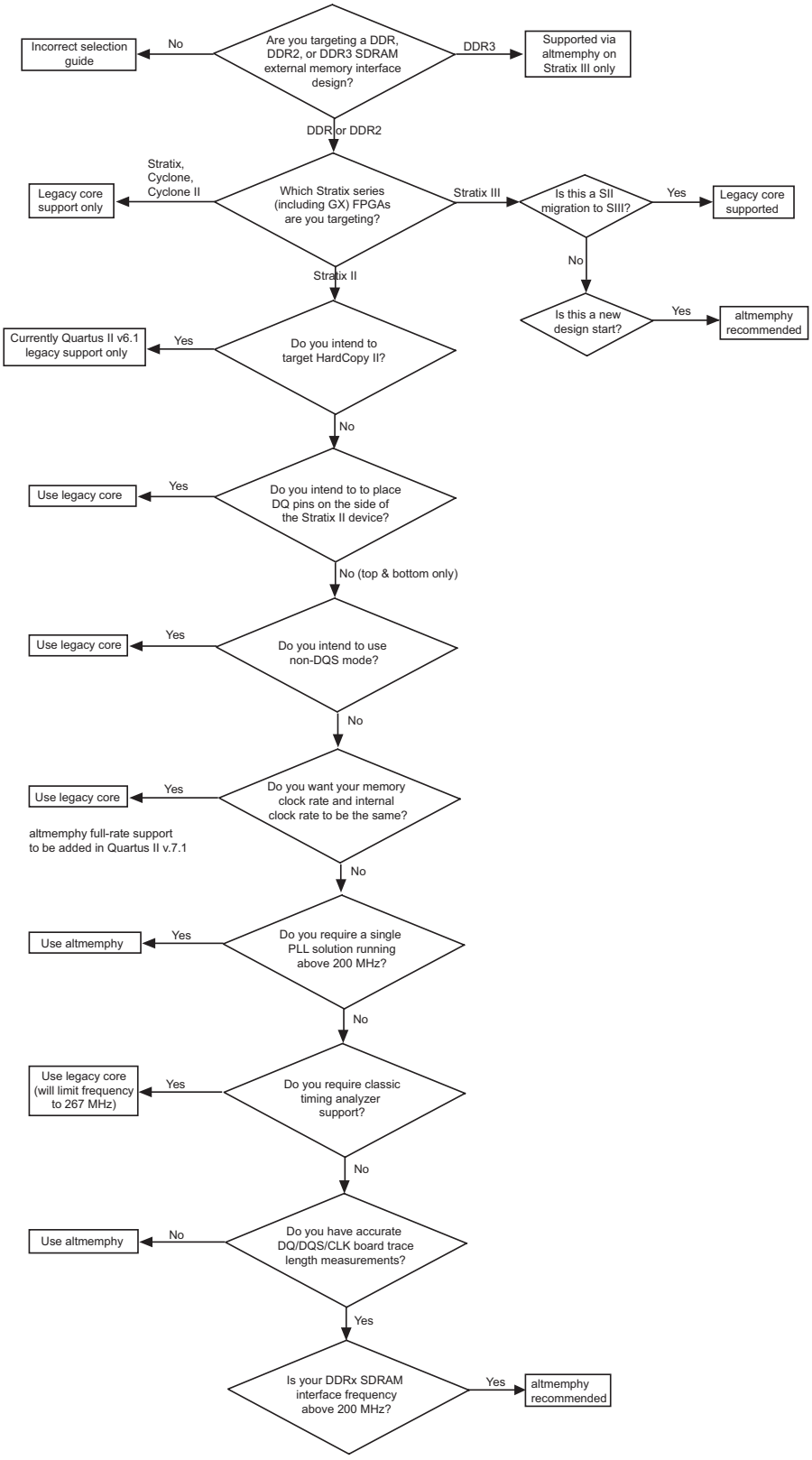
HardCopy II Devices

Altmemphy in Quartus II software version 6.1 does not support HardCopy II devices. Altmemphy in HardCopy II devices will be supported starting with version 7.1 of the Quartus II software.

Selection Flow Chart

Figure 3 can be used as a decision tree when deciding which solution is most appropriate for a design.

Figure 3. Selection Flow Chart



Conclusion

Stratix II series devices bring a range of external memory interface solution for both low-latency and high-frequency performance applications. This technical brief has shown the trade-offs between the various options to help guide in the selection of the most appropriate solution.

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