

Stratix II Military Temperature Range Support

Introduction

As part of Altera's initiative to provide enhanced commercial off-the-shelf (COTS) devices for military applications, the temperature range for the Stratix® II device family has been extended to enable operation across the military temperature range (-55°C to 125°C). This allows military programs to benefit from new technology and economies of scale by using commercially available Stratix II FPGAs.

Stratix II FPGAs are extremely robust devices capable of operating across a wide temperature range with excellent reliability characteristics. This technical brief will describe Altera's support for Stratix II military temperature range operation with appropriate background information. It will also explain how to utilize Stratix II devices across military temperature range operation and any limitations in operation that affect the datasheet specifications.

Military Temperature Support

Military temperature operation requires additional timing margin over industrial temperature operation to compensate for the potentially increased variation of f_{MAX} across temperature. With Altera® devices, increased timing margin is achieved by compiling the design using an industrial I4 part and set the temperature range to -55°C to 125°C in the Quartus® II software. Quartus II software provides separate timing models for 125°C at slow corner and -55°C at fast corner. This technique can be used to increase the timing margin of an industrial device to meet the constraints of military temperature range operation in Stratix II devices (shown in Table 1).

Table 1. Stratix II Military Temperature Device Support

Stratix II Device	Military Temp Support	Package	Type
EP2S15	Yes	All	Industrial -4 devices (I4)
EP2S30	Yes	All	Industrial -4 devices (I4)
EP2S60	Yes	All	Industrial -4 devices (I4)
EP2S90	Yes	All	Industrial -4 devices (I4)
EP2S130	No		
EP2S180	No		

Characterization results show that Stratix II operation across the military temperature range is bounded by the military temperature range of industrial I4 speed operation of the datasheet specifications and any relevant errata except where noted below.

- Worst-case standby power at +125°C is 1.8X of the worst-case standby power at +100°C. Therefore, careful power analysis and thermal management is required. For military temperature static power, the Stratix II PowerPlay Early Power Estimator or PowerPlay Power Analyzer version 6.1 or later should be used.
- Non-calibrated on-chip termination (OCT) will be bounded to:
 - +/-40% for series resistance
 - +/-50% for 1.2V series resistance
- Hot-socketing DC limit is raised to 350 μ A
- I/O F_{MAX} is 15% less than C5 specifications for all I/O standards
- LVDS I/O 2.5V minimum V_{OCM} is 1.1V, minimum V_{OD} is 240mV

Stratix II PLL Settings

Beginning with version 7.2, Quartus II software fully supports military temperature range operation for PLLs. The compiler will implement PLL settings that follow certain restrictions to ensure the PLL will operate correctly across the military temperature range.

The altpll MegaWizard® also supports military temperature range operation. While creating a custom altpll megafunction, indicate military temperature range operation by checking the “Use military temperature range devices only” checkbox on page 3.

As a reference, the following are the PLL setting restrictions for military temperature range operation:

- Ensure the M counter is between 3 and 19, and:
 - For M = 3 or 4, I_{CP} must be $\geq 36 \mu A$
 - For M = 5 or 6, I_{CP} must be $\geq 52 \mu A$
 - For M = 7, I_{CP} must be $\geq 57 \mu A$
 - For M = 8 or 9, I_{CP} must be $\geq 72 \mu A$
 - For M = 10, I_{CP} must be $\geq 77 \mu A$
 - For M = 11 or 12, I_{CP} must be $\geq 92 \mu A$
 - For M = 13 or 14, I_{CP} must be $\geq 110 \mu A$
 - For M = 15, I_{CP} must be $\geq 114 \mu A$
 - For M = 16, I_{CP} must be $\geq 127 \mu A$
 - For M = 17, I_{CP} must be $\geq 131 \mu A$
 - For M = 18 or 19, I_{CP} must be $\geq 144 \mu A$
- Ensure the phase frequency detector (PFD) input frequency is greater than or equal to 25 MHz and greater than eight times (8X) the bandwidth of the PLL.
 - PFD input frequency is defined as PLL input frequency (f_{IN}) divided by the N counter.
 - If the PFD does not meet the 8X rule, either the f_{IN} to the PLL must be increased or the N counter must be decreased.

In general, these PLL restrictions will reduce the input/output frequency combinations available (due to limited M counter choices), and reduce the PLL bandwidth range (due to limited charge pump current choices). Lower bandwidths will be more difficult to achieve.

Conclusion

These guidelines have been determined through additional characterization of Stratix II devices on samples of production silicon across military temperature ranges (125°C and -55°C), while the characterizations demonstrate correct operation across military temperatures by design. Production testing of industrial grade devices is performed at 100°C.

Further Information

- Detailed characterization reports are available to qualified customers. Contact an Altera sales representative for access to these reports:
www.altera.com/corporate/contact/con-index.html
- Stratix II PowerPlay Early Power Estimator:
www.altera.com/support/devices/estimator/pow-powerplay.html



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