This reference design is an Intel® FPGA targeted OpenCL™ implementation of a 2D parabolic partial differential equation (PDE) solver based on a modified Craig-Sneyd Alternate Direction Implicit (ADI) scheme intended for acceleration of financial applications such as option pricing.

The accelerator is a numerical solver for 2D parabolic partial differential equation, a type of PDE commonly found in financial applications where the equation to be solved has the general form of:

$$\frac{\partial V}{\partial t} = a \frac{\partial^2 V}{\partial x^2} + b \frac{\partial V}{\partial x} + c \frac{\partial^2 V}{\partial y^2} + d \frac{\partial V}{\partial y} + e \frac{\partial^2 V}{\partial x \partial y} - rV$$

where coefficient $r$ is a function of $t$, and coefficients $a$, $b$, $c$, $d$, and $e$ can be dependent on $x$, $y$, and $t$. To reduce the amount of data required to express and store coefficients $a$, $b$, $c$, $d$, and $e$, instead of allowing them to be arbitrary functions (of $x$, $y$, and $t$), they are required to be separable and take the following form:

$$\omega = \omega_t(t) + \omega_x(x, t) \cdot \omega_y(y, t)$$

For the current implementation, the $x$ and $y$ dimensions are discretized into a finite difference grid of fixed size $NX \times NY$, where $NX$ is 100 and $NY$ is 50. The $t$ dimension is discretized into a maximum of 103 steps. Variable step sizes are supported across all dimensions.

Authors

Jimmy Choi
SoC Design Engineer
Intel Corporation

Figure 1. Illustration of the 102 step PDE Solver for FX Rate
Built to Scale with Intel FPGA Financial Libraries

Intel will be delivering over 250 library functions in 2019 enabling you to develop your own financial algorithms targeted for your implementation. This library includes a vast array of functions including statistics, linear algebra, and math primitives. To enable easy development of your algorithms with the financial library functions we have built a platform with a full software stack to enable you to accelerate and orchestrate on FPGAs through OpenCL™. The PDE solver reference design leverages the orchestration capabilities of the software stack to deploy the PDE solver on four Intel Arria® 10 FPGA programmable acceleration cards on a single server.

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