Quartus II Software Version 9.1 SP2 Release Notes

April 2010 RN-01054-1.0

This document provides late-breaking information about the following areas of the Altera® Quartus®II software version 9.1 SP2:

For information about disk space and system requirements, refer to the **readme.txt** file in your **altera/<*version number*>/quartus** directory. For information about device support in this version of the Quartus II software, along with the latest information about timing and power models, refer to the *Quartus II Device Support Release Notes*. For the latest information about the MegaCore® IP Library, refer to the *MegaCore IP Library Release Notes and Errata*. Both documents are available on the Altera website at http://www.altera.com/literature/lit-rn.jsp.

New Features & Enhancements

The Quartus II software version 9.1 includes the following new features and enhancements:

- The Rapid Recompile option, which reduces compilation time and improves timing preservation when making small design changes. You can use the Rapid Recompile option in place of or together with creating design partitions to preserve placement and routing results from a previous compilation.
- You can use non-rectangular LogicLock™ regions to create more compact and efficient floorplans.
- Avalon® Verification IP components in SOPC Builder allow you to simulate the behavior of IP created for SOPC Builder systems and to monitor Avalon interface traffic. You can also perform Avalon Memory Map or Avalon Streaming Protocol assertion checking.
- The Quartus II software version 9.1 provides VHDL 2008 initial support.
- The IP library includes improved DDR2, DDR3, QDR II+, and RLDRAM II memory controllers.

- The Pin Advisor has been enhanced to include information on how to use the Quartus II software to generate more accurate and less pessimistic Simultaneous Switching Noise (SSN) results.
- The Quartus II software version 9.1 supports the following new megafunctions:
  - altotp megafunction
  - altfp_matrix_inv megafunction

The Quartus II software version 9.1 SP2 adds support for the following devices:

- Initial information support for these Cyclone® IV GX devices: EP4CGX30, EP4CGX50, EP4CGX75, EP4CGX110, EP4CGX150
- Advance support for these Cyclone III LS devices: EP3CLS70, EP3CLS100
- Advance support for these Cyclone IV GX devices: EP4CGX22, EP4CGX30
- Advance support for these Stratix® IV devices: EP4S40, EP4S100, EP4SE360, EP4SE820, EP4SGX70, EP4SGX110, EP4SGX290, EP4SGX360, EP4SGX530
- Full support for these Arria® II GX devices: EP2AGX95, EP2AGX125, EP2AGX190, EP2AGX260
- Full support for these Cyclone IV E devices: EP4CE6, EP4CE10, EP4CE15, EP4CE22, EP4CE30, EP4CE40, EP4CE55, EP4CE75, EP4CE115
- Full support for these Stratix IV E devices:
- Full support for these Stratix IV devices: EP4SE40, EP4SE100, EP4SE230, EP4SE290, EP4SE360, EP4SE530, EP4SGX110, EP4SGX290, EP4SGX360, EP4SGX530, EP4SE820
- Compilation support for this HardCopy® III device: HC325
- Compilation support for these HardCopy IV E devices: HC4E25, HC4E35
- Compilation support for these HardCopy IV GX devices: HC4GX15, HC4GX25, HC4GX35

The Quartus II software version 9.1 SP1 adds support for the following devices:

- Initial information support for these Cyclone IV GX devices: EP4CGX30, EP4CGX50, EP4CGX75, EP4CGX110, EP4CGX150
- Advance support for these Cyclone IV E devices: EP4CE6, EP4CE10, EP4CE15, EP4CE22, EP4CE30, EP4CE40, EP4CE55, EP4CE75, EP4CE115
- Full support for these Arria II GX devices: EP2AGX190, EP2AGX260
- Full support for these Stratix IV devices: EP4SGX290, EP4SGX360, EP4SGX530
- Compilation support for these HardCopy IV E devices: HC4E25, HC4E35
- Compilation support for these HardCopy IV GX devices: HC4GX15, HC4GX25, HC4GX35

The Quartus II software version 9.1 adds support for the following devices:

- Initial information support for these Cyclone IV GX devices: EP4CGX15, EP4CGX22, EP4CGX30
- Advance support for these Cyclone III LS devices: EP3CLS70, EP3CLS100

- Advance support for these HardCopy IV GX devices: HC4GX15, HC4GX25, HC4GX35
- Advance support for these Stratix IV devices: EP4SE360, EP4SE820, EP4S40G5, EP4S100G3, EP4S100G4, EP4S100G5, EP4SGX70HF35, EP4SGX110HF35, EP4SGX290KF43, EP4SGX290NF45, EP4SGX360KF43, EP4SGX360NF45, EP4SGX530KF43
- Full support for these Arria II GX devices: EP2AGX45, EP2AGX65, EP2AGX125ES
- Full support for these Cyclone III LS devices: EP3CLS150, EP3CLS200
- Full support for these HardCopy III devices: HC325, HC335
- Full support for these Stratix IV devices: EP4SE530ES, EP4SGX180, EP4SGX230, EP4SGX530ES, EP4S40G2, EP4S100G2

EDA Interface Information

The Quartus II software version 9.1 SP2 supports the following EDA tools:

Synthesis Tools	Version	NativeLink Support
Synopsys Synplify & Synplify Pro	C-2009.06	✓
Mentor Graphics Precision RTL Synthesis	2009a	✓
Mentor Graphics LeonardoSpectrum	2009a	✓
Synopsys Design Compiler	2004.12-SP4	
Mentor Graphics DK Design Suite	5.0 SP5	✓
Simulation Tools	**Version**	**NativeLink Support**
Mentor Graphics ModelSim	6.5b	✓
Mentor Graphics ModelSim-Altera	6.5b	✓
Mentor Graphics ModelSim-Altera Starter Edition	6.5b	✓
Cadence NC-Sim	8.2 (Linux only)	
Synopsys VCS / VCS MX	Y-2009.06-SP1	✓
Aldec Active-HDL	8.1-SP2 (Windows only)	✓
Aldec Riviera-PRO	2009.06	✓
Formal Verification Tools (Equivalence Checking)	**Version**	**NativeLink Support**
Cadence Encounter Conformal	8.1	
Chip Level Static Timing Analysis	**Version**	**NativeLink Support**
Synopsys PrimeTime	Z-2007.06	✓
Board Level Static Timing Analysis	**Version**	**NativeLink Support**
Mentor Graphics TAU	3.7	
Board Level Symbol/Pin-out Management	**Version**	**NativeLink Support**
Mentor Graphics I/O Designer	7.3	

Changes to Software Behavior

This section documents instances in which the behavior and default settings of this release of the Quartus II software have been changed from earlier releases of the software.

Items listed in the following table represent cases in which the behavior of the current release of the Quartus II software is different from a previous version.

Description	Workaround
Version 9.1 SP1	
The following Cyclone IV GX devices are not supported in the Quartus II software version 9.1 SP1 and later: ■ EP4CGX15BN11C6 ■ EP4CGX15BN11C7 ■ EP4CGX15BN11I7	
For the Cyclone IV GX device family, the RESERVE_ASDO_AFTER_CONFIGURATION assignment is not available. In the Quartus II software version 9.1, you could use a RESERVE_ASDO_AFTER_CONFIGURATION assignment to reserve both ASDO/DATA1 and *n*CSO pins in Bank 9 as user I/O pins in user mode. In the Quartus II software version 9.1 SP1 and later, the RESERVE_ASDO_AFTER_CONFIGURATION assignment is not available for the Cyclone IV GX device family. This change enables Fast Passive Parallel (FPP) configuration for some Cyclone IV GX devices, allowing you to reserve the ASDO/DATA1 pin while keeping the *n*CSO pin available for general purpose I/O.	To reserve a ASDO/DATA1 pin, use a RESERVE_DATA1_AFTER_CONFIGURATION assignment. To reserve a *n*CSO pin, use a RESERVE_FLASH_NCE_AFTER_CONFIGURATION assignment.
In the Quartus II software version 9.1, RX PCS and TX PCS clock names reported by the TimeQuest Timing Analyzer are incorrect. For example, in the Quartus II software version 9.1, the TimeQuest Timing Analyzer might report `xcvr_alt4gxb_component|receive_pcs0|clkout` as `xcvr_alt4gxb_component|receive_pcs0|recoveredclk` In the Quartus II software version 9.1 SP1 and later, the clock names reported by the TimeQuest Timing Analyzer are correct.	If you are using SDC assignments written for the Quartus II software version 9.1 in the Quartus II software version 9.1 SP1 or later, verify that your RX PCS and TX PCS clock names are correct.
Version 9.1	
ACEX, APEX, FLEX, and HardCopy Stratix device families are not provided with the Quartus II software version 9.1 and later.	Use the Quartus II software version 9.0 SP2 or earlier to support those devices. The Quartus II software version 9.0 and the associated service packs will remain available on the Altera website (http://www.altera.com).
The Simulator and the Waveform Editor will not be provided in future versions of the Quartus II software beginning with version 10.0.	Use the Quartus II software version 9.1 SP2 or earlier, Mentor Graphics ModelSim-Altera Edition, or a third-party EDA simulator and waveform editor.

Description	Workaround
For Arria II GX, Cyclone III, Cyclone IV, HardCopy III, HardCopy IV, Stratix III, and Stratix IV devices, Analysis and Synthesis performs timing-driven synthesis by default.	To turn off timing-driven synthesis, turn off **Timing-Driven Synthesis** on the **Analysis and Synthesis** page of the **Settings** dialog box.
Changes to the default assignment settings in the Quartus II software include the following: ■ The default value of PARALLEL_SYNTHESIS has changed to **On.** ■ For Arria II GX, Cyclone III, Cyclone IV GX, HardCopy III, HardCopy IV, Stratix III, and Stratix IV devices, the default value of SYNTH_TIMING_DRIVEN_SYNTHESIS has changed to **On**.	
Changes to TimeQuest Timing Analyzer behavior in the Quartus II software version 9.1 include the following: ■ **set_max_skew** now includes utsu, uth, utco, from_clock, to_clock, and clock_uncertainty. ■ In designs that target Stratix III devices, if ENA_REGISTER_MODE of the ena port is set to DOUBLE_REGISTER, the internal register-to-register timing of the enable signal is guaranteed by design and is excluded from timing analysis. ■ Stratix III I4 timing models have been updated in the Quartus II software versions 9.0 SP2 and 9.1. Only timing delays in Low Power mode LABs and Low Power mode MLABs in I4 industrial speed grade devices are affected. This change in the timing models may affect your static timing analysis and fitting result. Existing designs that target Stratix III I4 devices might exhibit some degradation in performance after timing analysis with the TimeQuest Timing Analyzer in the Quartus II software version 9.1. However, a full recompilation of the design removes any degradation in performance. Other speed grade devices (I3 and I4L at 1.1V; I4L at 0.9V; and all commercial speed grades) are not affected.	If your design works correctly in your hardware system, Altera recommends that you take no action. Otherwise, Altera recommends that you fully recompile the design.
Mentor Graphics ModelSim-Altera Edition no longer includes the alt_vtl library used to simulate MAX+PLUS II designs.	Use the alt_vtl library from the Mentor Graphics ModelSim-Altera Edition version 6.4a.
In designs that target Stratix IV devices, ALTGX megafunction instances created with the **Use external termination** option turned on in the Quartus II software version 9.0 and earlier did not disable internal termination. The Quartus II software version 9.1 disables internal termination when the **Use external termination** option is turned on.	This change in software behavior decreases the resistance in designs that use external termination and may change measured signal characteristics compared to those measured in previous versions of the Quartus II software. This change in software behavior does not affect designs that use internal termination.
Starting in the Quartus II software version 9.1, an ALTGX megafunction generates only a 1-bit rateswitch port for PCIE Gen 2 x4/x8 configurations. In previous versions of the Quartus II software, an ALTGX megafunction generated 4- or 8-bit rateswitch ports, of which only bit 0 was used.	

Known Issues & Workarounds

General Quartus II Software Issues

Issue	Workaround
Version 9.1 SP1	
Quartus II Help in the Quartus II software version 9.1 SP1 and earlier incorrectly states that the Fitter does not include **set_max_skew** constraints in design optimization, however, **set_max_skew** constraints are optimized by the Fitter. The **set_max_skew** command is available in the **::quartus::sdc_ext 1.0** Tcl package.	
If you use the Remote System Upgrade configuration scheme to create a Programmer Object File (**.pof**) to update a device programmed with a **.pof** from a previous version of the Quartus II software, the Quartus II software version 9.1 SP1 might generate an internal error similar to the following: `Internal Error: Sub-system: PGMIO, File: /quartus/pgm/pgmio/pgmio_pof_diff.cpp, Line: 635 data do not match`	Use the version of the Quartus II software you used to generate the original **.pof** to create the updated **.pof**.
If you implement an ALTCLKCTRL megafunction and then run the Design Assistant, the Design Assistant might generate a message similar to the following: `Critical Warning: (Critical) Rule C101: Gated clock should be implemented according to the Altera standard scheme. Found 1 node(s) related to this rule.`	You may safely ignore this message.

Issue	Workaround
Version 9.1	

If you use variable part select with two-dimensional arrays, the Quartus II software version 9.1 SP1 generates an error similar to the following:
`no support for variable part select of multidimensional arrays (System Verilog)`
The Quartus II software version 9.1 does not correctly synthesize variable part select with two-dimensional arrays.
For example, the following Verilog statements are not synthesized correctly:
`logic s[3:0] ;`
`logic [0:w-1][3:0]m ;`
`s = m[i+1];`
	Do not use variable part select with two-dimensional arrays. Use multiple constant part selects such as `m[2+:1]`, and then choose from them.

The Quartus II software version 9.1 does not correctly synthesize `disable` statements when the `disable` statement refers to a labeled statement. For example, the following Verilog statements are not synthesized correctly:
`lbl: out1 ,=r1^r2;`
`disable lbl;`
	Rewrite your code so that the statement is surrounded by a begin-end block and name the block after the begin keyword. For example, the following is synthesized correctly:
	`begin: lbl`
	`out1 <=r1^r2;`
	`disable lbl;`
	`end;`

Running Partition Merge after importing a design with empty partitions created with a previous version of the Quartus II software results in the following error: `Error: Missing required database file.`	Run Analysis and Synthesis before running Partition Merge.
For the ALTFP_MATRIX_MULT megafunction, the maximum column and row sizes for input matrices is limited to 64.	
If you attempt to add the ALTFP_MATRIX_MULT megafunction to your project with the MegaWizard Plug-In Manager, the MegaWizard Plug-In Manager fails to add the altfpc_lib library to your project.	Manually include the **altfpc_lib.v** or **altfpc_lib.vhd** file in the project.
If you attempt to add the ALTFP_MATRIX_INV megafunction to your project with the MegaWizard Plug-In Manager, the MegaWizard Plug-In Manager fails to add the altfpc_lib library to your project.	Manually include the **altfpc_lib.v** or **altfpc_lib.vhd** file in the project.

Issue	Workaround

The ALTFP_CONVERT megafunction fixed-point-to-floating-point and floating-point-to-fixed-point features are supported only from a command prompt.	To create an ALTFP_CONVERT megafunction that converts a single precision value to a Q16.16 fixed point value for a design that targets a Stratix III device, type the following at a command prompt:
	`clearbox cbx_altfp_convert CBX_AUTO_BLACKBOX=ALL OPERATION=FLOAT2FIXED WIDTH_EXP_INPUT=8 WIDTH_MAN_INPUT=23 WIDTH_INT=16 WIDTH_RESULT=32 DEVICE_FAMILY=STRATIXIII clock dataa result cbx_file=float2fixed.v`
	To create an ALTFP_CONVERT megafunction that converts a Q16.16 fixed point value to a single precision value, thy the following at a command prompt:
	`clearbox cbx_altfp_convert CBX_AUTO_BLACKBOX=ALL OPERATION=FIXED2FLOAT WIDTH_EXP_OUTPUT=8 WIDTH_MAN_OUTPUT=23 WIDTH_INT=16 WIDTH_DATA=32 DEVICE_FAMILY=STRATIXIII clock dataa result cbx_file=fixed2float.v`

At a resolution of 1024x768, the MegaWizard Plug-in Manager cannot display settings for the ALTREMOTE_UPDATE, ALTPLL, and ALTGX megafunctions.	Change your display settings to a higher resolution.
When a RAM is inferred under all the following conditions, the synthesized circuit is not guaranteed to be correct: ■ The read from and write to the memory occur in the same always block or process. ■ The always block or process that reads/writes to the memory array is combinational. The write assignment happens before the read.	To solve this problem, either disable RAM inference or rewrite the HDL description of the RAM. RAM inference can be disabled by setting the `auto_ram_recognition` variable to **Off**. Alternatively, a different HDL description can be used for the RAM (refer to the "Inferring Memory Functions from HDL Code" chapter in the *Quartus II Handbook*).
When you compile a project and then try to open the Assignment Editor, the Quartus II software displays an internal error if the selected devices in the **Migration Devices** dialog box include EP4SGX290KF40C3, EP4SGX360KF40C3, and EP4SGX530KH40C3.	In the **Device** page in the **Settings** dialog box, click **Migration Devices**. In the **Migration Devices** dialog box, click **OK** to close the dialog box. In the **Device** page, click **OK** to close the page.

In projects targeting Stratix IV GT and Arria GX devices, transceivers with ALTGX instances created in the Quartus II software version 9.0 SP1 might display an internal error in versions of the Quartus II software later than 9.0 SP1:
`Internal Error: Sub-system: FHSSI, File: /quartus/fitter/fhssi/fhssi_cell_group.cpp, Line: 1463`
`aux_cell != NULL`
	Regenerate the ALTGX instances.

Platform-Specific Issues

Windows Platforms Only

Issue	Workaround
Version 9.1	

If you attempt to install the Quartus II software version 9.1 to a disk drive that uses a FAT32 file system, installation fails and Windows generates an error similar to the following:
`File Error`
`The following error occurred on the file <file name>.`
`The directory or file cannot be created (0x52)`
	Refer to the solution available at http://www.altera.com/support/kdb/solutions/rd11122009_735.html.

Linux Platforms Only

Issue	Workaround
Version 9.1 SP1	

If you edit an existing megafunction variation with the MegaWizard, the Quartus II software might generate an error similar to the following:
`** Parsing error, line 1, uri file:/tmp/data911947738521942821 1iptb`
`Content is not allowed in prolog.`
	You may safely ignore this message.

Version 9.1	
The Quartus II Web Edition software version 9.1 for Linux is a beta release. This beta version allows you to experience the software before it is officially released, but it may have limited-feature functionality.	For a complete listing of features available with the Quartus II Web Edition software version 9.1 for Linux, refer to the Quartus II Web Edition Software download site.
If you access the TimeQuest Timing Analyzer GUI using remote access tools such as VNC, Xvnc, and Exceed, the GUI might become unresponsive.	Refer to the solution available at http://www.altera.com/support/kdb/solutions/rd02232010_42.html
The Toolbar dialog box does not close.	Close the Customize dialog box before attempting to close the Toolbar dialog box
The Quartus II GUI cannot be resized. This issue is corrected in the Quartus II software version 9.1 SP1	Refer to the solution available at http://www.altera.com/support/kdb/solutions/rd11102009_744.html.

Device Family Issues

Arria II GX

Issue	Workaround
Version 9.1 SP1	
In the Quartus II software, delay locked loops (DLLs) are numbered from 0 to 1. However, Chapter 7 "External Memory Interfaces in Arria II GX Devices" in Volume 1 of the *Arria II GX Device Handbook* numbers DLLs from 1 to 2.	Use numbers 0 to 1 to refer to DLLs when you make location assignments in the Quartus II software.
Version 9.1	
Netlists that have been exported using the Quartus II software version 9.1 cannot be imported to later versions of the Quartus II software.	Recompile your design using the Quartus II software version 9.1 SP1 or later.
For designs targeting EP2AGX45 and EP2AGX65 devices, the Quartus II software version 9.1 might incorrectly generate programming files, causing functional failures in some devices. This issue can occur when you program your device with the Quartus II Programmer or when you use any of the following file formats: **.pof**, **.rbf**, **.hexout**, **.ttf**, **.rpd**, **.jic**, **.jbc**, and **.svf**. This issue is corrected in the Quartus II software version 9.1 SP1.	Refer to the solution available at http://www.altera.com/support/kdb/solutions/rd11192009_371.html.
The Memory Initialization File (**.mif**) Generator might not create accurate data for designs that target the Arria II GX device family. This issue is corrected in the Quartus II software version 9.1 SP1.	In the generated **.mif**, change bit numbers 6 and 7 of the second word of the MIF header (MIF address "1") from "00" to "10". Note that the bit counting starts at 0.
In the Quartus II software version 9.1 and earlier, if an MLAB is configured without a clock enable and the MLAB does not share the same clock routing as its datain registers, write failures may occur in designs that target Stratix III, Stratix IV GX, or Arria II GX devices. In this configuration, the Assembler incorrectly grounds the clock enable of the MLAB and disables the write operation of the MLAB. This issue is corrected in the Quartus II software version 9.1 SP1.	If your design compiled in the Quartus II software version 9.1 or earlier and has run successfully in hardware, no action is required. Otherwise, refer to the solution available at http://www.altera.com/support/kdb/solutions/rd12272009_328.html.
Compilation of a design targeting an Arria II GX device that uses LVDS without Dynamic Phase Alignment (DPA) and a data rate higher than 840Mbit/s generates a report panel entitled "Transmitter/Receiver Package Skew Compensation" to guide you to compensate for the skew on your board trace. In the "Estimated TCCS/Sampling Window Reduction" column (the last column of the report panel), the delay reduction reported may be inconsistent with the value reported in "Recommended Trace Delay Addition."	Use the Recommended Trace Delay Addition value to compensate for the skew and ignore the Estimated TCCS/Sampling Window Reduction values.
For designs that use Arria II GX transceivers, generation of HSPICE Simulation Deck files with the EDA Netlist Writer is not supported.	To generate HSPICE Simulation Deck files, create a revision of your design and remove the transceiver pins from the revision.

Cyclone III

Issue	Workaround
Version 9.1 SP1	
The TimeQuest Timing Analyzer overestimates LVDS buffer output delays. This issue is corrected in the Quartus II software version 9.1 SP2	Use the Quartus II software version 9.1 SP2.
For designs that target Cyclone III, Cyclone IV, Stratix III, and Stratix IV devices, Design Space Explorer (DSE) selects the best result incorrectly. This issue is corrected in the Quartus II software version 9.1 SP2.	Manually identify the best result by performing the following steps: 1. Specify the exploration parameters you want DSE to use. 2. On the DSE Options menu, turn on **Archive All Compilations**. 3. Run DSE. 4. On the DSE Processing menu, click **View Last DSE Report for Project**. 5. In the DSE Report, review the Detailed Results table to correctly identify the best exploration point. The Detailed Results table is located in the Flow Summary section. 6. If you want to open the best design revision in the Quartus II software, open the Quartus II Archive File (**.qar**) corresponding to the best exploration point you identified in step 5. The **.qar** file is located in the *<design directory>***/dse** directory.

Cyclone IV E

Issue	Workaround
Version 9.1 SP2	
The cyclical redundancy check (CRC) feature is not supported with a core voltage set to 1.0 V. Additionally, the Quartus II software version 9.1 SP2 does not generate an error if an unsupported CRC block is instantiated, unless you use the CRCERROR pin.	Do not use the CRC feature with a core voltage of 1.0 V.

Version 9.1 SP1	
For designs that target Cyclone III, Cyclone IV, Stratix III, and Stratix IV devices, Design Space Explorer (DSE) selects the best result incorrectly. This issue is corrected in the Quartus II software version 9.1 SP2.	Manually identify the best result by performing the following steps: 1. Specify the exploration parameters you want DSE to use. 2. On the DSE Options menu, turn on **Archive All Compilations**. 3. Run DSE. 4. On the DSE Processing menu, click **View Last DSE Report for Project**. 5. In the DSE Report, review the Detailed Results table to correctly identify the best exploration point. The Detailed Results table is located in the Flow Summary section. If you want to open the best design revision in the Quartus II software, open the Quartus II Archive File (**.qar**) corresponding to the best exploration point you identified in step 5. The **.qar** file is located in the *<design directory>***/dse** directory.

For Cyclone IV EP4CE6FI7 devices, the Passive Parallel configuration scheme is not supported in the Quartus II software version 9.1 SP1.	Ensure that your pin placement is compatible with the Passive Parallel configuration scheme by performing the following steps:
	1. Set the same V_{CCIO} voltage level for I/O Bank 1 and I/O Bank 8. The V_{CCIO} voltage level of these two banks must be one of the following: 1.5 V, 1.8 V, 2.5 V, 3.0 V, or 3.3 V.
	2. Reserve `DATA[2..7]` pin locations for the Passive Parallel configuration scheme by including the following assignments in your project's Quartus II Settings File (**.qsf**):
	`set_instance_assignment -name RESERVE_PIN "AS INPUT TRI-STATED" -to ~ALTERA_DATA2~`
	`set_instance_assignment -name RESERVE_PIN "AS INPUT TRI-STATED" -to ~ALTERA_DATA3~`
	`set_instance_assignment -name RESERVE_PIN "AS INPUT TRI-STATED" -to ~ALTERA_DATA4~`
	`set_instance_assignment -name RESERVE_PIN "AS INPUT TRI-STATED" -to ~ALTERA_DATA5~`
	`set_instance_assignment -name RESERVE_PIN "AS INPUT TRI-STATED" -to ~ALTERA_DATA6~`
	`set_instance_assignment -name RESERVE_PIN "AS INPUT TRI-STATED" -to ~ALTERA_DATA7~`
	`set_instance_assignment -name IO_MAXIMUM_TOGGLE_RATE "0 MHz" -to ~ALTERA_DATA*~`
	`set_location_assignment PIN_E8 -to ~ALTERA_DATA2~`
	`set_location_assignment PIN_F8 -to ~ALTERA_DATA3~`
	`set_location_assignment PIN_B7 -to ~ALTERA_DATA4~`
	`set_location_assignment PIN_E7 -to ~ALTERA_DATA5~`
	`set_location_assignment PIN_E6 -to ~ALTERA_DATA6~`
	`set_location_assignment PIN_A5 -to ~ALTERA_DATA7~`

Cyclone IV GX

Issue	Workaround
Version 9.1 SP2	
Using a post-fit netlist to simulate (with or without timing) a VHDL design that uses the XAUI protocol might not work properly.	Use a mixed-language simulator based on the Verilog HSSI model.
Version 9.1 SP1	
If you attempt to instantiate an ALTGX megafunction in Basic mode with a `tx_forceelecidle` input port, instantiation fails and the Quartus II software generates a message similar to the following: `Error: ATOM <transceiver atom instance name> has port FORCEELECIDLE that cannot be connected because parameter datapath_protocol is not pipe` The Quartus II software version 9.1 SP1 does not support the `tx_forceelecidle` input port with ALTGX megafunctions instantiated in Basic mode.	Do not use the `tx_forceelecidle` input port.
During fitting, if a pin has the following assignments: ■ **I/O Standard** set to **1.5 V** ■ **Slew Rate** set to **2** ■ **Current Strength** set to **16 mA** the Quartus II software may generate an internal error similar to the following: `Internal Error: Sub-system: SIN, File: /quartus/tsm/sin/sin_titan_manager_body.cpp, Line: 533 Could not simulate with the default board trace model`	Change the **Slew Rate** or **Current Strength** pin assignment to a different setting.
Version 9.1	
In the New Project wizard, selecting a (not installed) device generates an internal error in the Quartus II software.	Select an installed device.

Stratix II

Issue	Workaround
Version 9.1	

If your design contains encrypted IP, exporting version-compatible database files or archiving HardCopy handoff files may result in an error similar to the following:
`Error: Can't generate HDBX file for the project because the encrypted source file cannot be located: "<file name>"`
`Error: Can't generate ATMX file for the project because the encrypted source file cannot be located: "<file name>"`
	Refer to the solution available at http://www.altera.com/support/kdb/solutions/rd11092009_176.html

Stratix II GX

Issue	Workaround
Version 9.1	
In reconfigurable ALT2GXB instances, the PLL logical number and PLL location number must match in order to work properly in hardware. If the logical number and location number do not match, the Quartus II software generates a message similar to the following: `Error: Can't place GXB CMU PLL`	Ensure that the PLL logical number and PLL location number match.

Stratix III

Issue	Workaround
Version 9.1 SP2	
MegaWizard-generated RAM blocks with read-during-write behavior set to New Data have `read_during_write_mode_port_a` and `read_during_write_port_b` parameters set to `NEW_DATA_WITH_NBE_READ`, even if no byte enable is used. These parameter settings negatively affect performance.	Set `read_during_write_mode_port_a` and `read_during_write_mode_port_b` to `NEW_DATA_NO_NBE_READ`.
The cyclical redundancy check (CRC) feature is not supported with a core voltage set to 0.9 V. Additionally, the Quartus II software version 9.1 SP2 does not generate an error if an unsupported CRC block is instantiated, unless you use the `CRCERROR` pin.	Do not use the CRC feature with a core voltage of 0.9 V.
Version 9.1 SP1	
For designs that target Cyclone III, Cyclone IV, Stratix III, and Stratix IV devices, Design Space Explorer (DSE) selects the best result incorrectly. This issue is corrected in the Quartus II software version 9.1 SP2.	Manually identify the best result by performing the following steps: 1. Specify the exploration parameters you want DSE to use. 2. On the DSE Options menu, turn on **Archive All Compilations**. 3. Run DSE. 4. On the DSE Processing menu, click **View Last DSE Report for Project**. 5. In the DSE Report, review the Detailed Results table to correctly identify the best exploration point. The Detailed Results table is located in the Flow Summary section. If you want to open the best design revision in the Quartus II software, open the Quartus II Archive File (**.qar**) corresponding to the best exploration point you identified in step 5. The **.qar** file is located in the *<design directory>*/**dse** directory.
If you configure an M144K memory block as x36 on port A or x18 on port B and data[0] is not connected, the block's other data lines might not be routed correctly.	Refer to the solution available at http://www.altera.com/support/kdb/solutions/rd01272010_556.html

In the Quartus II software, delay locked loops (DLLs) are numbered from 0 to 3. However, Chapter 8 “External Memory Interfaces in Stratix II Devices” in Volume 1 of the *Stratix III Device Handbook* numbers DLLs from 1 to 4.	Use numbers 0 to 3 to refer to DLLs when you make location assignments in the Quartus II software.
Version 9.1	
In the Quartus II software version 9.1 and earlier, if an MLAB is configured without a clock enable and the MLAB does not share the same clock routing as its `datain` registers, write failures may occur in designs that target Stratix III, Stratix IV GX, or Arria II GX devices. In this configuration, the Assembler incorrectly grounds the clock enable of the MLAB and disables the write operation of the MLAB. This issue is corrected in the Quartus II software version 9.1 SP1.	If your design compiled in the Quartus II software version 9.1 or earlier and has run successfully in hardware, no action is required. Otherwise, refer to the solution available at http://www.altera.com/support/kdb/solutions/rd12272009_328.html
In reconfigurable ALT2GXB instances, the PLL logical number and PLL location number must match in order to work properly in hardware. If the logical number and location number do not match, the Quartus II software generates a message similar to the following: `Error: Can't place GXB CMU PLL`	Ensure that the PLL logical number and PLL location number match.

Stratix IV

Issue	Workaround
See Stratix IV GX	

Stratix IV GX

Issue	Workaround
Version 9.1 SP1	
For designs that target Cyclone III, Cyclone IV, Stratix III, and Stratix IV devices, Design Space Explorer (DSE) selects the best result incorrectly. This issue is corrected in the Quartus II software version 9.1 SP2.	Manually identify the best result by performing the following steps: 1. Specify the exploration parameters you want DSE to use. 2. On the DSE Options menu, turn on **Archive All Compilations**. 3. Run DSE. 4. On the DSE Processing menu, click **View Last DSE Report for Project**. 5. In the DSE Report, review the Detailed Results table to correctly identify the best exploration point. The Detailed Results table is located in the Flow Summary section. If you want to open the best design revision in the Quartus II software, open the Quartus II Archive File (**.qar**) corresponding to the best exploration point you identified in step 5. The **.qar** file is located in the *<design directory>***/dse** directory.

Issue	Workaround
In the Quartus II software, delay locked loops (DLLs) are numbered from 0 to 3. However, Chapter 7 "External Memory Interfaces in Stratix IV Devices" in Volume 1 of the *Stratix IV Device Handbook* numbers DLLs from 1 to 4.	Use numbers 0 to 3 to refer to DLLs when you make location assignments in the Quartus II software.
Version 9.1	
In the Quartus II software version 9.1 and earlier, if an MLAB is configured without a clock enable and the MLAB does not share the same clock routing as its datain registers, write failures may occur in designs that target Stratix III, Stratix IV GX, or Arria II GX devices. In this configuration, the Assembler incorrectly grounds the clock enable of the MLAB and disables the write operation of the MLAB. This issue is corrected in the Quartus II software version 9.1 SP1.	If your design compiled in the Quartus II software version 9.1 or earlier and has run successfully in hardware, no action is required. Otherwise, refer to the solution available at http://www.altera.com/support/kdb/solutions/rd12272009_328.html
With the ALTGX megafunction, if your design uses dynamic protocol reconfiguration from x4 bonding in basic mode to XAUI or PCIE x4 protocols, simulation fails.	
The ALTGX_RECONFIG megafunction cannot support both Tx data rate division and channel/PLL reconfiguration simultaneously.	
If you attempt to instantiate an ALTGX megafunction with the following settings: ■ **Which protocol will you be using?** set to **Basic (PMA Direct)** ■ **Which subprotocol will you be using?** set to **XN** ■ **What is the number of channels?** set to a value greater than **4** ■ **Enable Channel and Transmitter PLL reconfiguration** set to **On** ■ **Use additional CMU/ATX Transmitter PLLs from outside the Transceiver block** set to **On** ■ you select a total of two PLLs, and ■ you select PLL3 as the PLL logical reference index of the main PLL the Quartus II software generates an internal error.	Create the ALTGX instance with one channel, and duplicate the one-channel instance in your design to create multiple channels.
If you enable serial loopback between two PMA Direct mode ALTGX transceivers placed in different channels or quads, communication between the transceivers may fail.	Enable serial loopback only between input and output pins on the same channel or quad.

Issue	Workaround
ALTGX x8 bonding (PCIE and Basic) with reconfiguration is not working appropriately in the Quartus II software version 9.1.	
ALTGX receivers in Basic (PMA Direct) mode may encounter a hardware hold failure in the transfer to core logic if default timing constraints are used, even after passing timing analysis with the preliminary timing model.	To ensure that the core registers latch the receiver's data with the same clock edge that the RX PMA launched the data with, add the following line to your SDC: `set_multicycle_path -setup -from [get_registers *alt4gxb*|wire_receive_pma*_recoverdata out*] 0`

Stratix IV GT

Issue	Workaround
Version 9.1	
During fitting, timing analysis, or power analysis, incorrect voltage settings of the VCC, VCCA, or VCCD power rails can generate the following error message: `Error: The supply voltage value <voltage> applied to the <power supply> power rail is illegal for the currently selected device.`	Select supply voltage values with the **Voltage** tab of the **Settings** dialog box.

HardCopy

Issue	Workaround
Version 9.1 SP1	
Because on-chip delay variation modeling for HardCopy III and HardCopy IV is missing from the timing models in the Quartus II software version 9.1 SP1 and earlier, a design that targets a HardCopy III or HardCopy IV device might not meet timing during PrimeTime analysis although the TimeQuest Timing Analyzer reports that the design meets timing.	Apply additional clock uncertainty of approximately 200 ps.
In the Quartus II software, delay locked loops (DLLs) are numbered from 0 to 3. However, Chapter 7 “External Memory Interfaces in HardCopy IV Devices” in Volume 1 of the *HardCopy IV Device Handbook* and Chapter 7 “External Memory Interfaces in HardCopy III Devices” in Volume 1 of the *HardCopy III Device Handbook* number DLLs from 1 to 4.	Use numbers 0 to 3 to refer to DLLs when you make location assignments in the Quartus II software.

Issue	Workaround
Version 9.1	
For designs that target HardCopy IV devices, if **Target Device** is set to **Auto device selected by the Fitter** and, in the Quartus II Settings File (**.qsf**) or with Tcl assignments, you have specified package or speed grade restrictions such that no valid HardCopy IV devices can be selected by the Fitter, the Quartus II software may generate an internal error during synthesis similar to the following: `Internal Error: Sub-system: SUTIL, File: /quartus/synth/sutil/sutil_device.cpp, Line: 1242 is_legal_device()`	Assign a device to your project with the **Device** page of the Settings dialog box.
For designs that target HardCopy III or HardCopy IV devices, if, on the **Dual-Purpose Pins** tab of the **Device and Pin Options** dialog box, **Data{7 .. 1]** is set to **As output driving ground**, compilation generates an internal error similar to the following: `Unknown power supply for configuration pins`	Do not set **Data[7 .. 1]** to **As output driving ground**.
In the ALTDQ_DQS MegaWizard, if the RLDRAMII mode is set to x18 or x36 and both the **Simulation Model** and **Generate netlist** options are turned on, the following message is generated: `Failed to generate the synthesis netlist file`	Use the megafunction-generated variation file as input to third party synthesis tools.

During compilation of a design that targets a HardCopy IV device, the Quartus II software might generate errors similar to the following:
`Critical Warning: Atom "*|atx_pll0" has data field INT_CHARGE_PUMP_CURRENT_BITS value 200 in revision "test_hciv" versus 144 in revision "test"`
`Critical Warning: Atom "*|atx_pll0" has data field INT_CHARGE_PUMP_CURRENT_BITS value 160 in revision "test_hciv" versus 144 in revision "test"`
`Critical Warning: Object "Inclk0 signal type" has property field "*|altpll:altpll_component|altpll_i4f2:auto_generated|pll1 " as value "Global Clock" in revision "sbtt_stratix_bridge_top" versus "--" in revision "sbtt_stratix_bridge_top_hc"`
	You may safely ignore these messages.

SOPC Builder Issues

Issue	Workaround
Version 9.1	
The Tcl parser used by SOPC Builder uses the Tcl version 8.0 API. The Quartus II software uses the Tcl version 8.5 API. Some Tcl syntax, such as regular expressions, may behave differently in your component's **hw.tcl** folder and in the Quartus II Tcl Interpreter.	Use the Tcl version 8.0 API command set.
The Vectored Interrupt controller does not support VHDL simulation models.	
The output port reset value of a parallel input/output (PIO) module may be invalid if the **Enable individual bit set/clear output register** option is turned on for the output register and the multi-bit output port reset value is not zero.	On the **Basic Settings** page of the MegaWizard interface for the PIO core, turn off **Enable individual bit set/clear output register**.

When adding components to your system, SOPC Builder might generate messages similar to the following:
`Warning: set_module_property on deprecated property class_name, please use name instead`
`Warning: set_module_property on deprecated property preview_elaboration_callback, please use elaboration_callback instead`
`Warning: set_module_property on deprecated property preview_validation_callback, please use validation_callback instead`
	You may safely ignore these messages.

In the System Console, if you set DC gain to 4, the **transceiver_reconfig_analog_get_rx_dcgain** and **transceiver_reconfig_analog_set_rx_dcgain** Tcl commands generate the following error: `Invalid DC Gain value`	Select a DC gain value between 0 and 3.
In designs that target Arria II GX or Stratix IV devices, if you set **DC gain** to **2** with the ALTGX MegaWizard, the effective **DC gain** of the receiver is incorrectly set to **1**.	After you configure your ALTGX megafunction instance, use the ALTGX_RECONFIG megafunction to set the **DC gain** to **2**.
In the System Console, if you call **design_load** twice on the same project, you lose plugin services.	Call **design_load** only once per design, per System Console session. If you need to reload the design, start a new System Console.

EDA Integration Issues

Issue	Workaround
Version 9.1	
Attempting to simulate the UNIPHY megafunction's generic memory model in the sample design provided with the Cadence NC-sim software version 8.2 fails with an error similar to the following: `Queue uses an element data type that is not currently supported.`	Use a vendor or third-party generic memory model.
On Linux computers, attempting to run the Mentor Graphics ModelSim-Altera or Mentor Graphics ModelSim-Altera Starter Edition **vsim** command from the *<path to ModelSim>*/**bin** directory generates an error similar to the following: `Error: cannot find /apps/altera/quartusII/9.1.linux.cb/modelsim_ase/bin/linux/vsim`	Run the **vsim** command from the *<path to ModelSim>*/**linuxaloem** directory.

Memory Interface Issues

Issue	Workaround
Version 9.1	
If a UNIPHY instance is generated in slave mode, the timing constraints are incorrect. In slave mode, the PLL is not instantiated inside the PHY, but is assumed to be external to the PHY. This issue is corrected in the Quartus II software version 9.1 SP1.	Manually edit the following two files: ■ *<core>*/**constraints**/*<core>*_**parameters.tcl**. In this file, PLL output ports are identified by their names. If the PLL is external to the PHY, replace the names of the PLL output ports with the names of the PLL ports you intend to use. ■ *<core>*/**constraints**/*<core>*.**sdc**. In this file, PLL output ports are referenced by prepending the UNIPHY hierarchy. If the PLL is external to the PHY, remove "`${inst}|`" from each PLL port reference.

In the RLDRAMII GUI of the UNIPHY megafunction, the tQKH parameter is defined as a "percentage of *half* of a clock period." However, in the generated timing constraints, the tQKH parameter is used as a "percentage of a *full* clock period." As a result, the read hold margin, as defined in the timing constraints, is too optimistic.
This issue is corrected in the Quartus II software version 9.1 SP1.
	Manually edit the following two files:
	■ *<core>*_**report_timing.tcl**
	■ *<core>*.**sdc**
	to apply the tCKH corrective factor to the equations where tQKH is used.
	For example, change
	`[ expr $tQKH * $tCK ]`
	to
	`[ expr $tQKH * $tCK * 0.45 ]`
	where '`0.45`' is an example value of the tCKH parameter. (the tCKH parameter for your memory device can be obtained from the RLDRAMII data sheet).

Issue	Workaround
If you use the ALTMEMPHY megafunction for DDR2 or DDR3 on discrete devices with dynamic parallel on-chip termination (OCT) and read or write operations occur close to each other, data written to the RAM might be corrupted.	Refer to the solution available at http://www.altera.com/support/kdb/solutions/rd01282010_876.html
During timing analysis, a warning regarding the PLL bandwidth setting may appear when there are cascading PLLs driving the ALTMEMPHY megafunction: `"Critical Warning: ALTMEMPHY PLL, <PLL name>, when fed by another PLL, must have bandwidth mode set to High instead of Auto"`	Set the bandwidth setting to **High** for the PLL using the ALTPLL megafunction.

Simulation Model Changes

altera_mf Models

Model	Changes
Version 9.1	
altqpram	■ This simulation model pertains to the APEX family only. Because the APEX family is not provided with the Quartus II software version 9.1, the altqpram model is no longer available.
altcam	■ This simulation model pertains to the APEX family only. Because the APEX family is not provided with the Quartus II software version 9.1, the altcam model is no longer available.

Note: Beginning with the Quartus II software version 9.1, APEX, FLEX, and HardCopy Stratix device families are no longer supported by the Quartus II software simulation models.

Latest Known Quartus II Software Issues

For more information about known software issues, look for information on the **Quartus II Software Support** page at the following URL:

http://www.altera.com/support/software/sof-quartus.html

You can find known issue information for previous versions of the Quartus II software on the Knowledge Database page at the following URL:

http://www.altera.com/support/kdb/kdb-index.jsp

Software Issues Resolved

The following Customer Service Requests were fixed or otherwise resolved in the Quartus II software version 9.1 SP2:

Customer Service Request Numbers Resolved in the Quartus II Software Version 9.1 SP2						
10705739	10714346	10715265	10716969	10723968	10727182	10727730
10730796	10732840	10732990	10733050	10733052	10733446	10733513
10734236	10734470	10734570	10735687	10737209	10737566	10737809
10738664	10738665	10739232	10739580	10739736	10739809	10740162
10740484	10740505	10741196	10741210	10741514	10741586	10741596
10741628	10742314	10742466	10742837	10742907	10742934	10743036
10743206	10743278	10743541	10743725	10743803	10743817	10743847
10743851	10744019	10744068	10744193	10744338	10744550	10744710
10744895	10744946	10745199	10745311	10745338	10745382	10745410
10745457	10745664	10745668	10745798	10745834	10746425	10746550
10746579	10746634	10746656	10746990	10747572	10747616	10747762
10747787	10747799	10748354	10748689	10748760	10750238	

The following Customer Service Requests were fixed or otherwise resolved in the Quartus II software version 9.1 SP1:

Customer Service Request Numbers Resolved in the Quartus II Software Version 9.1 SP1						
10673146	10676104	10678968	10679318	10679940	10691778	10692518
10693035	10694913	10696995	10701848	10703057	10704312	10705518
10708503	10711148	10711519	10711895	10712113	10713194	10713618
10715265	10716170	10716969	10718725	10718727	10718960	10720061
10720394	10721126	10722315	10722438	10722562	10723044	10724919
10724991	10725050	10725109	10725128	10725236	10725401	10725486
10726294	10726313	10726366	10726369	10726639	10726716	10726740
10726802	10727098	10727182	10727190	10727626	10727680	10727685
10727896	10727999	10728271	10728485	10728513	10728517	10728676
10728834	10728992	10729071	10729162	10729259	10729260	10729298
10729358	10729508	10729593	10729708	10729717	10729720	10729729
10729760	10729875	10729905	10729982	10730004	10730063	10730164
10730342	10730404	10730418	10730504	10730519	10730574	10730702
10731091	10731202	10731573	10731594	10731605	10731778	10731824
10731852	10732219	10732361	10732379	10732398	10732412	10732428
10732429	10732465	10732480	10732504	10732544	10732548	10732618
10732663	10732669	10732699	10732866	10732903	10732907	10732942
10733027	10733042	10733215	10733257	10733324	10733339	10733340
10733394	10733577	10733604	10733626	10733637	10733760	10733878
10733881	10733968	10734121	10734341	10734492	10734531	10734561
10734580	10734588	10734664	10734726	10734778	10734838	10734855

Customer Service Request Numbers Resolved in the Quartus II Software Version 9.1 SP1						
10734899	10735334	10735364	10735409	10735418	10735455	10735492
10735674	10735687	10735693	10735715	10735718	10735731	10735921
10736101	10736107	10736115	10736192	10736267	10736349	10736532
10736655	10737344	10737606	10737798	10738094	10738288	10738541
10738563	10738596	10738642	10738777	10738958	10739124	10739232
10739362	10739403	10739578	10739580	10739669	10739906	10741370
10741785	10741821	10742371	10743080			

The Quartus II software version 9.1 SP2 includes the following patches released for the Quartus II software version 9.1 SP1:

Quartus II Software Version 9.1 SP1 Patches Included in this Release						
1.02	1.06	1.07	1.08	1.09	1.13	1.16
1.23	1.28	1.29	1.31	1.32	1.35	1.36
1.37	1.38	1.39	1.41			

The Quartus II software version 9.1 SP1 includes the following patches released for the Quartus II software version 9.1:

Quartus II Software Version 9.1 Patches Included in this Release						
0.01	0.03	0.06	0.08	0.09	0.10	0.11
0.12	0.13	0.16	0.20	0.21	0.22	0.23
0.25	0.26	0.28	0.29	0.30	0.32	0.34
0.35	0.39	0.41	0.44	0.45	0.46	0.50
0.51	0.52	0.53	0.54	0.58	0.59	0.60
0.62	0.63	0.65	0.67	0.68	0.69	0.73
0.75	0.77	0.78	0.85			

Revision History

Revision	Description
1.0	Initial Release

101 Innovation Drive
San Jose, CA 95134
www.altera.com
Technical Support
www.altera.com/support