Altera Complete Design Suite Version 14.0 Update Release Notes

September 2014

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The *Altera® Complete Design Suite Version 14.0 Update Release Notes* describes each of the Altera Complete Design Suite software updates. The Altera Complete Design Suite software updates are cumulative; update 2 includes update 1.

The Altera Complete Design Suite version 14.0 software updates require the Altera Quartus® II software release version 14.0. If you do not have the Quartus II software release version 14.0, please install it prior to installing any Altera Complete Design Suite version 14.0 software updates to ensure the Quartus II software runs properly.

Related Information

Quartus II Software and Device Support Release Notes Version 14.0

New Features in Update 2

The Altera Complete Design Suite version 14.0 software update 2 includes MAX® 10 device support. This is the first Altera Complete Design Suite release to include software, IP core, and programming support for the first member of the MAX 10 device family.

ModelSim®-Altera Edition software version 14.0 update 2 includes simulation support for MAX 10 device designs.

Related Information

MAX 10 Device Documentation

101 Innovation Drive, San Jose, CA 95134

Issues Addressed in Update 2

Quartus II Compilation and Design Flows

- Includes two commands to install and use MAX 10 design examples downloaded from the Design Store (**http://cloud.altera.com/devstore**):
  - To install a downloaded platform, use the command:

    ```
    quartus_sh --platform_install -package <.par file> -destination <install path>
    ```

    The `destination` is optional.
  - To create a project based on a downloaded template, use the command:

    ```
    quartus_sh --platform -name <platform name> -search_path <path to
    platform .qar file> -output <output directory> -project <output project name> -
    revision <output project revision name>
    ```

    The `search_path`, `output`, `project`, and `revision` are optional.
- Corrects the Transceiver Toolkit GUI channel numbering for automatically created channels.
- Fixes an internal error in the Design Space Explorer copy protection library (CPT) subystem; this error affected designs using incremental compilation with encrypted IP.
- Fixes an internal error that occurs when you delete any setting's assignment value in the **More EDA netlist writer settings...** dialog box (**Settings** > **EDA Tool Settings** > **Simulation**) and then reopen the dialog box.

Qsys

- Removes recommended upgrade messages from Qsys. Prior to this fix, you could erroneously receive recommended IP upgrade notifications when your IP versions were up-to-date.

IP and IP Cores

- Includes new messages relating to version compatibility and upgrading of the following IP cores:
  - alt_e40_e100
  - altera_int_osc
  - altera_pcie_256_hip_avmm
  - altera_pcie_sriov
- **40GbE MAC IP Core (Legacy)**
  - Fixes the 40-Gbps Ethernet (GbE) transmit (TX) media access control (MAC) core logic to prevent a dead-lock state when sending specific malformed packets to the TX client-side interface.
- **EMIF**
  - Fixes an issue causing unsuccessful calibration for some External Memory Interface (EMIF) designs targeting Arria® V or Cyclone® V devices.
- **HPS IP Core**
  - Fixes the displayed phase-locked loop (PLL) frequencies so only valid Hard Processor System (HPS) PLL frequencies are shown. Prior to this fix, Qsys displayed incorrect PLL frequencies for some Cyclone V devices, preventing you from selecting valid HPS PLL configurations.

- **JESD204B IP Core**
  - Updates the IP core version number to 14.0.2; the IP core was updated for the Altera Complete Design Suite version 14.0 software update 1, but the IP core version number was not updated.
- **Internal Oscillator IP Component**
  - Fixes the `clkout` signal from "conduit" to "clock output."
- **PCIe®**
  - Fixes the following single-root I/O virtualization (SR-IOV) IP issues:
    - Properly decodes the function number of the PCI Express® (PCIe) Transaction Layer Protocol (TLP) headers for a completion status match. Prior to this fix, the completion TLP headers coming back from the root complex side with various function IDs might be incorrectly decoded and forwarded to an unintended channel.
    - Includes buffering logic to release the TLP to the application layer when the end of packet (EOP) is decoded. Prior to this fix, downstream TLP headers with invalid data between the start of packet (SOP) and EOP caused the internal state machine to malfunction.
  - Fixes the PCIe Hard IP (HIP) reset module for the Arria V, Cyclone V, and Stratix® V devices when the HIP is configured as a root port; with this update, the root port will not reset the root port stack when the PCIe Link Training and Status State Machine (LTSSM) transitions to the disabled state.
- **SDI II IP Core**
  - Fixes a Serial Digital Interface (SDI) II IP core issue where the receiver (RX) cannot lock to the high definition (HD) standard with certain seeds.

DSP Builder Advanced Blockset

- Fixes an external memory interface block issue. Prior to this fix, designs using external memory interface blocks could not be synthesized or were incorrect.
- Fixes shared memory block issues. Prior to this fix, the shared memory block did not account for the endian setting of the design and ignored the LSB of the Avalon® Memory-Mapped (Avalon-MM) slave bus address when configured in read-only mode.
- Does not create obsolete Simulink types.

Nios II Embedded Design Suite

- Corrects the S-Record File (**.srec**) selection for the Arria V GZ device in **em_epcs_qsys.pm**; you can now boot the Nios II EPCQ from EPCQ256 using the Arria V GZ device.
- Fixes the 64 bit free-running timer; you can now set the counter value to 2^64.

Altera SoC Embedded Design Suite

- Fixes HPS DDR3 calibration issues for the Cyclone V device single core variants. Prior to this fix, the Quartus II software incorrectly set an on-chip termination (OCT) related bit for single core devices, resulting in calibration issues.
- The Embedded Design Suite (EDS) Flash Programmer (`quartus_hps`) includes support for 8 gigabit (Gb) NAND flash memory.
- Fixes the polarity of the Chip Enable signal.
- Fixes a USB-Blaster™ II bug in the Parallel Flash Loader, where the USB-Blaster II leaves TCK high before performing the `aji_delay` requested delay.

Altera SDK for OpenCL

- Enables loop pipelining to improve the performance of out-of-order loops in the task flow.
- Fixes compiler assertions in optimization passes, improves runtime during Verilog generation, and fixes rare deadlocking circuit scenarios.
- Updates memory dependencies to avoid compiler crashes and improve runtime.
- Fixes a bug in address logic used for lookups into multidimensional file scope constant arrays.
- Fixes a bug in big-endian hardware support that causes the final bytes of kernel argument data to become corrupted upon transfer from the host to the device. This bug was exposed when the aggregate length of a kernel's argument list was not a multiple of 4 bytes.
- Fixes an illegal Verilog bit-select range when the on-chip memory bank has a depth of one word.
- Fixes the Custom Platform Toolkit swapper test to work with any size Altera Offline Compiler Executable File (**.aocx**). Prior to this fix, the test errored out if the **.aocx** was larger than 100 megabytes (MB).
- Fixes a coalescing loop pipelining issue that could cause a crash when a shift register is used outside of the loop performing the shift operation.
- Increases emulation speed for some application classes, where a kernel with few threads communicates with a kernel with a large number of threads.
- Fixes an issue causing a crash in loop pipelining when an invariant value is incorrectly pipelined in the task flow. Prior to this fix, you could encounter the crash by using a loop with a special value in the first iteration and a loop invariant value in all subsequent iterations.
- Improves the optimization report by using the filename and line number to map to the source code. Prior to this fix, the line and column number were used to map to the source code. This improvement simplifies development when your design is split across multiple files.
- Fixes a failure to compress loop-carried values into the innermost loop of a nest when there is a sibling loop at the same depth. Prior to this fix, the failure was observed through a non-deterministic crash or incorrect results. The analysis now correctly tracks the compression value and generates the correct hardware.

Issues Addressed in Update 1

Quartus II Compilation and Design Flows

- Fixes internal error generation when concurrently acquiring multiple SignalTap™ II Logic Analyzer instances.
- Fixes an issue that occurs when you apply the "Basic OR" condition type to storage qualifier conditions. Prior to this fix, the condition logic implemented incorrectly in the SignalTap II Logic Analyzer if the tapped node set, enabled as a storage qualifier input, differed from the tapped node set enabled as a trigger input.
- Fixes the functional safety separation flow for Cyclone IV and Cyclone V device families. Prior to this fix, during the partition import of strictly preserved safety partitions, routes to top-level safe I/O buffers were not correctly preserved. The design modification flow could generate an internal error and fail when the Assembler detected the preservation mismatch.
- Fixes the error "Can't launch default web browser" when accessing PDF tutorials.
- Fixes an issue with the Tcl Script File (**.tcl**) specified by the `PRE_FLOW_SCRIPT_FILE` Quartus Settings File (**.qsf**) assignment. When the **.tcl** fails the flow now stops, but in the Quartus II software release version 14.0 the flow erroneously continued despite the error.

- Fixes an internal error that occurs when using the **User option** dialog box to update the Executable and Linking Format File (**.elf**) file path on the bus added by the Nios® II plug-in in the SignalTap II Logic Analyzer.
- Enables the input cascade feature for the 5SGXA5, 5SGXA7, 5SGTC5, and 5SGTC7 Stratix V devices. This feature was erroneously disabled in previous Altera Complete Design Suite releases.
- Fixes an issue that causes some non-Configuration via Protocol (CvP) channels to fail dynamic reconfiguration when the CvP feature is enabled in Stratix V devices.

Fitter

- Fixes an issue where an internal error occurs in the Fitter during partial reconfiguration compilations due to a failure in routing a phase-locked loop (PLL) feedback path.
- Fixes the synthesis error "selected PCS configuration is illegal." This error affected designs using partial reconfiguration and targeting Stratix V devices.
- Improves the Fitter's ability to solve hold timing in Arria V devices, focusing on registered paths terminating in digital signal processing (DSP) blocks.
- Fixes an issue where the Fitter issues an internal error when compiling a design with Arria V and Cyclone V transceivers.
- Fixes an issue that causes an internal error for designs with Low Power Double Data Rate 2 (LPDDR2) memory interfaces when the parameter tcwl = 1; this issue affected Cyclone V devices.

Quartus II Programmer

- Fixes an issue causing an internal error when you select **File** > **Combine Programming Files** and add a local update enabled SRAM Object File (**.sof**) to page 0 in Active Serial programmer mode.

USB-Blaster II

- Supports Advanced Encryption Standard (AES) key programming and fuse blowing.
- Fixes the USB-Blaster II to properly indicate the USB hub speed. The teal-colored LED indicates a high-speed USB connection and the blue-colored LED indicates a full-speed USB connection as described in the **USB-Blaster II Download Cable User Guide**.

Qsys

- Fixes an issue where the Qsys interrupt request (IRQ) bridge erroneously inserted clock crossers.

IP and IP Cores

- **40- and 100-Gbps Ethernet MAC and PHY MegaCore Function**
  - Fixes an issue in the 40-gigabits per second (Gbps) Ethernet (GbE) media access controller (MAC) that prevents outgoing pause control frames from being sent when the tranceiver (TX) is in the paused (TXOFF) state.
- **CPRI IP Core**
  - Includes a patch correcting the Cyclone V clock data recovery (CDR)/clock multiplier unit (CMU) block configuration for 6.144 Gbps CPRI.
- **DisplayPort IP Core**
  - Fixes a DisplayPort AUX channel issue that prevents video from the DisplayPort source from being transmitted to the DisplayPort MegaCore receiver (RX) at the desired resolution.
- **JESD204B IP Core**
  - Fixes the incorrect interface type of `jesd204_rx_int` and `jesd204_tx_int` to enable connection to interrupt receiver components in Qsys.
  - Fixes the signal type of `pll_locked`, `tx_cal_busy`, `rx_cal_busy` and `rx_is_lockedtodata` to resolve a signal type mismatch issue when connecting the IP core and the transceiver reset controller component in Qsys.
  - Fixes the incorrect *readLatency* value of the JESD204B Avalon Memory-Mapped (Avalon-MM) slave interfaces to prevent Qsys from generating incorrect interconnect component settings. Prior to this fix, the incorrect settings prevented data capture at the Avalon-MM master-component side during read events.
- **PCIe**
  - Fixes the Qsys direct memory access (DMA) design example provided with the preliminary single-root I/O virtualization (SR-IOV) IP; the Requester ID assigned to the transmitted packets has been corrected. This issue only affected the PCI Express (PCIe) SR-IOV DMA design example, it did not affect the Avalon-MM interface IP or the SR-IOV bridge IP.
  - Fixes the transmit FIFO buffer logic to prevent buffer underflow causing `tx_st_valid_hip` to deassert in the middle of the Transaction Layer Packet (TLP).
  - Fixes intermittent hardware failures when:
    1. The Avalon-MM interface DMA read data mover requests reading a small packet crossing a 64-byte boundary. Prior to this fix, if the host split the read request completion into a smaller completion packet, the Avalon-MM DMA embedded controller could hang
    2. Downstream burst memory requests have non-zero Traffic Class and Attribute TLP fields
    3. Operating with mixed traffic involving DMA write and high performance RXM modules
  - Fixes an issue that caused the Avalon-MM interface DMA to fail to generate files on a Windows-based platform.
  - Fixes intermittent data corruption that could occur when using the RX burst master in the Avalon-MM DMA IP during simultaneous TX traffic.
  - Fixes an issue that prevented the SR-IOV bridge from generating simulation files on the Windows OS.
- **SerialLite III Streaming IP Core**
  - Fixes an error that could occur when the SerialLite III Streaming IP core is used with certain clock frequencies; the issue affected Arria V GZ and Stratix V devices.
- **Transceiver PHY IP Core**
  - Fixes a transceiver reconfiguration issue that occurs when using both receive-only and bidirectional transceiver channels; this issue affected Cyclone V devices.

Nios II Embedded Design Suite

- Fixes the scatter-gather direct memory access (SGDMA) driver's data cache handling capability, enabling compatibility with first and second generation Nios II cores.
- Fixes an issue affecting code creation for controlling the Clocked Video Input, Clocked Video Output, Frame Reader, Switch, and Control Synchronizer IP. Prior to this fix, when you selected an SOPC Information File (**.sopcinfo**) generated from a Qsys system containing this IP, and used the file to create a new project, Eclipse failed with a "Failed to execute /create-this-bsp…" error message and no project was created.

Altera SoC Embedded Design Suite

- Fixes an issue with the SoC Golden Hardware Reference Design (GHRD) device tree node for the USB component generated by `sopc2dts`. To create a correct device tree, regenerate your design's **.sopcinfo** file with the Altera Complete Design Suite Version 14.0 Update 1 release of Qsys before using `sopc2dts`.
- Fixes an issue that occurs when the SDRAM interface drives an output port for Cyclone V device families. Prior to this fix, physical synthesis timing analysis could fail if the path to the port had the worst timing violation on the port.

Altera SDK for OpenCL

- Includes the Custom Platform Toolkit with the Software Development Kit (SDK) for OpenCL™(1); the toolkit is available at `board/custom_platform_toolkit` in your Linux or Windows installation.
- Fixes the `num_compute_units` kernel attribute allowing you to use OpenCL kernels, including `num_compute_units`, when compiling the kernel for big-endian architectures.
- Fixes an optimization failure when attempting to promote private memory to registers. Prior to this fix optimization would fail when you reinterpreted arrays as a scalar type with a larger size than the array. For example, the following codeblock will now correctly be promoted to registers:

```
unsigned char x[3];
unsigned int y = *(unsigned int *)x
```

- Includes an Altera Offline Compiler (AOC) error issued when a struct in a kernel argument contains a pointer, instead of containing a direct pointer to pointer kernel argument. Your compilation will generate an understandable error message early in your design flow if you violate the specification.
- Improves clock frequency for designs previously limited by narrow (less than 32 bit) multipliers by pipelining the narrow multiplers. Multiplication of short and byte-sized values consumes 3 clock cycles and operates at a higher clock frequency than previous releases.
- Fixes an incorrect traversal in an optimization that leads to an assertion failure when generating Verilog. You will no longer see the assertion `reachesMemDepOperand(P, TD) FAILED` when using some local memory configurations in your designs.
- Includes the following emulator improvements:
  - Supports multiple `aocx` files handled from the same host program
  - Handles more OpenCL built-in types and functions
  - Fixes memory allocation issues regarding emulations using local buffers
  - Improves error messages and printouts
- On Windows-based systems, disregards unsupported `-g` in emulator mode and improves the `-d` error message when the linker for emulation creation is not found.
- Fixes a system crash triggered by writing a shift register carried through multiple loops, where the innermost loop is not pipelined but has memory dependence.

(1) OpenCL and the OpenCL logo are trademarks of Apple Inc. used by permission of the Khronos Group™.

- On Windows-based systems, fixes an issue that could incorrectly connect I/O channels in OpenCL designs.
- Fixes memory issues by supporting logical address mapping on the the Avalon-MM interface in `altera_onchip_flash` IP; the address mapping creates contiguous memory space and the address always starts from 0.
- Allows you to use the `#pragma unroll` directive without an explicit factor value (`#pragma unroll` versus `#pragma unroll <N>`) in more cases. Expressing unrolls without an explicit factor value allows you to use cleaner, more generic code.
- Enhances Quality of Results (QoR) to increase throughput for certain coding styles. For example, when you write kernels with nested loops, and the inner-most loop is not frequently executed, the throughput significantly increases. This enhancement corrects the delay model for Boolean variables to improve the II variable.
- Adds optimization to significantly improve overall throughput of designs and reduce the FPGA resource consumption on your circuit.
- Reduces the long AOC compile time and high AOC memory usage observed when the target application has a large number of load and store instructions.
- Includes information explaining why loops are not pipelined to the optimization report, allowing you to pinpoint the cause of any unpipelined loops in your design. This update also includes analysis improvements to determine if a loop should or should not be pipelined, preventing functionally incorrect results.
- Fixes an issue where `wdapi1021.dll` was not correctly copied during installation of the reference boards.
- Fixes an issue causing extraneous error messages when you pass in incorrect parameters with the `--no-interleaving` flag, or compile kernels with illegal channel configuration.
- You can now profile kernels written in multiple **.cl** files so the profile information displays correctly in the profiler GUI. Prior to this fix, the profiler GUI incorrectly displayed multiple files, reporting false bottlenecks in the program.
- Includes language error checks in the front end compiler; unsupported OpenCL code, such as dynamic array declarations, will be caught with meaningful error messages and line number annotations included with the messages.
- Windows-based system emulation now uses the temporary directory indicated by the `TMP` or `TEMP` variable in your environment.

Software Issues Resolved

Table 1: Customer Service Requests Resolved in the Altera Complete Design Suite Version 14.0 Update 2

Customer Service Request Numbers Resolved					
11045094	11047847	11061251	11064927	11065697	11065832
11066547	11068665	11070283	11070851	11071998	11074176
11079276	11079865	11080470	11080609	—	—

Table 2: Customer Service Requests Resolved in the Altera Complete Design Suite Version 14.0 Update 1

Customer Service Request Numbers Resolved					
11050083	11058326	11061022	11064255	11069227	11070720

Customer Service Request Numbers Resolved					
11071037	11073437	—	—	—	—

Software Patches Included in Update Releases

Table 3: Software Patches included in the Altera Complete Design Suite Version 14.0 Update 2

Software Version	Patch	Customer Service Request Number
Quartus II 13.0sp1	1.79	—
Quartus II 13.1.4	4.37	11064927
Quartus II 13.1.4	4.38	11065832
Quartus II 13.1.4	4.39	11070283
Quartus II 13.1.4	4.40	—
Quartus II 13.1.4	4.42	11047847
Quartus II 13.1.4	4.48	11065832
Quartus II 14.0	0.08a	11065697, 11068665, 11070851
OpenCL 14.0	0.01cl	11066547
Quartus II 14.0.1	1.01	—

Table 4: Software Patches included in the Altera Complete Design Suite Version 14.0 Update 1

Software Version	Patch	Customer Service Request Number
Quartus II 13.1	0.92	—
Quartus II 13.1	0.100	—
Quartus II 13.1.3	3.10	11064482
Quartus II 13.1.4	4.30	—
Quartus II 13.1.4	4.32	11058326; 11064255
Quartus II 13.1.4	4.41	—
Quartus II 13.1.4	4.43	11050083
Quartus II 13.1.4	4.44	11070720
Quartus II 13.1.4	4.45	11064482
Quartus II 14.0	0.09	—

Latest Known Altera Complete Design Suite Issues

For information about known software issues, please visit the Altera Knowledge Database.

Related Information

- Altera Knowledge Database
- Altera Documentation: Release Notes
- Quartus II Software Support

Document Revision History

Table 5: Altera Complete Design Suite Version 14.0 Updates Document Revision History

Date	Document Version	Changes
September 2014	14.0.2.0	Added Altera Complete Design Suite version 14.0 update 2 information.
August 2014	14.0.1.0	Initial Release.