Altera Complete Design Suite Version 13.1 Update Release Notes

RN-01080-13.1.1.0 Release Notes

This document provides information about the Altera® Complete Design Suite version 13.1 update 1.

You must either have previously installed the Quartus II software version 13.1 or must install the Quartus II software version 13.1 before installing this update. Otherwise, the update will not be installed correctly and the Quartus II software will not run properly.

For information about the Quartus II software version 13.1, refer to the *Quartus II Software and Device Support Release Notes Version 13.1*.

Issues Addressed in Update 1

The Altera Complete Design Suite version 13.1 update 1 addresses the following software issues:

Device Support

- Provides full compilation and programming support for the following Arria V devices: 5ASXMB3E4F31I3 and 5ASXMB5E4F31I3.
- Provides full compilation and programming support for the following Cyclone V devices: 5CSEMA2, 5CSEBA2, 5CSXFC2, 5CSEMA4, 5CSEBA4, 5CSXFC4.
- Fixes an issue in the Quartus II software version 13.1 related to minor temperature-related routing resistance variances for Cyclone V devices and reverts timing delays to match those in the Quartus II software version 13.0 SP1. The impact to designs compiled with version 13.1 was small and is unlikely to cause a silicon issue.

Nios II EDS

- Corrects an issue that caused some Nios II EDS utilities to fail with no error output or messages when run on a Windows PC. The affected utilities are: `sof2flash`, `elf2flash`, `elf2hex` and `bin2flash`.

Qsys

- Adds UART1 pin location information for Arria V SoCs to the Peripherals Pin Multiplexing tab in Qsys.

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Quartus II Compilation Flows

- Fixes missing Arria V GZ Programmable Power Technology Optimization settings on the **More Settings** panel of the **Fitter Settings** dialog box in the Quartus II software.
- Fixes an internal error that was generated when a PLL clock is routed to external IO pin with a `create_generated_clock` SDC assignment. The internal error generated in previous versions of the Quartus II software was:
  `Internal Error: Sub-system: VPR20KMAIN, File: /quartus/fitter/vpr20k/quartus_interface/qi_common/vpr_qi_tis_interface.cpp, Line: 1161`
- Prevents an internal error in Advanced Single Event Upset (SEU) Detection, CvP Update, and Partial Reconfiguration flows when Strictly Preserved logic is placed into a single 1x1 Logic Lock region with no preserved routes leaving or entering the region. The internal error prevented is:
  `Internal Error: Sub-system: MSF, File: /quartus/db/msf/msf_masks_code.cpp, Line: 191 !routing.empty()`
- Fixes an issue in the Fitter where LVDS input buffers are powered by VCCPD, but VCCIO was mistakenly assigned to LVDS input pins with differential OCT.
- Fixes a problem with the register packer where register banks could be accidentally merged within DSP inputs when the input to the Fitter came from third party synthesis tools.
- Fixes an issue in which the Quartus II Fitter fails to place one or more nodes, including at least one dual-regional clock driver, generating an Error message similar to
  `Error (175001): Could not place dual-regional clock driver`
  In previous versions of the Quartus II software, this error occurred after the Fitter indicated that it had successfully placed all clocks in the design through messages like
  `Info (11178): Promoted <x> clocks...` or
  `Info (11191): Automatically promoted <x> clocks...`
- Removes incorrect error messages that can occur when using the Engineering Change Order (ECO) Fitter flow.
- Fixes an issue with VCCIO, VCCPD, and VCCN voltage rail settings in Stratix V 5SGXMBBR2H40I2L devices. Previous versions of the Quartus II software ignored a Quartus II Settings File (.qsf) assignment of `set_global_assignment -name STRATIX_DEVICE_IO_STANDARD "1.8 V"` and the I/O banks remained at 2.5 V.

Transceiver Toolkit

- Fixes an issue in the Transceiver Toolkit that caused receiver-only autosweep to always report a bit error rate of 1.

Simulation

- In previous versions of the Quartus II software, simulation of a Stratix V example design with a VHDL testbench fails in NCSIM because:
  1. Multiple copies of same file were being generated. NCSIM is not able to bind the instance to the correct module.
  2. Port corresponding to the unused lanes were not terminated during file generation.

  In Update 1, the above mentioned issues are fixed. Regenerate the files to simulate the VHDL example design in NCSIM.
- Fixes a simulation mismatch at the outputs of an adder when performing multiple DSP chaining with 18x18+36 mode through HDL code (inferencing). In previous versions of the Quartus II software, there was a chance to have a functionality issue if the input is signed and the result width for each DSP blocks are different.
- Removes unnecessary notification messages during simulation. The removed messages are of the form:
  `Input frequency on DLL instance <name> now matches with specified clock frequency.`

DSP Builder

- Fixes DSP Builder Advanced incorrectly merging duplicate delays that have configuration differences:
  - between the status of the minimum delay checkbox
  - equivalence group, if minimum delay has been checked.
- Fixes the following issues in DSP Builder Advanced optimization of constant fixed-point sub-expressions:
  - Addition and subtraction of signals with differing fraction lengths
  - Comparing signals with 0
  - Adding and subtracting without word growth and comparing with a constant
  - Comparing signals with differing fraction lengths
  - Bitwise ANDing and ORing of signals with differing fraction length
  - Adding and subtracting of non-zero constants with non-constant signals

IP

Ethernet IP Cores

- Fixes a problem in the KR4 Configuration of the 40G/100G Ethernet Megacore where reads from the MAC RX Statistics Registers may return invalid data.
- Enables MAC 10/100 half duplex support in the 10/100Mb Small MAC variation of the Triple-Speed Ethernet IP core.

EMIF IP Cores

- Fixes the behavior of the timing counters used during the power-on memory initialization and reset period of DDR memory interfaces. In previous versions of the Quartus II software, these timers assumed an AFI clock period of 266 MHz, therefore interfaces with AFI clock frequencies faster than 266 MHz had slightly shorter reset and initialization periods than the JEDEC-required specification. This change now adjusts the counters according to the AFI frequency such that the initialization time remains constant irrespective of interface frequency or rate. This change also ensures that the `Tinit` value specified in the MegaWizard Plug-In Manager under the **Memory Timing** tab modifies the initialization counter accordingly. Previous versions of Quartus hard-coded the memory initialization time to 500 µs.
  - Device Families Affected: Arria V, Cyclone V, Stratix IV, and Stratix V
  - Protocols Affected: DDR2 and DDR3 (for AFI clock frequencies greater than 266 MHz).
- Previous versions of the Quartus II software did not properly configure the memory controller for the Hard Processor Subsystem (HPS) when an LPDDR2 memory interface is selected in Arria V SoC and Cyclone V SoC devices. This problem manifests as a calibration failure error during the memory initialization phase. This update fixes this issue and this fix is recommended for any customer using LPDDR2 on an HPS.
  - Device Families Affected: Arria V SoC and Cyclone V SoC
  - Protocols Affected: LPDDR2
- In the Altera Complete Design Suite version 13.1, EMIF IP cores incorrectly issued a warning to indicate that Cyclone V timing models are preliminary. However, the last Cyclone V (non-SoC) timing models became final in ACDS 13.1. This update removes the EMIF IP preliminary timing model warning.

Software Issues Resolved

The following Customer Service Requests were fixed or otherwise resolved in the Altera Complete Design Suite version 13.1 update 1:

Customer Service Request Numbers Resolved in the Quartus II Software Version 13.1 Update 1							
10862388	10865226	10957886	10990717	10995942	11001820	11002391	11004954
11005496	11007025	11007465	—	—	—	—	—

Software Patches Included in this Release

The Altera Complete Design Suite version 13.1 update 1 includes the following patches released for previous versions of the Altera Complete Design Suite software:

Quartus II Software Version	Patch	Customer Service Request Number	Quartus II Software Version	Patch	Customer Service Request Number
13.1	0.24	10957886,10990717	13.1	0.04	11002391
13.1	0.20	—	13.1	0.02	10995942
13.1	0.16	10862388	13.0 SP1	1.dp5e	—
13.1	0.11	10845226	13.0 SP1	1.67	10957886
13.1	0.07	11004954	13.0 SP1	1.51	10865226
13.1	0.05	11001820	13.0	0.48	10957886

Latest Known Quartus II Software Issues

For more information about known software issues, can find known issue information refer to the Knowledge Database page at the following URL:

http://www.altera.com/support/kdb/kdb-index.jsp

For technical support information about the Quartus II software, refer to the **Quartus II Software Support** page at the following URL:

http://www.altera.com/support/software/sof-quartus.html

Document Revision History

The following table shows the revision history for this document.

Document Revision History

Date	Version	Changes
December 2013	13.1.1.0	Initial release.