Quartus II Software Version 10.1 Device Support

This document provides late-breaking information about device support in the Altera® Quartus® II software version 10.1. For information about disk space and system requirements, refer to the **readme.txt** file in your **altera/<*version number*>/**quartus directory. For information about new features, EDA Tool version support, and existing and resolved software issues, refer to the *Quartus II Software Release Notes*.

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Device Support and Pin-Out Status

This section contains information about the status of device support in the Quartus II software version 10.1.

Full Device Support

Full compilation, simulation, timing analysis, and programming support is now available for the following new devices and device packages:

Table 1. Devices with Full Support

Device Family	Devices	
Arria®II GZ	EP2AGZ225	EP2AGZ300
	EP2AGZ350	
Cyclone®IV GX	EP4CGX22	EP4CGX30
	EP4CGX110	EP4CGX150
HardCopy®IV GX	HC4GX15	
MAX®V	5M80ZM68	5M80ZT100
	5M160ZM68	5M160ZT100
	5M160ZM100	5M240Z
	5M570Z	5M1270Z
	5M2210Z	

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Advance Device Support

Compilation, simulation, and timing analysis support is provided for the devices listed in Table 2 that will be released in the near future. The Compiler generates pin-out information for these devices in this release, but does not generate programming files.

Table 2. Devices with Advance Support

Device Family	Devices	
Cyclone IV GX	EP4CGX50	EP4CGX75
MAX V	5M40Z	5M80ZM64
	5M80ZE64	5M160ZE64

Initial Information Device Support

Compilation, simulation, and timing analysis support is provided for the devices listed in Table 3 that will be released in the near future. Programming files and pin-out information, however, are not generated for these devices in this release.

Table 3. Devices with Initial Information Support

Device Family	Devices	
Stratix®V	5SGXA3	5SGXA4
	5SGXA5	5SGXA7
	5SGXB5	5SGXB6
	5SGSB7	5SGSB8

Memory and Disk Space Recommendations

A full installation of the Altera Complete Design Suite requires approximately 8.2 GB of available disk space on the drive or partition where you are installing the Altera Complete Design Suite and approximately 30 MB of available space on the drive that contains your **TEMP** directory (Windows only).

The Quartus II Stand-Alone Programmer requires a minimum of 1 GB of RAM plus additional memory, based on the size and number of **.sof** files and the size and number of devices being configured.

Altera recommends that your system be configured to provide virtual memory equal to the recommended physical RAM that is required to process your design.

Table 4 lists the memory required to process designs targeted for Altera devices.

Table 4. Memory and Disk Space Recommendations

Device	Recommended Physical RAM	
	32-bit	64-bit
Arria GX(EP1AGX20) Cyclone (EP1C3, EP1C4, EP1C6, EP1C12, EP1C20) Cyclone II (EP2C5, EP2C8, EP2C20) Cyclone III (EP3C5, EP3C10, EP3C16, EP3C25, EP3C40) Cyclone IV E (EP4CE6, EP4CE10, EP4CE15, EP4CE22, EP4CE30, EP4CE40) Cyclone IV GX (EP4CGX15, EP4CGX22, EP4CGX30) All MAX, MAX II, MAX V series devices Stratix (EP1S10, EP1S20) Stratix GX (EP1SGX10) Stratix II (EP2S15)	512 MB	512 MB
Cyclone III (EP3C55, EP3C80) Cyclone IV E (EP4CE55, EP4CE75)	768 MB	1.0 GB
Arria GX (EP1AGX35, EP1AGX50, EP1AGX60) Arria II GX (EP2AGX45) Cyclone II (EP2C35, EP2C50) Cyclone IV E (EP4CE115) Cyclone IV GX (EP4CGX50, EP4CGX75) Stratix (EP1S25, EP1S30, EP1S40, EP1S60) Stratix GX (EP1SGX25, EP1SGX40) Stratix II (EP2S30) Stratix II GX (EP2SGX30, EP2SGX60) Stratix III (EP3SL50, EP3SE50, EP3SL70)	1.0 GB	1.5 GB
Arria GX (EP1AGX90) Arria II GX (EP2AGX65) Cyclone II (EP2C70) Cyclone III (EP3C120) Cyclone III LS (EP3CLS70, EP3CLS100) Cyclone IV GX (EP4CGX110, EP4CGX150) HardCopy II (HC210) Stratix (EP1S80) Stratix II (EP2S60, EP2S90) Stratix II GX (EP2SGX90) Stratix III (EP3SE80) Stratix IV (EP4SGX70)	1.5 GB	2.0 GB

Table 4. Memory and Disk Space Recommendations (Continued)

Device	Recommended Physical RAM	
	32-bit	64-bit
Arria II GX (EP2AGX95, EP2AGX125, EP2AGX190) Arria II GZ (EP2AGZ225) Cyclone III LS (EP3CLS150, EP3CLS200) Stratix II (EP2S130, EP2S180) Stratix II GX (EP2SGX130) HardCopy II (HC220, HC230, HC240) Stratix III (EP3SL110, EP3SE110, EP3SE150, EP3SL200) Stratix IV (EP4SGX110, EP4SGX230, EP4S40G2, EP4S100G2)	3.0 GB	4.0 GB
Arria II GX (EP2AGX260) Arria II GZ (EP2AGZ300) Stratix III (EP3SE260, EP3SL340) Stratix IV (EP4SGX290) Stratix V (5SGXA3)	4.0 GB	6.0 GB
Arria II GZ (EP2AGZ350) Stratix IV (EP4SGX360, EP4S100G3, EP4S100G4) Stratix V (5SGXA4) HardCopy III (HC325) HardCopy IV (HC4E25)	(1)	8.0 GB
HardCopy III (HC335) HardCopy IV (HC4GX15) Stratix IV (EP4SGX530, EP4SE530, EP4SE820, EP4S40G5, EP4S100G5) Stratix V (5SGXA5, 5SGXB5)	(1)	12.0 GB
HardCopy IV (HC4E35, HC4GX25) Stratix V (5SGXA7, 5SGXB6, 5SGSB7)	(1)	16.0 GB
HardCopy IV (HC4GX35) Stratix V (5SGSB8)	(1)	20.0 GB

(1) These devices cannot be compiled on a 32-bit system.

Timing and Power Models

Table 5 lists a summary of timing and power model status in the current version of the Quartus II software.

Table 5. Devices with Timing and Power Models

Device Family	Device	Timing Model Status	Power Model Status
Arria II GX	EP2AGX45	Final – 10.0	Final – 10.0
	EP2AGX65		
	EP2AGX95		
	EP2AGX125		
	EP2AGX190	Final – 10.0 SP1	
	EP2AGX260		
Arria II GZ	All	Preliminary	Preliminary
Cyclone III LS	EPC3LS70	Final – 10.0	Final – 10.0 SP1
	EPC3LS100		
	EPC3LS150		
	EPC3LS200		
Cyclone IV E	(All 1.0V)	Final – 10.0 SP1	Final – 10.0 SP1
	(All 1.2V)	Final – 10.0	
Cyclone IV GX	EP4CGX15	Final – 10.1	Preliminary
	EP4CGX22	Preliminary	
	EP4CGX30		
	EP4CGX50		
	EP4CGX75		
	EP4CGX110	Final – 10.1	
	EP4CGX150		
HardCopy III	(All)	Preliminary	Preliminary
HardCopy IV E	(All)	Preliminary	Preliminary
HardCopy IV GX	(All)	Preliminary	Preliminary
MAX IIZ	EPM240Z	Final – 9.0 SP1	Final – 9.0 SP1
	EPM570Z		
MAX V	(All)	Preliminary	Preliminary
Stratix III	EP3SE50	Final – 9.0	Final – 9.0
	EP3SE80	Final – 8.1	
	EP3SE110	Final – 8.1	
	EP3SE260	Final – 9.0	
	EP3SL50	Final – 9.0	
	EP3SL70	Final – 9.0	
	EP3SL110	Final – 8.1	
	EP3SL150	Final – 8.1	
	EP3SL200	Final – 9.0	
	EP3SL340	Final – 8.1	

Table 5. Devices with Timing and Power Models (Continued)

Device Family	Device	Timing Model Status	Power Model Status
Stratix IV	EP4SE230	Final – 9.1 SP1	Final – 10.0
	EP4SGX180		
	EP4SGX230		
	EP4S40G2		
	EP4S100G2		
	EP4SE360	Final – 9.1 SP2	
	EP4SE530		
	EP4SGX290		
	EP4SGX360		
	EP4SGX530		
	EP4S40G5		
	EP4S100G3		
	EP4S100G4		
	EP4S100G5		
	EP4SGX70	Final – 10.0	Final – 10.1
	EP4SGX110		
	EP4SE820	Final – 10.0 SP1	
Stratix V	(All)	Preliminary	Preliminary

The current version of the Quartus II software also includes final timing and power models for the Arria GX, Cyclone, Cyclone II, Cyclone III, HardCopy II, MAX, MAX II, Stratix, Stratix II, Stratix II GX, and Stratix GX device families. Timing models for these device families became final in the Quartus II software versions 8.1 and earlier.

Changes in Device Support

The following section is divided into device support changes according to whether the change is a notification, or whether the change has been fixed or not fixed. The section pertains to all device families except for Stratix V devices.

Change Notifications

This section provides notifications for devices.

Arria II GX power model updated

For Arria II GX devices, the power model was updated to reduce static power consumption. This is a change to a finalized power model.

Applies to: Arria II GX devices

Arria II GX VCO frequency change

The maximum frequency of a PLL VCO in Arria II GX has been updated to 1.4 GHz. Designs with a PLL VCO frequency higher than 1.4 GHz will need to rerun the Fitter to recalculate the valid PLL settings.

Applies to: Arria II GX devices

Arria II GX new DLL range

The frequency range specification of the Delay Lock Loop (DLL) in Arria II GX devices is updated after further characterization.

For details and solutions, refer to the *Errata Sheet for Arria II GX*.

Applies to: Arria II GX devices

Device Support Not Fixed

This section provides details for device support issues that have not yet been fixed.

Gate-level simulation flow for Stratix V designs

The generation of EDA simulation netlist files for post-synthesis or post-fit gate-level simulation is not supported in the Quartus II software version 10.1.

Applies to: Stratix V devices

MAX 7000 S Programmer error

For MAX 7000 S devices, performing blank-check operations in the Programmer causes internal errors when using any other devices in the same JTAG chain.

Applies to: MAX 7000 S devices

Device Support Fixed

This section provides details for device support issues that have been fixed.

Final timing model change – Cyclone III LVDS maximum speed increase

The Cyclone III LVDS maximum speed clock frequency has been increased from 370 MHz to 402.5 MHz. This issue was fixed in the Quartus II software version 10.1.

Applies to: Cyclone III, C7 devices

Stratix IV and HardCopy IV incorrect VCM programming

For Stratix IV and HardCopy IV devices, prior to the release of the Quartus II software version 10.1, Altera incorrectly programmed the VCM (input common mode voltage) of dedicated HSSI refclk pins. The value of 0.82 V as the VCM was chosen, when the industry spec is 1.1 to 1.2 V. To use the previous setting, you must use the **.ini** file available from Altera.

Applies to: Stratix IV and HardCopy IV devices

Arria II GX incorrect timing delay values

Arria II GX devices with a speed grade of 6 exceed the maximum data rate specified in the device datasheet. In versions of the Quartus II software 10.0 and earlier, the data rate limit is not enforced during the compilation flow.

Applies to: Arria II GX devices

Final timing model change — Stratix III DDR input functional failure

Stratix III DDR input registers fail to capture edge-aligned input data correctly while the TimeQuest Timing Analyzer shows positive slack when you use the corner clock pin and corner PLL.

The final timing model was changed for Stratix III devices by updating the delay for a path from the corner clock pin to the corner PLL. Designs utilizing the affected path on the affected Stratix III parts must rerun the TimeQuest Timing Analyzer. If new timing violations occur, you must rerun the Fitter.

This issue was fixed in the Quartus II software version 10.0 SP1.

Applies to: Stratix III devices, including EP3SL200F1517, EP3SE260F1517, EP3SL340F1517, EP3SL340F1760

Cyclone IV GX incorrect megafunction setting

All High-Speed Serial Interface (HSSI) PLLs should have the operation mode set to **no_compensation**, except for CPRI with PLL phase frequency detector (PFD) feedback turned on when the feedback is set to **normal**. MPLLs 6 and 7 do not support **compensation** mode, but the altgx megafunction incorrectly sets the compensation mode to **normal** for CPRI with PFD turned off and duplex SDI design with reconfiguration turned on. The incorrect megafunction setting causes the placer to not use MPLL 6 or 7, which causes a no-fit.

For the design scenarios mentioned above, manually edit the generated altgx design file to modify the instance of the PLL operation mode to **no_compensation**.

Applies to: Cyclone IV GX devices

PCI Express Compiler cannot generate files for Gen1 protocol

The PCI Express Compiler v10.0 did not support IP and MegaWizard generation or regeneration of PCIe® Gen1 x4 or x8 designs targeting the Stratix IV and HardCopy IV device families.

For more information and solutions for this issue, refer to Knowledge Database solution *rd07012010_723*.

This issue is fixed in the Quartus II software versions 10.0 SP1 and later.

Applies to: Stratix IV and HardCopy IV devices

Cyclone IV GX incorrect simulation

In versions of the Quartus II software versions 10.0 and earlier, for Cyclone IV GX devices, when simulating a design containing an altlvds megafunction, an incorrect result could occur when the **Enable bitslip control** option was turned on.

Applies to: Cyclone IV GX devices prior to the Quartus II software version 10.1