Quartus II Software Version 10.1 Release Notes

This document provides late-breaking information about the following areas of the Altera® Quartus® II software version 10.1:

For information about disk space and system requirements, refer to the **readme.txt** file in your **altera/<*version number*>/quartus directory**. For information about device support in this version of the Quartus II software, along with the latest information about timing and power models, refer to the *Quartus II Device Support Release Notes*. For the latest information about the MegaCore® IP Library, refer to the *MegaCore IP Library Release Notes and Errata*. Both documents are available on the Altera website at http://www.altera.com/literature/lit-rn.jsp.

New Features & Enhancements

The Quartus II software version 10.1 includes the following new features and enhancements:

- The MegaWizard™ Plug-In Manager now supports the following megafunctions: ALTSQRT, LPM_ADD_SUB, LPM_COMPARE, LPM_CONSTANT, LPM_COUNTER, LPM_DIVIDE, LPM_MUX and LPM_SHIFTREG.
- The MegaWizard Plug-In Manager now supports the following new IP cores: Interlaken MegaCore function and Reed Solomon II MegaCore function.

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- The System Console includes a new External Memory Interface Debug Toolkit. You can use the External Memory Interface Debug Toolkit to connect to the DDR2 and DDR3 SDRAM controllers with UniPHY external memory interfaces in your design to diagnose the status of calibration and report margining. In addition, you can use this tool to produce a report of calibration and margining that you can share with Altera.
- The Quartus II software version 10.1 includes the following improvements to the Chip Planner:
  - Displays more detailed routing
  - Provides a **Locate History** dialog box that allows you to quickly traverse resources that you have located in the Chip Planner from other Quartus II software tools
  - Provides a **Properties** dialog box that provides detailed properties of resources you select
- You can now directly provide feedback to Altera. You can provide general feedback, report an issue, or make suggestions regarding the user interface and usability of the Altera Complete Design Suite.
- Quartus II Help can be used with the following browsers:
  - Local Quartus II Help (Help on a local drive installed by the Altera Installer) is fully compatible with Microsoft Internet Explorer 7 and Safari 4 running on Windows XP 32-bit operating systems. Local Quartus II Help is compatible with Google Chrome; however, you cannot open a Chrome browser from the Quartus II GUI; you must start Chrome with the `--allow-file-access-from-files flag` and then navigate to *<quartus installation directory>***/common/help/master.htm**. Local Quartus II Help can be used with Mozilla Firefox 2.0 running on Linux systems and Mozilla 3.5 running on Windows systems; however, some Help text display controls are not functional.
  - Quartus II web-based Help (hosted at http://quartushelp.altera.com/current) is fully compatible with Microsoft Internet Explorer 7, Safari 4, and Google Chrome. Quartus II Web Help can be used with Mozilla Firefox; however, some Help text display controls are not functional.
- The Qsys system integration tool is now available as beta for evaluation in the Quartus II software subscription edition version 10.1.

  CAUTION: Altera does not recommend using the beta release of Qsys in the Quartus II software version 10.1 for designs that are close to completion and are meeting design requirements.

  Before using Qsys, review "Qsys (Beta) Issues" in this document and *AN 632: SOPC Builder to Qsys Migration Guidelines* for known issues and limitations. For the latest known issues related to the beta version of Qsys, refer to *New Qsys Issues*. To submit general feedback or request technical support on the beta release of Qsys, submit a service request through **mysupport.altera.com**. Alternatively, to submit general feedback, click **Feedback** on the Quartus II software Help menu.

EDA Interface Information

The Quartus II software version 10.1 supports the following EDA tools:

Synthesis Tools	Version	NativeLink Support
Synopsys Synplify & Synplify Pro	C-2009.12	✓
Mentor Graphics® Precision RTL Synthesis	2010a	✓
Mentor Graphics LeonardoSpectrum™	2010a	✓
Mentor Graphics DK Design Suite	5.0 SP5	✓
Simulation Tools	**Version**	**NativeLink Support**
Mentor Graphics ModelSim®	6.6c	✓
Mentor Graphics ModelSim-Altera	6.6c	✓
Mentor Graphics ModelSim-Altera Starter Edition	6.6c	✓
Mentor Graphics QuestaSim	6.6c	✓
Cadence NC-Sim	9.2 (Linux only)	—
Synopsys VCS / VCS MX	2010.06 (Linux only)	✓
Aldec Active-HDL	8.3 (Windows only)	✓
Aldec Riviera-PRO	2010.10	✓
Formal Verification Tools (Equivalence Checking)	**Version**	**NativeLink Support**
Cadence Encounter Conformal	8.1	—
Chip Level Static Timing Analysis	**Version**	**NativeLink Support**
Synopsys PrimeTime	Z-2007.06	✓
Board Level Static Timing Analysis	**Version**	**NativeLink Support**
Mentor Graphics TAU		—
Board Level Symbol/Pin-out Management	**Version**	**NativeLink Support**
Mentor Graphics I/O Designer		—

Changes to Software Behavior

This section documents instances in which the behavior and default settings of this release of the Quartus II software have been changed from earlier releases of the software.

Refer to the Quartus II Default Settings File (**.qdf**), <*Quartus II installation directory*>**/quartus/bin/assignment_defaults.qdf**, for a list of all the default assignment settings for the latest version of the Quartus II software.

Items listed in the following table represent cases in which the behavior of the current release of the Quartus II software is different from a previous version.

Description	Workaround
Version 10.1	
The Classic Timing Analyzer is not provided in the Quartus II software beginning with version 10.1.	Use the Quartus II TimeQuest Timing Analyzer. For more information, refer to *Switching to the Quartus II TimeQuest Timing Analyzer*.
The TimeQuest Timing Analyzer no longer applies clock uncertainty to transfers involving the same physical launch and latch edge (that is, the latch and launch edges—rising or falling—are the same edge of a clock source and occur at the same time). Such transfers typically occur in hold analysis, but may also occur in setup analysis with a **Multicycle value** of **0**. This change in software behavior applies to all device families that support clock uncertainty.	
Sample waveforms are not provided in the MegaWizard Plug-In Manager.	
The `X_ON_VIOLATION` parameter is not provided with the `DFFEAS` primitive.	
The simulation model of the `DFFEAS` primitive in **altera_primitives.v** has been updated to improve performance; as a result, `d` and `clk` ports are no longer assigned to internal tristate buffers.	Connect `d` and `clk` ports, even if you expect these ports to be tristated `0`. For more information, refer to *Tribuf effects on simulation time and dffeas model changed* on the Altera Forums.
For designs that target the Cyclone IV GX device family, the ALTGX MegaWizard Plug-In Manager no longer provides an **85 Ohms** option under **What is the receiver termination resistance?** and **Select the transmitter termination resistance**.	Use **100 Ohms** or **150 Ohms**.
For the ALTFP_DIV, ALTFP_EXP, ALTFP_INV, ALTFP_INV_SQRT, ALT_FP_LOG, ALTFP_MULT, ALTFP_SQRT, ALTMULT_ACCUM, ALTMULT_ADD, ALTMULT_COMPLEX, ALTFP_MATRIX_INV, ALTFP_MATRIX_MULT, and LPM_MULT megafunctions, the MegaWizard Plug-In Manager no longer supports the Altera Hardware Description Language (AHDL). You can edit existing AHDL megafunction variations, but you cannot create new variations.	To create a new variation of a listed megafunction, use VHDL or Verilog HDL.

Known Issues & Workarounds

General Quartus II Software Issues

Issue	Workaround
Version 10.1	
If your computer display uses a dots per inch (DPI) setting greater than 96, the computer does not correctly display the Quartus II software GUI.	Use a DPI setting of 96.

Issue	Workaround
If your computer display has a screen resolution of 1024x768, not all of the DDR2 SDRAM CONTROLLER WITH UNIPHY, DDR2 SDRAM CONTROLLER WITH ALTMEMPHY, SERIAL LITE II, and CIC megafunctions can be displayed in the MegaWizard Plug-In Manager.	Change your screen resolution to a higher value.
If your computer display has a screen resolution of 1024x768, the horizontal scroll bar is not visible in the ALTPLL MegaWizard Plug-In Manager.	Change your screen resolution to a higher value or move the page to see the horizontal scroll bar.
If your computer display has a screen resolution of 1024x768, the SDI MegaWizard Plug-In Manager does not display a vertical scroll bar when resized.	Change your screen resolution to a higher value.
The Quartus II software supports `reg` and `logic` SystemVerilog keywords (and, for Verilog, `reg`) only to indicate the power-up value of a register. `reg` and `logic` are not supported for other purposes (for example, to pass a value to other hierarchies).	In contexts other than indicating the power-up value of a register, use `wire`. For more information, refer to *Recommended HDL Coding Styles* in volume 1 of the *Quartus II Handbook*.
The CUSTOM PHY megafunction is hidden in the Quartus II software version 10.1.	To see the CUSTOM PHY megafunction, download a Transceiver Toolkit sample design from On-chip Debugging Design Examples on the Altera website. Refer to the **readme.txt** file in the download for instructions to create a customized script to use with your project.
The LOW LATENCY PHY megafunction is hidden in the Quartus II software version 10.1.	To see the LOW LATENCY PHY megafunction, download a Transceiver Toolkit sample design from On-chip Debugging Design Examples on the Altera website. Refer to the **readme.txt** file in the download for instructions to create a customized script to use with your project.
The LOW LATENCY PHY megafunction does not support loopback modes.	
In the Transceiver Toolkit, if you use a LOW LATENCY PHY megafunction in PMA Direct mode and have more than one channel, the channels and links that are automatically generated function only for the first channel.	If you want to create more than one new transmitter channel, receiver channel, or transceiver link in PMA Direct mode, you must do so manually. To correctly address the transceiver settings, ensure that the generator and checker for the LOW LATENCY PHY megafunction is multiplied by four. In PMA Direct mode, when the phase compensation FIFO mode is set to None, the addressing scheme is 0, 4, 8, 12, and so forth; rather than the typical 0, 1, 2, 3, and so forth that is used in other modes. For example, if generator2 is connected to channel tx_parallel_data_2 with the LOW LATENCY PHY megafunction, you must set the channel tx_parallel_data_2 to channel tx_parallel_data_8 (channel 2 multiplied by four) for the transceiver settings to communicate on the correct channel.
In Mentor Graphics ModelSim-Altera version 6.6c, if your design exceeds the maximum number of untagged module or entity instances allowed (approximately 3000), it issues an error that incorrectly reports the number of instances in the design as zero: `**Warning: Design size of 0 instances exceeds ModelSim ALTERA recommended capacity.`	

Issue	Workaround
In the Chip Planner, if you attempt to create an atom in a design that targets an Arria GX, Arria II GX, Arria II GZ, Stratix II, Stratix II GX, Stratix III, or Stratix IV device by right-clicking a COMB node of an ALM and selecting **Create Atom**, the Chip Planner displays `Can't create node. Click the System tab on the Messages window for details.` However, the Messages window does not contain any details.	To create an atom for a COMB node of an ALM: 1. Select and right-click an empty FF of an ALM and then click **Create Atom**. 2. In the **Create Atom** dialog box, name the atom you created in step 1. 3. Select and right-click an empty COMB node of the same ALM and then click **Create Atom**. 4. In the **Create Atom** dialog box, name and specify the type of atom you created in step 3. 5. In the Change Manager window of the Chip Planner, select and right-click the atom you created in step 1, and then click **Restore Selected Change**. You can proceed to run **Check and Save all Netlist Changes** to verify these engineering changes.
The Quartus II software does not infer embedded memories for an internal clock crossing bridge FIFO buffer if its depth is too small, which can lead to setup timing violations.	Use an instance assignment to force inference of embedded memories for the FIFO buffer. For example, use `set_instance_assignment -name ALLOW_ANY_RAM_SIZE_FOR_RECOGNITION -to <design FIFO name>`

Platform-Specific Issues

Windows Platforms Only

Issue	Workaround
Version 10.1	
In the Text Editor, scrolling using a mouse wheel might not function correctly.	In Windows, change your Wheel settings: 1. Click the **Start** button, and then click **Control Panel**. 2. In the Control Panel window, click **Mouse**. 3. In the **Mouse Properties** dialog box, click the **Wheel** tab. 4. Under **Roll the wheel one notch to scroll**, select **The following number of lines at a time**.

Linux Platforms Only

Issue	Workaround
Version 10.1	
When viewing the Quartus II software with a remote client, the GUI can be difficult to read.	In the shell environment, set the following environment variable before you start the Quartus II software: `QUARTUSII_ENABLE_INTERNAL_ANTI_ALIASING=on`

Device Family Issues

Arria II GZ

Issue	Workaround
Version 10.1	
The ALTGX_RECONFIG MegaWizard Plug-In Manager incorrectly displays the `pre-tap` and second `post-tap` pre-emphasis ports in the ALTGX_RECONFIG megafunction. The Arria II GZ device family does not support `pre-tap` and second `post-tap` pre-emphasis settings.	Do not enable the `pre-tap` and second `post-tap` pre-emphasis ports.

Cyclone IV GX

Issue	Workaround
Version 10.1	
In the ALTGX MegaWizard Plug-In Manager, if you enter parameter information out of order, compilation might fail with an error similar to the following: `Error: Parameter "common_mode" of instance "transmit_pma0" has illegal value "0.6v" assigned to it. Possible parameter values are: "0.65V", "TRISTATE".`	Use the **Next** button to enter the settings in the correct order.
The SHIFT REGISTER (RAM-BASED) megafunction does not support MLAB or M512 memory blocks.	Use M9K blocks.
If you attempt to drive a PLL input with a low-speed clock (the `tx_clkout` port of ALTGX) for non-transceiver applications, the Quartus II software incorrectly prevents the connection and issues a message similar to the following: `Error: Port <port name> of <atom type> Atom <atom name> cannot be connected to <atom type> Atom <atom name>`	To drive a PLL input with a low-speed clock (the `tx_clkout` port of ALTGX) for non-transceiver applications, refer to the solution available at: http://www.altera.com/support/kdb/solutions/rd12132010_299.html

MAX

Issue	Workaround
Version 10.1	
If your design includes a D flipflop (DFF), the Design Assistant issues an error similar to the following: Internal Error: Sub-system: DRC, File: `/quartus/tsm/drc/drc_tdb_netx.cpp, Line: 6270`	Turn off the Design Assistant; on the **Design Assistant** page of the **Settings** dialog box, turn off **Run Design Assistant during compilation**.

MAX V

Issue	Workaround
Version 10.1	
If you select **MAX V** in the **Family** box of **Device** dialog box, the **Devices** box contains two options: **MAX V Z** and **All**. However, only the **All** option is valid.	In the **Devices** box, do not use the `MAX V Z` option. Select **All**.
If your design includes a D flipflop (DFF), the Design Assistant issues an error similar to the following: Internal Error: Sub-system: DRC, File: `/quartus/tsm/drc/drc_tdb_netx.cpp, Line: 6270`	Turn off the Design Assistant; on the **Design Assistant** page of the **Settings** dialog box, turn off **Run Design Assistant during compilation**.
In the MegaWizard Plug-In Manager, AHDL is not supported for the MAX V OSCILLATOR, ALTUFM_I2C, ALTUFM_NONE, ALTUFM_PARALLEL, or ALT_UFM_SPI megafunctions. Attempting to synthesize one of these AHDL megafunctions in the Quartus II software fails with an error similar to the following: `Error: Can't open AHDL Include File maxv_ufm.inc`	Use VHDL or Verilog HDL.
Behavioral simulation of an ALTLVDS_TX megafunction is not supported.	Use gate-level simulation.

Stratix II GX

Issue	Workaround
Version 10.1	
In the ALT2GXB MegaWizard Plug-In Manager, on the **General** page of the **Parameter Settings** tab, if you attempt to change **What protocol will you be using?** from **Basic** to **XAUI**, the MegaWizard Plug-In Manager incorrectly selects **CPRI**. If you then attempt to change the setting from **CPRI** to **XAUI**, the MegaWizard Plug-In Manager closes.	To successfully select the XAUI protocol: 1. In the **Which protocol with you be using?** box, select **XAUI**. The **CPRI** protocol is incorrectly displayed. 2. In the **Which protocol will you be using?** box, select **Basic**. The **Basic** protocol is displayed. 3. In the **Which protocol will you be using?** box, select **XAUI**. The **XAUI** protocol is now correctly selected.
If your ALT2GXB instance has a word alignment pattern length of 20 bits, on the **Basic 2** page of the ALT2GXB MegaWizard Plug-In Manager, the number displayed in the **What is the word alignment pattern length?** box of the **Protocol Settings** tab is **10** and the pattern displayed in the **What is the word alignment pattern?** box is truncated to 10 bits.	Before making any other changes to your ALT2GXB instance, in the ALT2GXB MegaWizard Plug-In Manager, set **What is the word alignment pattern length?** to **20** and copy the word alignment pattern from your HDL file to the **What is the word alignment pattern?** box.

Stratix IV GX

Issue	Workaround
Version 10.1	
In an ALTGX megafunction, reconfiguration of a clock multiplier unit (CMU) PLL might fails if the CMU PLL drives a transmitter channel using a central clock divider through X4/XN and either ■ The transceiver channel is in bonded mode configuration, or ■ The **Use central clock divider to drive the transmitter channels using X4/XN lines** option on the **Main PLL** page of the **Reconfiguration Settings** tab is on.	Set location assignments to place the CMU PLL that drives a transceiver channel using a central clock divider at location CMU0 PLL.
In an ALTGX megafunction, reconfiguration of a clock multiplier unit (CMU) PLL might cause functional failures if the transmitter channel in the same block is driven by a CMU PLL placed at location CMU1 PLL and the **Use central clock divider to drive the transmitter channels using X4/XN lines** option on the **Main PLL** page of the **Reconfiguration Settings** tab is on.	Set location assignments to place the CMU PLL that drives a transceiver channel using a central clock divider at location CMU0 PLL.
In the ALTGX MegaWizard Plug-In Manager, on the **Modes** page of the **Reconfiguration Settings** tab, if you turn on **Enable Channel and Transmitter PLL reconfiguration** and **Use additional CMU/ATX Transmitter PLLs from outside the Transceiver block**, set **How many additional PLLs are used?** to **2** or **3**, and then on the **Main PLL** page turn on **Use central clock divider to drive the transmitter channels using X4/XN lines**, **clearbox.exe** generates an error: `clearbox.exe has encountered a problem and needs to close. We are sorry for the inconvenience.`	Before you turn on **Use central clock divider to drive the transmitter channels using X4/XN lines**, on the **PLL 2 page**, change **What is the PLL logical reference index (used in reconfiguration)?** from **2** to **3**.
In the LOW LATENCY PHY megafunction, the **10G** option is not available.	Do not use the **10G** option.

Stratix V

Issue	Workaround
Version 10.1	
In the Pin Planner, the Live I/O Check feature is not supported. Attempting to run Live I/O Check fails with an error similar to the following: `Internal Error: Sub-system CUT, FileL /quartus/db/cut/cut_generic_pll_group.cpp, Line:298`	

If you attempt to use the Cadence Encounter Conformal software for formal verification of **altddio_out.v**, **altlvds_tx.v**, **altlvds_rx.v**, **lvds_tx.v**, **lvds_rx.v**, **flvds_tx.v**, **flvds_rx.v**, **altmult_add.v**, **altmult_accum.v**, or **altpll.v**, formal verification fails with the error: `Error RTL 18.3: Function call does not refer to function definition`	
The CUSTOM PHY megafunction does not support VHDL simulation with Cadence NC-Sim.	
The CUSTOM PHY MegaWizard Plug-In Manager does not prevent illegal combinations of **Data rate** and **Input clock frequency**. If you enter illegal an illegal combination, during compilation, the Quartus II software might generate messages similar to the following: `Warning: altera_xcvr_custom_phy: Simulation libraries for Mentor simulators may not be present`	The Data rate should be a minimum of **622 Mbps** and a maximum of **6.5 Gbps**.

The CUSTOM PHY MegaWizard Plug-In Manager might display the following messages:
`Warning: altera_xcvr_custom_phy: Simulation libraries for Mentor simulators may not be present.`
`Warning: altera_xcvr_low_latency_phy: Simulation libraries for Mentor simulators may not be present.`
	These warnings are caused by missing encrypted Stratix V component Verilog files, which are not required.
	You may safely ignore these messages.

In a Tx-only Serial Advanced Technology Attachment (SATA) transceiver interface generated by the Custom PHY MegaWizard Plug-In Manager, output from a `tx_serial_data` port is undefined because the `tx_forcelecidle` driver is missing.	
The byte ordering feature of the CUSTOM PHY megafunction is subject to incorrect behavior.	
Simulation of 10GBASE-R PHY, CUSTOM PHY, INTERLAKEN, LOW LATENCY PHY, PCI EXPRESS, PCI EXPRESS PIPE, and XAUI megafunctions fails if you use ModelSim with mixed languages.	Turn off ModelSim optimization with the `-novpt` option of the `vsim` command.
For the ALTMULT_ACCUM, ALTMULT_ADD, and ALTMULT_COMPLEX megafunctions, the MegaWizard Plug-In Manager does not support VHDL.	Use Verilog HDL.

During generation of a 10GBASE-R PHY, XAUI PHY, CUSTOM PHY, or LOW LATENCY PHY megafunction, the MegaWizard Plug-In Manager generates an error similar to the following: `Warning: altera_10gbaser_phy: Simulation libraries for Mentor simulators may not be present`	You may safely ignore this message.
If you attempt to instantiate a x-1 LOW LATENCY PHY megafunction that uses 10GB PCS and more than six channels, fitting fails because the PLL cannot drive more than six channels. The Fitter generates messages similar to the following: `Error: Could not place ATX PLL hsl2_rev1:inst24|altera_xcvr_low_latency_phy:hsl2_rev1_inst|alt_pma:alt_pma_inst|alt_pma_sv:alt_pma_sv_inst|altera_xcvr_10g_custom:altera_xcvr_10g_custom_inst|pll[0].tx_pll~LC_PLL`	Instantiate a x-1 design for one channel, and then repeat the instantiation to meet the number of channels you require.

SOPC Builder Issues

Issue	Workaround
Version 10.1	
SOPC Builder requires Cyclone IV GX device information during system generation. If Cyclone IV GX device information is not installed with the Quartus II software version 10.1, system generation fails with the following error: `Family name "Cyclone IV GX" is illegal`	Install Cyclone IV GX device family to the Quartus II software.
In the **Custom Instructions** tab, SOPC Builder might display the same custom instruction multiple times.	Each displayed custom instruction refers to the same underlying custom instruction. You can safely choose any of the displayed instructions.

Qsys (Beta) Issues

The Qsys system integration tool is available as beta for evaluation in the Quartus II software subscription edition version 10.1.

CAUTION

Altera does not recommend using the beta release of Qsys in the Quartus II software version 10.1 for designs that are close to completion and are meeting design requirements.

Before using Qsys, review this Qsys (Beta) Issues section and *AN 632: SOPC Builder to Qsys Migration Guidelines* for known issues and limitations. For the latest known issues related to the beta version of Qsys, refer to *New Qsys Issues*. To submit general feedback or request technical support on the beta release of Qsys, submit a service request through **mysupport.altera.com**. Alternatively, to submit general feedback, click **Feedback** on the Quartus II software Help menu.

Issue	Workaround
Version 10.1	
Qsys does not support all Altera IP megafunctions. For example, Qsys does not support the 10GBASE-R PHY, ASI, CPRI, FFT, FIR COMPILER, PCI EXPRESS, REED SOLOMON, VITERBI, and XAUI PHY megafunctions.	Use the MegaWizard Plug-In Manager or SOPC Builder (if supported). For a complete list of IP megafunctions supported by Qsys, refer to the **Component Library** tab in the Qsys GUI.
Qsys requires Cyclone IV GX device information during system generation. If Cyclone IV GX device information is not installed with the Quartus II software version 10.1, system generation fails with the following error: `Family name "Cyclone IV GX" is illegal`	Install the Cyclone IV GX device family to the Quartus II software.
Qsys does not generate a simulation model in VHDL, and the **Create VHDL simulation model** option on the **Generate** tab is unavailable.	To simulate a Qsys system, use a Verilog simulation model and Verilog simulator.
Qsys does not generate a simulation testbench file, and the **Create testbench Qsys system and testbench Verilog simulation model** on the **Generate** tab is unavailable.	Create your testbench manually, or modify a testbench generated by SOPC Builder and instantiate the Qsys system under test. Refer to the template on the **HDL Example** tab for a sample instantiation of the system.
Changes to the **Export As** column made immediately before saving a system are not saved.	After you click in the **Export As** column, press Enter or click elsewhere in the GUI. You can refer to the **HDL Example** tab to verify the signals exported from the system.
Changes made from outside the Qsys GUI to a subsystems or components are not immediately reflected in the Qsys GUI.	To read changes made from outside the Qsys GUI to a subsystem or component, on the Qsys File menu, select **Refresh System** or press F5.
Generating a large Qsys system with many instances, or generating a system multiple times in a single Qsys session might cause memory problems. These memory problems can result in an error message similar to the following: `Error writing sopcinfo report java.lang.OutOfMemoryError: Java heap space`	Close Qsys and reopen it to clear the memory. To generate a large system, use the command-line `ip-generate` options.

Issue	Workaround
The Nios II Software Build Tools (SBT) for Eclipse do not support the Run as ModelSim simulation flow to simulate Nios II software code with Qsys systems.	Run your simulation outside the Eclipse environment. You can use the generated ModelSim **script mti_setup.tcl** as an example for your testbench and simulation environment. To simulate a Nios II processor running software code, you must generate a Nios II Memory Initalization File (**.mif**). To generate the **.mif** file: 1. In Eclipse, right-click the application project, point to **Make Targets**, and then click **Build**. 2. Select **mem_init_install** and then click **Build**. For the latest simulation recommendations, refer to *New Qsys Issues*.
Memory initialization does not function correctly if an on-chip memory (RAM or ROM) component has **Initialize memory content** turned on and **Enable non-default initialization file** turned off.	Turn on **Enable non-default initialization file** and specify the name of the memory instance.
Qsys does not support legacy SOPC Builder PLL components, except those with an input frequency of 50 MHz. Generating a design that includes a legacy PLL with an input frequency not set to 50 MHz fails with an error similar to the following: `Error: altera_avalon_pll_khh3cm2h: CLock yyclock_inclk0 of frequency 50.000 MHz driving the PLL module conflicts with the PLL inclock of frequency 125.000 MHz.`	If you want to configure a PLL with an input frequency other than 50 MHz, replace the SOPC Builder PLL with an Avalon ALTPLL.
In Avalon Tristate Conduit Interfaces, shared signal name assignments in the Tristate Conduit Pin Sharer might become invalid if signals are later added or removed from Generic Tristate Controllers or there is a change to Tristate Conduit Pin Sharer connectivity.	Declare signal sharing in the Tristate Conduit Pin Sharer only after completely parameterizing the Generic Tristate Controllers and connecting them to the Tristate Conduit Pin Sharer.
SOPC Builder drivers for Avalon Memory-Mapped (MM) Tristate components are not automatically upgraded in Qsys.	To transfer the required driver assignments to an upgraded Generic Tristate Controller, on the **System** menu, select **Run Qsys Upgrade Transforms**. Then, in the Generic Tristate Controller GUI, enter `embeddedsw.configuration.softwareDriver` in the **Key** column of the **Module Assignments** table and enter the driver name in the **Value** column.
The legacy altera_avalon_lan9c111 component is not available in Qsys and the software driver is not automatically upgraded in Qsys.	If you have an existing SOPC Builder design with an altera_avalon_lan9c111 component, you can migrate the design to the Qsys Generic Tristate Controller. To transfer the required driver assignments to an upgraded Generic Tristate Controller, on the **System** menu, select **Run Qsys Upgrade Transforms**. Then, in the Generic Tristate Controller GUI, enter `embeddedsw.configuration.softwareDriver` in the **Key** column of the **Module Assignments** table and enter `altera_avalon_lan9c111_hal_driver` in the **Value** column.

Issue	Workaround

If you generate the simple socket server and web server Nios II example designs that contain tristate components, the Nios II Software Build Tools for Eclipse generates errors similar to the following:
`[Error ] 'EXT_FLASH_BASE' undeclared`
`[Error ] 'EXT_FLASH_BASE' undeclared`
	In the **network_utilities.c** file, on lines 213 an 419 change
	`EXT_FLASH_NAME`
	to
	`AV_TRI_S1_EXT_FLASH_0_NAME`
	and on line 290 change
	`EXT_FLASH_BASE`
	to
	`AV_TRI_S1_EXT_FLASH_0_BASE`

For Nios II processor vectors, Qsys performs an upgrade transformation on legacy tristate components. If you have assigned vectors to tristate components, Qsys might generate errors similar to the following: `[Error ] System.cpu: "Reset vector memory" (resetSlave) out of range`	Reassign the vectors to the updated tristate memory names.
If you use Qsys upgrade transforms to migrate a Common Flash Interface (CFI) memory component (altera_avalon_cfi_flash), which requires a Nios II software driver with initialization, the Board Support Package (BSP) does not correctly specify the required driver. Although the BSP compiles and no error message is issued, the component does not function correctly.	Instantiate the legacy Flash Memory Interface (CFI) component (altera_avalon_cfi_flash). To transfer the required driver assignments to an upgraded Generic Tristate Controller: 1. On the **System** menu, select **Run Qsys Upgrade Transforms**. 2. In the Generic Tristate Controller GUI, enter `embeddedsw.configuration.softwareDriver` in the **Key** column of the **Module Assignments** table and enter `altera_avalon_flash_driver` in the **Value** column. 3. Modify the **alt_sys_init.c** file created during BSP generation by following these steps: a. In the Device Headers section, change the include statement from `altera_generic_tristate_controller.h` to `altera_avalon_cfi_flash.h`. b. In the Device Storage section, change `ALTERA_GENERIC_TRISTATE_CONTROLLER_INSTANCE (<instance_name_caps>, <instance_name>)` to `ALTERA_AVALON_CFI_FLASH_INSTANCE (<instance_name_caps>, <instance_name>)`. In the `alt_sys_init` function, change `ALTERA_GENERIC_TRISTATE_CONTROLLER_INIT (<instance_name_caps>, <instance_name>)` to `ALTERA_AVALON_CFI_FLASH_INIT (<instance_name_caps>, <instance_name>)`.

Issue	Workaround
If your system includes a custom component that requires a Nios II software driver with initialization, the driver might not be found and the Board Support Package might fail to compile with errors about missing identifiers and assignments. Components are affected if the **_sw.tcl** file sets the property "`set_sw_property auto_initialize true`" to **request alt_sys_init.c** initialization.	Instantiate the custom component in SOPC Builder and then open the system in Qsys. To transfer the required driver assignments to an upgraded Generic Tristate Controller, on the **System** menu, select **Run Qsys Upgrade Transforms**. Then, in the Generic Tristate Controller GUI, enter `embeddedsw.configuration.softwareDriver` in the **Key** column of the **Module Assignments** table and, in the **Value** column, enter the driver name that is listed in the component's **_sw.tcl** file. You might need to add an entry into the `alt_irq_init` function, depending on the exact requirements of the component's driver. You might also need to add additional driver-specific header files to the Device Headers section.
If you instantiate a Generic Tristate Controller for CFI in Qsys (which requires a Nios II software driver with initialization) the Board Support Package fails to compile with errors regarding missing identifiers and assignments.	Modify the **alt_sys_int.c** file created during BSP generation by following these steps: 1. In the Device Headers section, change the include statement from `altera_generic_tristate_controller.h` to `altera_avalon_cfi_flash.h`. 2. In the Device Storage section, change `ALTERA_GENERIC_TRISTATE_CONTROLLER_INSTANCE (<instance_name_caps>, <instance_name>)` to `ALTERA_AVALON_CFI_FLASH_INSTANCE (<instance_name_caps>, <instance_name>)`. In the `alt_sys_init` function, change `ALTERA_GENERIC_TRISTATE_CONTROLLER_INIT (<instance_name_caps>, <instance_name>)` to `ALTERA_AVALON_CFI_FLASH_INIT (<instance_name_caps>, <instance_name>)`
Designs that use the Generic Tristate Controller component without a Tristate Conduit Pin Sharer might become unresponsive in hardware and in simulation. Tristate conduit masters do not function correctly because the controller loops back the request signal onto the grant signal. An affected system generates messages similar to the following: `Warning: Found combinational loop of 8 nodes.`	Add a Tristate Conduit Pin Sharer component between the tristate conduit bridge and any tristate conduit controllers, even if no pins require sharing.
Connecting a tristate conduit pin sharer output interface to its input interface causes the GUI to become unresponsive.	You cannot connect a tristate conduit pin sharer to itself.
Qsys does not support components that have the module property `INSTANTIATE_IN_SYSTEM_MODULE` set to `FALSE`. Qsys does not export to the top level interfaces of modules that are not instantiated in the system to the top level.	To manually export the interface of a module that is not instantiated in Qsys to the top level: 1. Create a wrapper HDL file. 2. Map one half of the wrapper to Avalon-compliant interfaces, and the other half to a conduit. 3. Manually export the conduit by specifying the exported name in the **Export As** column in Qsys.

Issue	Workaround
The Avalon-MM `arbiterlock` signal is not supported.	For all Avalon-MM masters that use `arbiterlock`, add burst capabilities to the master and set the burst count according to the duration of arbiter lock required. For example, replace an arbiter locked transaction of 16 accesses with a burst transaction using a burst count of 16.
Slaves wider than the master might receive illegal byteenable combinations during burst transactions.	Ensure that the bursting master performs accesses aligned to the slave word size. For example, if a 32-bit master accesses a 128-bit slave, ensure that the master accesses offsets in the slave address space that are multiples of 16 bytes.
If an Avalon Memory-Mapped (MM) master writes to an Avalon-MM slave that does not have a byte enable input signal and has a wider data width than the master, data corruption might occur on the slave words.	Add a byte enable signal to any slave that has a wider data width than its master.
When converting an SOPC Builder system with more than one clock source to Qsys, the generated Qsys system has multiple reset inputs—one for each clock source—even if the **Use SOPC Builder port naming** option on the **Project Settings** tab of the Qsys GUI is turned on.	In the top level of your design, connect all reset inputs generated by Qsys to the same reset source.
Designs coverted from SOPC Builder that use pipeline and clock crossing bridges with bursts disabled and data widths other than 32 bits have incorrect **Maximum burst size** values.	Change the **Burstcount width** value and, if applicable, the **Burstcount units** value, so that the **Maxiumum burst size** value in the GUI displays **1** (nonbursting).
Quartus II Archive Files (**.qar**) do not automatically include Qsys input files such as Qsys System Files (**.qsys**) and the source files for custom components defined in the system.	To include the Qsys input files in the **.qar** file, on the Project menu, select **Add/Remove Files in Project**, browse to the files, and then click **Open**.

For designs that include ALTMEMPHY, the *<memory controller name><random string>*_**pin_assignments.tcl** file generated by Qsys does not assign correct pin names. Running the Tcl file immediately after generation results in incorrect pin assignments.	After you generate your design and before you run the Tcl script, open the Tcl file and change the line
	`set instance_name "<memory controller name>_<random string>"`
	to
	`set instance_name "<memory controller name>"`

Attempting to import an SOPC Builder design that contains an ALTMEMPHY-based memory controller to Qsys fails and Qsys displays a message similar to the following: `Exception during validation: altera.util.UnsupportedDeviceFamily Unsupported device family: unknown.`	Re-create the system in Qsys.
If you simulate an ALTMEMPHY-based megafunction as part of a Qsys system, the simulator might generate the following error: `Instantiation of 'stratixiii_ddio_in' failed`	Add the following global assignment to the Quartus II IP File (**.qip**) generated by Qsys: `set_global_assignment -name EDA_DESIGN_EXTRA_ALTERA_SIM_LIB stratixiii -section_id eda_simulation`

Issue	Workaround

For components that use the deprecated Memory-Mapped flow control, Qsys issues warnings during generation. For the Altera Avalon JTAG UART component, Qsys generates the following messages:
`Warning: "No matching role found for jtag_uart_0:avalon_jtag_slave:dataavailable (dataavailable)"`
`Warning: "No matching role found for jtag_uart_0:avalon_jtag_slave:readyfordata (readyfordata)"`
For the DMA Controller component, Qsys generates the following messages:
`Warning: "No matching role found for dma_0:write_master:write_endofpacket (endofpacket)"`
`Warning: "No matching role found for dma_0:read_master:read_endofpacket (endofpacket)"`
`Warning: "No matching role found for dma_0:read_master:read_flush (flush)"`
`Warning: "No matching role found for dma_0:control_port_slave:dma_ctl_readyfordata (readyfordata)"`
	You may safely ignore these messages because the signals are not required for design operation.

Module (or entity) names and file names generated by Qsys for each component instance are dependent on parameter settings. If you change the parameters of a component and then regenerate synthesis or simulation files, a new file is generated with a different entity, module, and file name. The file from any previous parameterization is not removed from the output directory.	Avoid defining assignments or scripts that depend on a component's module or entity name. Instead, rely on your component instance name. If your IP or component generates any files (such as Tcl scripts) that must be run after generation, be sure that you use the latest generated file to reflect the most recent parameterization. If you do not need older generated files, you may delete them from your output directory.
If, on the **Project Settings** tab, **Global reset** is turned off, a transaction can be issued from a component in a reset domain that is not currently reset to a domain that is currently in reset. The transaction might be accepted by the interconnect logic within the domain that is currently in reset. The result is system-dependent, but can include system lockup—the transaction appears to have been accepted, but actually is ignored.	Carefully control reset deassertion sequencing among multiple reset domains and ensure that transactions are not issued across reset domain boundaries when some reset domains are in reset but others are not in reset.
If you generate a design that contains a Nios II processor, Qsys might generate messages similar to the following: `Generation callback did not provide a top level file. Found altera_nios2_qsys_<random character>.v in output directory - callback must 'add_file $output_dir/altera_nios2_qsys_<random character>.v {SIMULATION SYNTHESIS}`	You may safely ignore these messages.

Issue	Workaround
If you simulate a Qsys design that includes an the EPCS Serial Flash Controller, simulation displays messages similar to the following: `Error: Overwriting different file */altera_avalon_epcs_flash_controller_*_boot_rom.hex file`	You may safely ignore this message. Replace each ***/altera_avalon_epcs_flash_controller_*_boot_rom.hex** file with the generated files from the **elf2hex/elf2dat** directory during memory initialization file preparation.
Qsys does not support the **Controller shares dq/dqm/addr I/O pins** option of the SDRAM Controller. Attempting to use an SDRAM Controller with **Controller shares dq/dqm/addr I/O pins** turned on results in an error similar to the following: `Error: sdram_0: Invalid tristate bridge selection for pin-sharing. Please parameterize the SDRAM to resolve this issue.`	On the **Memory Profile** page of the **Parameter Settings** tab of the SDRAM Controller Parameter Editor, turn off **Controller shares dq/dqm/addr I/O pins**.

Antivirus Verification

The Altera Complete Design Suite version 10.1 has been verified virus-free using the following software:

McAfee VirusScan Enterprise + AntiSpyware Enterprise 8.7.0i
Scan Engine Version: 5400.1158
DAT Version: 6174.0000

Latest Known Quartus II Software Issues

For more information about known software issues, look for information on the **Quartus II Software Support** page at the following URL:

http://www.altera.com/support/software/sof-quartus.html

For the latest known issues related to the beta version of Qsys, refer to the New Qsys Issues wiki page at the following URL:

http://www.alterawiki.com/wiki/New_Qsys_Issues

You can find known issue information for previous versions of the Quartus II software on the Knowledge Database page at the following URL:

http://www.altera.com/support/kdb/kdb-index.jsp

Software Issues Resolved

The following Customer Service Requests were fixed or otherwise resolved in the Quartus II software version 10.1:

Customer Service Request Numbers Resolved in the Quartus II Software Version 10.1							
10456560	10551928	10596802	10620510	10624158	10638364	10642774	10649102
10650882	10654269	10656631	10657086	10657337	10662357	10662391	10665466
10668236	10671172	10671421	10672796	10673957	10674414	10674824	10679540
10680271	10680995	10684200	10684689	10684764	10688025	10691878	10692851

Customer Service Request Numbers Resolved in the Quartus II Software Version 10.1							
10693773	10697479	10698132	10698980	10700162	10703578	10704527	10704643
10705047	10708891	10711536	10711675	10712456	10713750	10714541	10716896
10718354	10718766	10720096	10720566	10721121	10721152	10721479	10724991
10725128	10725906	10726382	10727667	10727694	10727786	10728635	10729172
10729208	10729208	10729358	10729604	10730594	10731127	10731344	10731809
10733115	10733122	10733123	10733329	10734366	10734595	10735065	10735456
10735651	10735674	10735750	10736295	10736580	10736838	10737206	10738239
10738665	10739037	10739339	10739558	10739563	10739803	10740468	10740732
10740984	10741596	10741709	10742241	10743422	10743610	10743837	10743893
10744106	10744151	10744481	10745382	10745405	10745842	10746208	10746400
10746467	10746759	10746960	10747006	10747020	10747763	10748137	10748214
10748229	10749173	10749208	10749426	10749489	10749492	10749842	10749881
10750406	10750562	10750619	10750661	10750782	10751047	10751202	10751245
10751292	10751552	10751803	10751824	10751852	10751886	10752200	10752343
10752696	10752855	10753015	10753159	10753865	10753969	10754026	10754105
10754112	10754476	10754506	10754528	10754552	10754606	10754771	10754894
10754894	10754911	10755083	10755124	10755320	10755336	10755389	10755533
10755729	10755739	10755885	10755913	10755961	10756073	10756134	10756289
10756394	10756553	10756593	10756596	10756668	10756747	10756782	10756806
10757217	10757227	10757272	10757502	10757549	10757551	10757841	10757880
10757908	10758235	10758666	10758679	10758718	10758835	10759089	10759102
10759182	10759237	10759292	10759336	10759451	10759547	10759553	10759629
10760108	10760121	10760741	10760764	10760776	10760795	10760803	10760815
10760860	10761178	10761349	10761417	10761643	10761833	10761852	10762026
10762087	10762180	10762273	10762306	10762423	10762477	10762478	10762797
10762983	10762985	10763234	10763377	10763451	10763458	10763498	10763581
10763587	10763666	10763759	10763801	10763851	10763871	10763943	10763944
10764006	10764031	10764195	10764265	10764309	10764362	10764643	10764661
10764698	10764699	10764703	10764719	10764720	10764793	10764863	10765002
10765023	10765096	10765114	10765192	10765307	10765324	10765591	10765593
10765653	10765712	10765718	10765797	10765827	10765852	10765879	10765972
10766032	10766217	10766303	10766392	10766596	10766615	10766666	10766811

Customer Service Request Numbers Resolved in the Quartus II Software Version 10.1							
10766985	10767040	10767080	10767106	10767123	10767144	10767285	10767292
10767455	10767503	10767615	10767627	10767628	10767638	10767663	10767671
10767672	10767800	10767854	10767856	10767958	10768050	10768058	10768221
10768266	10768276	10768278	10768289	10768346	10768466	10768468	10768512
10768540	10768548	10768659	10768672	10768724	10768730	10768739	10768741
10768752	10768781	10768784	10768916	10768922	10768963	10768966	10768982
10769033	10769041	10769054	10769179	10769213	10769214	10769249	10769261
10769358	10769382	10769407	10769470	10769561	10769658	10769771	10769786
10769787	10769810	10769878	10769883	10769970	10769985	10769987	10770007
10770011	10770012	10770015	10770035	10770058	10770072	10770091	10770113
10770173	10770237	10770284	10770293	10770298	10770304	10770305	10770317
10770366	10770389	10770393	10770429	10770492	10770508	10770524	10770529
10770603	10770611	10770700	10770734	10770736	10770755	10770765	10770784
10770790	10770812	10770839	10770876	10770942	10770948	10771078	10771142
10771151	10771154	10771197	10771234	10771275	10771308	10771320	10771373
10771377	10771395	10771396	10771408	10771412	10771432	10771433	10771440
10771472	10771481	10771527	10771611	10771636	10771638	10771658	10771660
10771667	10771677	10771689	10771695	10771732	10771845	10771849	10771858
10771862	10771875	10771885	10771888	10771897	10772031	10772034	10772076
10772086	10772103	10772119	10772134	10772136	10772194	10772308	10772321
10772346	10772462	10772473	10772482	10772486	10772491	10772495	10772496
10772653	10772671	10772702	10772718	10772726	10772731	10772732	10772802
10772866	10772918	10773045	10773090	10773094	10773194	10773223	10773278
10773306	10773380	10773385	10773406	10773408	10773409	10773444	10773482
10773548	10773569	10773582	10773622	10773673	10773733	10773824	10773861
10773864	10773958	10773991	10774000	10774007	10774065	10774068	10774133
10774140	10774144	10774158	10774189	10774219	10774227	10774306	10774344
10774353	10774383	10774414	10774471	10774512	10774532	10774584	10774655
10774711	10774789	10774798	10774945	10774989	10775013	10775023	10775083
10775117	10775139	10775263	10775353	10775360	10775362	10775392	10775512
10775513	10775516	10775553	10775598	10775624	10775626	10775639	10775677
10775775	10775783	10775833	10775944	10776002	10776011	10776019	10776044

Customer Service Request Numbers Resolved in the Quartus II Software Version 10.1							
10776089	10776106	10776114	10776156	10776219	10776228	10776294	10776350
10776450	10776483	10776528	10776541	10776577	10776611	10776666	10776669
10776751	10776760	10776825	10776840	10776902	10777030	10777032	10777051
10777061	10777070	10777094	10777107	10777112	10777144	10777155	10777184
10777202	10777208	10777236	10777240	10777248	10777289	10777347	10777391
10777403	10777421	10777446	10777460	10777463	10777491	10777503	10777518
10777636	10777647	10777739	10777784	10777810	10777876	10777888	10777902
10777909	10778000	10778025	10778026	10778044	10778170	10778198	10778210
10778264	10778266	10778392	10778406	10778432	10778449	10778453	10778519
10778676	10778696	10778736	10778754	10778949	10778956	10778968	10779024
10779048	10779049	10779203	10779231	10779280	10779281	10779355	10779378
10779442	10779455	10779491	10779534	10779594	10779595	10779610	10779773
10779886	10779936	10779948	10780029	10780085	10780124	10780136	10780224
10780289	10780352	10780384	10780520	10780523	10780536	10780596	10780665
10780672	10780805	10780841	10780940	10780977	10780993	10781130	10781133
10781196	10781216	10781382	10781435	10781439	10781453	10781555	10781639
10781745	10781779	10781938	10781973	10782040	10782041	10782061	10782151
10782169	10782397	10782413	10782429	10782507	10782519	10782880	10783067
10783143	10783166	10783221	10783311	10783312	10783425	10783582	10783722
10783803	10783950	10783991	10784146	10784194	10784261	10784299	10784335
10784495	10784516	10784538	10784547	10784645	10784713	10784723	10784726
10784768	10784805	10784867	10784951	10785064	10785115	10785440	10785571
10785613	10785752	10785789	10786359	10786367	10786426	10786682	10787808
10788784	—	—	—	—	—	—	—

Software Patches Included in this Release

The Quartus II software version 10.1 includes the following patches released for previous versions of the Quartus II software:

Quartus II Software Version	Patch	Customer Service Request Number
10.0 SP1	1.178	10786049
10.0 SP1	1.174	10771689
10.0 SP1	1.173	10779594

Quartus II Software Version	Patch	Customer Service Request Number
10.0 SP1	1.172	10773431, 10779259
10.0 SP1	1.166	10781435
10.0 SP1	1.165	—
10.0 SP1	1.162	10771689
10.0 SP1	1.161	10777421
10.0 SP1	1.16	10779048
10.0 SP1	1.159	10782758
10.0 SP1	1.158	10778044
10.0 SP1	1.157	10776450
10.0 SP1	1.156	10779936
10.0 SP1	1.155	10781973
10.0 SP1	1.154	10777460
10.0 SP1	1.152	10779886
10.0 SP1	1.15	10779355
10.0 SP1	1.148	10777446
10.0 SP1	1.147	10778406
10.0 SP1	1.146	10777888
10.0 SP1	1.145	10777984
10.0 SP1	1.144	10781573
10.0 SP1	1.143	10773431, 10775003, 10779259
10.0 SP1	1.142	10779048
10.0 SP1	1.141	10745382, 10751336
10.0 SP1	1.14	10777051
10.0 SP1	1.139	10779048
10.0 SP1	1.138	10770304
10.0 SP1	1.136	10778170
10.0 SP1	1.135	10780136
10.0 SP1	1.134	10757551
10.0 SP1	1.133	10777463
10.0 SP1	1.132	10776669
10.0 SP1	1.131	10778432
10.0 SP1	1.13	10774827

Quartus II Software Version	Patch	Customer Service Request Number
10.0 SP1	1.129	—
10.0 SP1	1.128	10777965
10.0 SP1	1.126	10777784
10.0 SP1	1.124	—
10.0 SP1	1.122	10772462
10.0 SP1	1.121	10771078
10.0 SP1	1.12	10775139
10.0 SP1	1.119	10774007
10.0 SP1	1.118	10770389
10.0 SP1	1.117	10778264
10.0 SP1	1.116	10775944
10.0 SP1	1.114	10773482
10.0 SP1	1.113	10776963
10.0 SP1	1.112	10773582
10.0 SP1	1.11	10775626
10.0 SP1	1.109	10774945
10.0 SP1	1.107	10771197
10.0 SP1	1.106	10775314
10.0 SP1	1.105	10770007
10.0 SP1	1.104	10776418
10.0 SP1	1.103	10711328
10.0 SP1	1.101	10772702
10.0	0.6	10778949
10.0	0.59	10778044
10.0	0.57	10771078
10.0	0.55	10776106
10.0	0.54	10775139
10.0	0.53	10777358
10.0	0.5	10770007
10.0	0.49	10775314
10.0	0.45	10773569
10.0	0.44	10768129

Quartus II Software Version	Patch	Customer Service Request Number
10.0	0.43	10772702
10.0	0.4	10773124
10.0	0.35	10769985
10.0	0.33	10771417
10.0	0.05	10759553
9.1 SP2	2.96	—
9.1 SP2	2.95	10772308
9.1 SP2	2.92	10766985
9.1 SP2	2.9	10773582
9.1 SP2	2.81	10771417
9.1 SP2	2.78	10762180
9.1 SP2	2.64	10762478
9.1 SP2	2.6	10758666
9.1 SP2	2.56	10761178
9.1 SP2	2.54	10759553
9.1 SP2	2.48	10756747
9.1 SP2	2.114	10778044
9.1 SP2	2.112	10778044
9.1 SP2	2.109	10778044
9.1 SP2	2.108	10778044
9.1 SP2	2.106	10777888
9.1 SP2	2.104	10778044
9.1 SP2	2.101	10774827
9.1 SP2	2.1	10767106
9.1 SP1	1.76	10776294
9.1 SP1	1.75	10765593
9.1	0.92	10766985
9.0 SP2	2.206	10765972

Document Revision History

Table 1 shows the revision history for this document.

Table 1. Document Revision History

Date	Version	Changes
December 2010	1.0	Initial release.