About These Release Notes
System Requirements ................................................................. xiii
Update Status ............................................................................. xiv

Chapter 1. 8B10B Encoder/Decoder
Revision History ........................................................................... 1–1
Errata ......................................................................................... 1–1

Chapter 2. ASI
Revision History ........................................................................... 2–1
Errata ......................................................................................... 2–1
Incorrect User Guide on ACDS ...................................................... 2–1
NativeLink Simulation Fails .......................................................... 2–2
VCS Simulator ............................................................................ 2–2
NativeLink Does Not Support Gate-Level Simulation ...................... 2–3

Chapter 3. CIC
Revision History ........................................................................... 3–1
Errata ......................................................................................... 3–1
Error Generating HDL for Decimator with More Than 9 Stages and 11 Interfaces 3–1

Chapter 4. CRC Compiler
Revision History ........................................................................... 4–1
Errata ......................................................................................... 4–1
Incorrect User Guide on ACDS ...................................................... 4–1
Testbench Directory Generated When You Create a Simulation Model 4–2

Chapter 5. DDR and DDR2 SDRAM Controller Compiler
Revision History ........................................................................... 5–1
Errata ......................................................................................... 5–1
Incorrect User Guide on ACDS ...................................................... 5–2
DDR and DDR2 SDRAM Controllers Verilog HDL Design Does Not Work 5–2
“Cannot Find Source Node” Error During Post-Compile Timing Analysis 5–3
VHDL Package Declaration Error When Upgrading the MegaCore Function 5–3
Read Requests Are Sometimes Discarded ........................................ 5–4
Error: Can't Find the Clock Output Pins. Stop. .................................. 5–5
ODT Launches Off System Clock .................................................. 5–5
Error Message When Recompiling a Project ..................................... 5–6
Pin Planner HDL Syntax Error ..................................................... 5–6

Chapter 6. DDR and DDR2 SDRAM High-Performance Controller
Revision History ........................................................................... 6–1
Errata ......................................................................................... 6–1
Incorrect User Guide on ACDS ...................................................... 6–2
DDR2 Controller Designs with ODT Setting and Registered DIMM Options Enabled Cannot Be Generated 6–3
Simulation Fails When test_incomplete_writes Signal is Asserted .......... 6–4
DDR2 Full Rate Controller Designs with Error Correction Coding (ECC) Fail to Meet Timing 6–5

© 1 July 2009 Altera Corporation Library Version 9.0 MegaCore IP Library Release Notes and Errata
Chapter 7. DDR3 SDRAM High-Performance Controller
Revision History ................................................................. 7–1
Errata .................................................................................. 7–1
  Address Mirroring Not Supported By Memory Simulation Model ...................... 7–2
  Incorrect User Guide on ACDS ............................................ 7–2
  Simulation Fails When test_incomplete_writes Signal is Asserted ..................... 7–3
  Different Read Data Orders ..................................................................... 7–3
  Memory Preset Parameters Do Not Get Updated ......................................... 7–4
  Designs with Error Correction Coding (ECC) Do Not Work After Subsequent Reset 7–5
  Incorrect Controller Latency Information in User Guide .................................. 7–5
  Unable to Deliberately Corrupt the ECC Data When Using the Native Interface 7–6
  DDR3 SDRAM High-Performance Controller May Not Appear in SOPC Builder 7–6

Chapter 8. FFT
Revision History ................................................................... 8–1
Errata .................................................................................. 8–1
  Example Design Fails Compilation ......................................................... 8–1
  Display Symbol Button in IP Toolbench is Missing ..................................... 8–2
  Cannot Find Memory Initialization File if Not in Project Directory ................. 8–2
  Floating-Point FFT Produces Non-Zero Output ........................................ 8–3
  Simulation Errors—Synopsys VCS .................................................... 8–3
  Simulation Errors—Incorrect Results ...................................................... 8–4
  Simulation Errors—MATLAB Model Mismatch ....................................... 8–4
  Gate-Level Simulations ........................................................................ 8–5

Chapter 9. FIR Compiler
Revision History .................................................................. 9–1
Errata .................................................................................. 9–1
  Simulation Fails for the Coefficient Reloadable Filters ............................... 9–2
  Incorrect Results for Multi-Bit Serial or Interpolation with Signed Binary Fractional 9–2
  Cannot Select M9K Data or Coefficient Storage When Device Family is Cyclone III 9–2
  Incorrect Output for Signed Binary Fractional Multi-Bit Serial or Interpolation Filter 9–3
Chapter 10. HyperTransport

Revision History ................................................................. 10–1
Errata ................................................................................. 10–1

Chapter 11. NCO

Revision History ................................................................. 11–1
Errata ................................................................................. 11–1

Cannot Implement Multiplier-Based Architecture using Multipliers for Arria II GX .................. 11–1
Resource Estimate Displays LEs Instead of ALUTs for Arria II GX ........................................ 11–2
Warning Message Displayed Twice .................................................................................... 11–2
Mismatches Between Multiplier-Based MATLAB and RTL Models ...................................... 11–3
Mismatches Between the MATLAB and RTL Models ............................................................ 11–3
The MATLAB Simulation File Cannot be Used on UNIX ...................................................... 11–4

Chapter 12. Nios II Processor

Revision History ................................................................. 12–1
Errata ................................................................................. 12–1

Design Assistant Error on Clock Signal Source in HardCopy Designs ...................................... 12–2
Nios II MMU Micro TLBs Not Flushed .................................................................................. 12–2
Hardware Breakpoints Not Supported with Nios II MMU and MPU .................................... 12–2
Nios II Ports Created Incorrectly ....................................................................................... 12–3
Errors Adding Custom Instruction to the Nios II Processor .................................................. 12–3

Chapter 13. PCI Compiler

Revision History ................................................................. 13–1
Errata ................................................................................. 13–1

Incorrect User Guide on ACDS ......................................................................................... 13–2
F1152 Packages for HardCopy III and HardCopy IV-E Not Supported .................................. 13–2
Wirebond Packages for HardCopy III and HardCopy IV-E Not Supported ............................ 13–3
Designs With Stratix III Devices Fail to Meet Timing ............................................................ 13–3
Designs With Stratix IV Devices Fail to Meet Timing ............................................................ 13–3
Device Support Incorrect in User Guide ............................................................................... 13–4
Full Compilation Fails for Some Cyclone III Devices When Using Recommended PCI Pin Assignments 13–4
TimeQuest Timing Analysis Fails for Stratix III Devices When Using Recommended PCI Constraints at Lower Seed Number ................................................................ 13–5
TimeQuest Timing Analysis Fails for HardCopy II Devices When Using Recommended PCI Constraints .............................................................................................. 13–6
TimeQuest Timing Analysis Fails for Some Arria GX and Stratix II Devices When Using Recommended PCI Constraints .................................................................................. 13–6
TimeQuest Timing Analysis Fails for Some Cyclone Devices When Using Recommended PCI Constraints .............................................................................................. 13–7

Bit Serial Filter With 32-Bit Coefficients Does Not Work ..................................................... 9–3
Half-Band Decimator and Symmetric Interpolator Do Not Support Unsigned Type ................ 9–4
Signed Binary Fraction Results in Output Bit Width Mismatch .......................................... 9–4
Incorrect Screenshot in the User Guide ............................................................................... 9–4
Some Gate Level Simulations are Incorrect ....................................................................... 9–5
Cannot Find Memory Initialization File if Not in Project Directory .................................... 9–5
Block Memory Incorrectly Used When Logic Storage Selected ....................................... 9–6
Simulation Result Incorrect Using MCV Interpolation Filters ...................................... 9–6
Reloadable Coefficient Filters Fail for Some MCV Filters ................................................. 9–7
Quartus II Simulation Vector File Not Generated ............................................................. 9–7

Incorrect Screenshot in the User Guide ............................................................................... 9–4
Some Gate Level Simulations are Incorrect ....................................................................... 9–5
Cannot Find Memory Initialization File if Not in Project Directory .................................... 9–5
Block Memory Incorrectly Used When Logic Storage Selected ....................................... 9–6
Simulation Result Incorrect Using MCV Interpolation Filters ...................................... 9–6
Reloadable Coefficient Filters Fail for Some MCV Filters ................................................. 9–7
Quartus II Simulation Vector File Not Generated ............................................................. 9–7

Designs With Stratix IV Devices Fail to Meet Timing ............................................................ 13–3
Wirebond Packages for HardCopy III and HardCopy IV-E Not Supported .......................... 13–2
F1152 Packages for HardCopy III and HardCopy IV-E Not Supported .................................. 13–2
Designs With Stratix III Devices Fail to Meet Timing ............................................................ 13–3
Designs With Stratix IV Devices Fail to Meet Timing ............................................................ 13–3
Device Support Incorrect in User Guide ............................................................................... 13–4
Full Compilation Fails for Some Cyclone III Devices When Using Recommended PCI Pin Assignments 13–4
TimeQuest Timing Analysis Fails for Stratix III Devices When Using Recommended PCI Constraints at Lower Seed Number ................................................................ 13–5
TimeQuest Timing Analysis Fails for HardCopy II Devices When Using Recommended PCI Constraints .............................................................................................. 13–6
TimeQuest Timing Analysis Fails for Some Arria GX and Stratix II Devices When Using Recommended PCI Constraints .................................................................................. 13–6
TimeQuest Timing Analysis Fails for Some Cyclone Devices When Using Recommended PCI Constraints .............................................................................................. 13–7
Chapter 14. PCI Express Compiler

Revision History .......................................................... 14–1

Errata ................................................................. 14–2

- When Using the Avalon-MM interface, Disabling the Master Bus Does Not Stop Requests ........ 14–4
- An Error Might Occur in Logging a Poisoned TLP ........................................ 14–4
- The tx_cred Signal Indicates Incorrect Non-Posted Credits Available for the Soft IP Implementation 14–4
- Hard IP Implementation Returns 0x00 when the Interrupt Pin Register Is Read .............. 14–5
- PCI Express Compiler User Guide Provides Incorrect Speed Grade Information for Gen1 .... 14–5
- The tx_cred Signal Indicates Incorrect Non-Posted Credits Available in Hard IP Implementation ... 14–6

Description of the Completion Side Band Signals and Error Handling in the PCI Express Compiler

User Guide is Incomplete ........................................ 14–6

Transaction Layer ................................................. 14–7

Completion Side Band Signals ................................ 14–9

The Receive Direction Transaction Layer Routing Rules are Incomplete in PCI Express Compiler User Guide .................................................. 14–11

A ×1 or ×4 Soft IP Variation Might Incorrectly Issue a NAK ........................................ 14–11

You Cannot Use the MegaWizard Plug-In Manager to Edit the SERDES in the Hard IP

Implementation of the PCI Express MegaCore Function ........................................ 14–12

Gate-Level Simulation Fails for Hard IP Variations ................................................ 14–12

Incorrect Link Training for Stratix IV GX Gen2 ×8 Hard IP Implementation ............... 14–13

Guidelines for Passing the PCI Express Electrical Gold Test on the v2.0 Compliance Base Board (CBB) 14–13

Endpoints Using the Hard IP Implementation Incorrectly Handle CfgRd0 ............. 14–14

Endpoints Using the Soft IP Implementation Incorrectly Handle CfgRd0 ............. 14–14

The Hard IP Implementation of the PCI Express Compiler May Be Unable to Exit the Disable State at the Gen2 Rate .................................. 14–15

Timing Closure for Chaining DMA Design Example Gen1×8 in Stratix IV C3 and C4 Speed Grades . 14–15

The ×8 Soft IP Implementation of PCI Express MegaCore Function Only Supports 4 KByte Expansion

ROM BAR .......................................................... 14–16

The Description of cfg_devcsr[31:0] in the PCI Express Compiler User Guide is Incorrect .... 14–16

Adding Two PCI Express Components to an SOPC Builder System May Cause a System Error ... 14–17

License File for Soft IP Implementation of the PCI Express Compiler Does Not Work ........ 14–17

EDA Netlist Writer Does Not Write Netlist for Hard IP Implementation of PCI Express ........ 14–18

Stratix IV Projects with Pin Assignments Specified Using the Pin Planner May Fail Quartus II

Compilation ...................................................... 14–18

Simulation Fails when Using ModelSim AE for Stratix II GX MegaCore Functions with the Avalon-ST or Descriptor/Data Interfaces ........................................ 14–18

The Chaining DMA Design Example May Issue DMA Write Requests that Violate the 4 KByte Boundary Rule in the VHDL Version ........................................ 14–19

Design Example in Hardware Might Require the RC Slave Module .......................... 14–19

Root Port BFM in Version 8.1 of the PCI Express Testbench is not Backwards Compatible .... 14–20

Incorrect Connection of SOPC Builder Interrupt Sources to PCI Express Components ........ 14–20

PCI Express Avalon-MM Tx Interface Deadlocks on a Read Request ..................... 14–21

Unable to Compile the Example Design Successfully in Quartus II when using ECRC Forwarding . 14–21

Chaining DMA Design Example Forwards Tx ECRC with Incorrect Alignment ........... 14–22

User Guide Incorrectly Documents the Number of Address Pages ......................... 14–22

User Guide Incorrectly Documents rx_st_data and tx_st_data in 128-Bit Mode ................ 14–23
Revision History

Chapter 16. POS-PHY Level 4

Errata
Missing Timescale Directive in NativeLink Verilog HDL Testbench
Compilation Error in NativeLink VHDL Flow for NCSim
IP Toolbench Incorrect Behavior
Errors with Pin Planner Top-Level File

Chapter 17. RapidIO

Errata
Error Response Packet Can Be Sent Twice if the io_m_rd_readerror Signal is Asserted
Stratix III Device Support Level is Reported as Preliminary
Response Packet is Sent for Request Packet with Reserved Transaction Type
User Guide Description of Direction of io_s_rd_read Signal is Incorrect
SOPC Builder Testbench May Fail on 1× Stratix GX Variations at 1.25 Gbaud
Transport Layer Can Drop Outgoing Packets if Physical Layer Transmit Buffer Fills
Testbench Fails on Some Stratix GX Variations
Some Variations With Reference Clock Frequency 390.625 MHz do Not Meet Timing
The packet_transmitted Output Signal is Not Reliable — Cancelled
Migration of Existing RapidIO MegaCore Function May Generate Warning Message
SourceID Can Be Incorrectly Set to Zero in NWRITE_R Response Packets
A Cancelled Packet Can Be Processed As a Normal Packet
Chapter 19. Reed-Solomon Compiler

Revision History ......................................................... 19–1

Errata ................................................................. 19–1

User Guide Link from IP Toolbench is Inactive ......................... 19–1

Verilog HDL Simulation Fails .......................................... 19–2

RS Decoder Fails When Number of Check Symbols and Symbols are Similar 19–2

Display Symbol Button in IP Toolbench is Missing .................. 19–3

Verilog HDL Designs Do Not Simulate in Synopsys VCS ............... 19–3

No Symbol In IP Toolbench Symbol Window .......................... 19–3

File Summary Does Not List All Generated Files ..................... 19–4
Chapter 20. RLDRAM II
Revision History ................................................................. 20–1
Errata .................................................................................. 20–1
  Incorrect User Guide on ACDS ............................................. 20–2
  RLDRAM II Verilog HDL Design Does Not Work .................. 20–2
  Error When Upgrading ........................................................ 20–3
  NativeLink Fails with the ModelSim Simulator ....................... 20–4
  Add an RLDRAM II Controller to a Project with Other Memory Controllers 20–4
  Simulating with the NCSim Software ..................................... 20–5
  Simulating with the VCS Simulator ....................................... 20–5
  Multiple Instances of the auk_ddr_functions.vhd File ............. 20–6
  Gate-Level Simulation Filenames ......................................... 20–6
  Unpredictable Results for Gate-Level Simulations (HardCopy II Devices Only) .. 20–7
  Editing the Custom Variation (non-DQS Mode) ..................... 20–7

Chapter 21. SDI
Revision History ................................................................. 21–1
Errata .................................................................................. 21–1
  Incorrect User Guide on ACDS ............................................. 21–2
  No Support for IP Advisor .................................................. 21–2
  The Interface Signals Do Not Behave As Expected ................ 21–3
  Transmitter Line Number (LN) Insertion ............................... 21–3
  Cyclical Redundancy Check (CRC) Error When Receiving 3G-SDI 425M-A Input 21–4
  SDI Receiver Misdetects Data Rate ....................................... 21–4
  SDI Receiver Fails to Align .................................................. 21–4
  Example Designs Are Out of Date ....................................... 21–5
  Quartus II Fitter Reports Error When PLL-Generated Clock of 67.5 MHz Is Used in Stratix GX Devices 21–6
  NativeLink Fails With ModelSim Simulator ......................... 21–6
  Timing Not Met in C5 Speed Grade Stratix II GX Devices ........ 21–7

Chapter 22. SerialLite II
Revision History ................................................................. 22–1
Errata .................................................................................. 22–1
  Incorrect User Guide on ACDS ............................................. 22–2
  Simulating Streaming Mode Design with a Non-Default Reference Clock Frequency Selected 22–2
  Selecting Non-Default Input Clock Frequency Value for Stratix IV GX Devices ........ 22–3
  Demo Testbench Cannot Be Simulated With Arria GX Variants .... 22–3
  Timing Analyzer Reports “Critical Warning: Timing Requirements Not Met” .......... 22–4
  Stratix IV Internal Core Clocking Is Incorrect for a Design Using TSIZE = 2 and Data Rate > 3,125 Mbps 22–5
  Link Management FIFO May Overflow When Small Packets Are Sent Continuously Over a Long 22–5
  Period of Time ................................................................... 22–5
  Rx Only Mode With Clock Compensation Does Not Support All Reference Clock Selections ... 22–6
  Generation Fails or Corrupt Variation Generated if Asymmetric Broadcast Mode Used .... 22–6

Chapter 23. Triple Speed Ethernet
Revision History ................................................................. 23–1
Errata .................................................................................. 23–1
  Half-Duplex Late Collision in MACs Corrupts Next Packets .......... 23–2
  MACs in Half-Duplex Mode Continue Transmitting Packets ....... 23–3
Chapter 24. UTOPIA Level 2 Master

Revision History ...................................................... 24–1
Errata ................................................................. 24–1

Chapter 25. UTOPIA Level 2 Slave

Revision History ...................................................... 25–1
Errata ................................................................. 25–1

Chapter 26. Video and Image Processing Suite

Revision History ...................................................... 26–1
Errata ................................................................. 26–2
Deinterlacer and Frame Buffer Connected to DDR3 May Not Work Properly .......... 26–3
RTL Simulation Reports Errors When Using Verilog HDL .............................. 26–4
Incorrect Simulation Models Created for Deinterlacer and Frame Buffer ........ 26–4
Deinterlacer and Test Pattern Generator May Not Upgrade ....................... 26–4
The 2D Median Filter Does Not Support 7x7 Filter Size ............................... 26–5
Misleading Error Message Issued by Color Plane Sequencer ...................... 26–5
Changing Target Device After Quartus II Compilation Causes Error ............ 26–6
Active Picture Line Selection Should be Available for Separate Sync Mode ...... 26–6
v7.2 MegaCore Functions are Not Compatible with v8.x Quartus II ............... 26–7
Packets Sent to VIP Cores Must Have Non-Empty Payload ....................... 26–7
Control Port Behavior Unpredictable for Scaler and Clipper ..................... 26–7
Error in Clocked Video Output Constraint File ...................................... 26–8
Simulation Models Not Created For Clocked Video Functions ..................... 26–8
Cannot Connect Adapter in SOPC Builder For Multiple Parallel Planes ....... 26–9
Line Buffer Compiler Does Not Generate for Arria GX ............................ 26–10
Misleading Warning Message for Color Plane Sequencer .......................... 26–10
Color Plane Sequencer Does Not Report GUI Messages .......................... 26–11
The .hex Files for Simulation in SOPC Builder Systems Must be Moved ......... 26–11
Deinterlacer Fails to Generate in Some Configurations ............................ 26–12
Color Plane Sequencer Shows Parallel Bit Ranges in Reverse Order ........................................ 26–12
Clipper Fails to Send EOP When Active Region is Bottom Right ........................................ 26–13
File Name Clash for Files Generated by Clocked Video Functions ........................................ 26–13
The F Falling Edge Line Clocked Video Output Parameter Not Loaded ................................. 26–13
Layers Supported by Alpha Blending Mixer Incorrect in User Guide .................................. 26–14
Addendum to the Alpha Blending Mixer Functional Description ........................................ 26–14
Control Register Map for the Clipper Missing From User Guide ........................................ 26–14
SOPC Builder Avalon-ST Adapter Does Not Support Avalon-ST Video ............................... 26–15
Scalar Coefficients Preview Window Cannot be Closed ....................................................... 26–16
Precision Must be Set When Using Lanczos Coefficients in Scaler ..................................... 26–16
Cyclone II M4K Fails in Alpha Blending Mixer and Gamma Corrector ................................ 26–16

Chapter 27. Viterbi Compiler
Revision History .................................................................................................................. 27–1
Errata .................................................................................................................................. 27–1
Trellis Mode Fails .............................................................................................................. 27–1
Testbench ber_clear Signal is Not Connected ................................................................. 27–2
Gate-Level Simulation Fails ............................................................................................... 27–2
Display Symbol Button in IP Toolbench is Missing ......................................................... 27–2
IP Functional Simulation Model Fails ................................................................................. 27–3
File Summary Does Not List All Generated Files ............................................................ 27–3

Additional Information
How to Contact Altera ......................................................................................................... Info–1
Typographic Conventions .................................................................................................. Info–1
These release notes cover versions 8.0 through 9.0 of the Altera® MegaCore® IP Library. The chapters in these release notes describe the revision history and errata for each product in the MegaCore IP Library.

From v8.0 onwards, this document replaces all individual IP product release notes and errata sheets that Altera previously published.

Errata are functional defects or errors, which may cause the product to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

The product errata tables use the following indicators:

- A checkmark “✓” indicates an issue is applicable to that version
- “Fixed” indicates the issue was fixed in that version
- A dash “—” indicates the issue is not applicable to that version

For the most up-to-date errata for this release, refer to the latest version of the MegaCore IP Library Release Notes on the Altera website.

For more information about Quartus® II issues, refer to the Quartus II Software Release Notes.

These release notes use the following Altera trademarks:

- Arria® devices
- Avalon® interface
- Cyclone® devices
- HardCopy® devices
- MegaCore function
- MegaWizard™ Plug-In
- Nios® II processor
- Quartus II software
- SignalTap® II logic analyzer
- Stratix® devices

**System Requirements**

The MegaCore IP Library is distributed with the Quartus II software and downloadable from the Altera website, www.altera.com.
For system requirements and installation instructions, refer to *Quartus II Installation & Licensing for Windows and Linux Workstations*.

## Update Status

The following table shows the chapter update status for these release notes.

<table>
<thead>
<tr>
<th>Chapter</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. 8B10B Encoder/Decoder</td>
<td>15 May 2009</td>
</tr>
<tr>
<td>2. ASI</td>
<td>1 July 2009</td>
</tr>
<tr>
<td>3. CIC</td>
<td>15 May 2009</td>
</tr>
<tr>
<td>4. CRC Compiler</td>
<td>1 July 2009</td>
</tr>
<tr>
<td>5. DDR and DDR2 SDRAM Controller Compiler</td>
<td>1 July 2009</td>
</tr>
<tr>
<td>6. DDR and DDR2 SDRAM High-Performance Controller</td>
<td>1 July 2009</td>
</tr>
<tr>
<td>7. DDR3 SDRAM High-Performance Controller</td>
<td>1 July 2009</td>
</tr>
<tr>
<td>8. FFT</td>
<td>15 May 2009</td>
</tr>
<tr>
<td>9. FIR Compiler</td>
<td>15 June 2009</td>
</tr>
<tr>
<td>10. HyperTransport</td>
<td>15 March 2009</td>
</tr>
<tr>
<td>11. NCO</td>
<td>15 May 2009</td>
</tr>
<tr>
<td>13. PCI Compiler</td>
<td>1 July 2009</td>
</tr>
<tr>
<td>14. PCI Express Compiler</td>
<td>1 July 2009</td>
</tr>
<tr>
<td>15. POS-PHY Level 2 and 3 Compiler</td>
<td>15 March 2009</td>
</tr>
<tr>
<td>16. POS-PHY Level 4</td>
<td>15 June 2009</td>
</tr>
<tr>
<td>17. RapidIO</td>
<td>1 July 2009</td>
</tr>
<tr>
<td>18. QDRII SRAM</td>
<td>1 July 2009</td>
</tr>
<tr>
<td>19. Reed-Solomon Compiler</td>
<td>15 May 2009</td>
</tr>
<tr>
<td>20. RLDRAM II</td>
<td>1 July 2009</td>
</tr>
<tr>
<td>21. SDI</td>
<td>1 July 2009</td>
</tr>
<tr>
<td>22. SerialLite II</td>
<td>1 July 2009</td>
</tr>
<tr>
<td>23. Triple Speed Ethernet</td>
<td>1 July 2009</td>
</tr>
<tr>
<td>24. UTOPIA Level 2 Master</td>
<td>15 March 2009</td>
</tr>
<tr>
<td>25. UTOPIA Level 2 Slave</td>
<td>15 March 2009</td>
</tr>
<tr>
<td>26. Video and Image Processing Suite</td>
<td>1 July 2009</td>
</tr>
<tr>
<td>27. Viterbi Compiler</td>
<td>1 July 2009</td>
</tr>
</tbody>
</table>
Revision History

Table 1–1 shows the revision history for the 8B10B Encoder/Decoder MegaCore function.

For more information about the new features, refer to the 8B10B Encoder/Decoder MegaCore Function User Guide.

Table 1–1. 8B10B Encoder/Decoder MegaCore Function Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.0 SP1</td>
<td>May 2009</td>
<td>Preliminary support for HardCopy III and HardCopy IV E devices.</td>
</tr>
<tr>
<td>9.0</td>
<td>March 2009</td>
<td>Preliminary support for Arria II GX device family.</td>
</tr>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>Preliminary support for Stratix IV device family.</td>
</tr>
</tbody>
</table>

Errata

No known issues in v9.0, 8.1, and 8.0.
2. ASI

Revision History

Table 2–1 shows the revision history for the ASI MegaCore function.

For more information about the new features, refer to the *ASI MegaCore Function User Guide*.

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.0 SP2</td>
<td>July 2009</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>9.0 SP1</td>
<td>May 2009</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>9.0</td>
<td>March 2009</td>
<td>Preliminary support for Arria II GX devices.</td>
</tr>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>• Preliminary support for Stratix IV devices.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added GX transceiver-based core for Arria GX devices.</td>
</tr>
</tbody>
</table>

Errata

Table 2–2 shows the issues that affect the ASI MegaCore function v9.0 SP2, 9.0 SP1, 9.0, 8.1, and 8.0.

Not all issues affect all versions of the ASI MegaCore function.

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Jul 09</td>
<td>Incorrect User Guide on ACDS</td>
<td>Fixed</td>
</tr>
<tr>
<td>15 May 08</td>
<td>NativeLink Simulation Fails</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>VCS Simulator</td>
<td>—</td>
</tr>
<tr>
<td>01 Dec 06</td>
<td>NativeLink Does Not Support Gate-Level Simulation</td>
<td>✓</td>
</tr>
</tbody>
</table>

Incorrect User Guide on ACDS

The user guide that is on the Altera Complete Design Suite (ACDS) is an out-of-date version.

**Affected Configurations**

This issue affects no configurations.
Design Impact

There is no design impact.

Workaround

Download the latest *ASI MegaCore Function User Guide* from the Altera website.

Solution Status

This issue is fixed in version 9.0 SP2 of the ASI MegaCore function.

NativeLink Simulation Fails

The NativeLink example simulation fails because it cannot find the memory initialization files (.mif).

Affected Configurations

This issue only affects example simulations.

Design Impact

This issue has no design impact.

Workaround

Regenerate both the ASI receiver and ASI transmitter MegaCore functions.

1. Double click on the asi_rx instance in the project navigator pane. This action opens up the asi_rx instance MegaWizard Plug-In Manager.
2. Click Finish, then Exit.
3. On the Tools menu, click MegaWizard Plug-In Manager.
4. Select Edit an existing megafunction.
5. Browse to \72\ip\asi\testbench\asi_mc_build, select asi_tx_sim.v, and click Next.
6. In the MegaWizard Plug-In Manager, click the Finish button, then Exit.

The .vo files for both cores are now regenerated.

You can now proceed with NativeLink simulation as described in the user guide.

Solution Status

This issue is fixed in version 8.0 of the ASI MegaCore Function.

VCS Simulator

The ASI MegaCore function may not work with the VCS simulator.

Affected Configurations

This issue affects all configurations.
Design Impact
If you simulate your design in the VCS simulator, it may not work.

Workaround
Use a different simulator.

Solution Status
This issue is fixed in version 8.0 of the ASI MegaCore function.

NativeLink Does Not Support Gate-Level Simulation
When using the NativeLink simulation example, the gate-level simulation design fails.

Affected Configurations
This issue affects all simulators supported by NativeLink.

Design Impact
This issue only affects simulation and does not affect the design compilation.

Workaround
Perform an RTL simulation of the NativeLink simulation example.

Solution Status
This issue will be fixed in a future version of the ASI MegaCore function.
Revision History

Table 3–1 shows the revision history for the CIC MegaCore function.

For information about the new features, refer to the CIC MegaCore Function User Guide.

Table 3–1. CIC MegaCore Function Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.0 SP1</td>
<td>May 2009</td>
<td>Preliminary support for HardCopy III and HardCopy IV E devices.</td>
</tr>
</tbody>
</table>
| 9.0    | March 2009 | - Preliminary support for Arria II GX.  
|        |            | - Added an option to optimize for speed.               |
| 8.1    | November 2008 | - Full support for Stratix III.  
|        |            | - Withdrawn support for UNIX.                         |
| 8.0    | May 2008   | - Full support for Cyclone III.  
|        |            | - Preliminary support for Stratix IV.                  |

Errata

Table 3–2 shows the issues that affect the CIC MegaCore function v9.0, v8.1, and v8.0.

Table 3–2. CIC MegaCore Function Errata

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 Mar 09</td>
<td>Error Generating HDL for Decimator with More Than 9 Stages and 11 Interfaces</td>
<td>9.0 ✔ 8.1 ✔ 8.0 —</td>
</tr>
</tbody>
</table>

Error Generating HDL for Decimator with More Than 9 Stages and 11 Interfaces

An error is issued when you generate HDL after selecting a Decimator filter with Number of Stages set to more than 9 and Number of Interface to more than 11.

Affected Configurations

Decimator filters with more than 9 stages and more than 11 interfaces.

Design Impact

An error is issued when you generate HDL.

Workaround

If you want more than 9 stages you must select 11 interfaces or fewer. If you want more than 11 interfaces you must choose 9 stages or fewer.
Solution Status

This issue will be fixed in a future version of the CIC MegaCore function.
Revision History

Table 4–1 shows the revision history for the CRC Compiler.

For more information about the new features, refer to the CRC Compiler User Guide.

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.0 SP2</td>
<td>July 2009</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>9.0 SP1</td>
<td>May 2009</td>
<td>Preliminary support for HardCopy III and HardCopy IV E devices.</td>
</tr>
<tr>
<td>9.0</td>
<td>March 2009</td>
<td>Preliminary support for Arria II GX device family.</td>
</tr>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>Preliminary support for Stratix IV device family.</td>
</tr>
</tbody>
</table>

Errata

Table 4–2 shows the issues that affect the CRC Compiler v9.0 SP2, 9.0 SP1, 9.0, 8.1, and 8.0.

Not all issues affect all versions of the CRC Compiler.

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Jul 09</td>
<td>Incorrect User Guide on ACDS</td>
<td>9.0 SP2 9.0 SP1 9.0 8.1 8.0</td>
</tr>
<tr>
<td>01 Dec 06</td>
<td>Testbench Directory Generated When You Create a Simulation Model</td>
<td>✔ ✔ ✔ ✔ ✔</td>
</tr>
</tbody>
</table>

Incorrect User Guide on ACDS

The user guide that is on the Altera Complete Design Suite (ACDS) is an out-of-date version.

Affected Configurations

This issue affects no configurations.

Design Impact

There is no design impact.

Workaround

Download the latest CRC Compiler User Guide from the Altera website.
Solution Status
This issue is fixed in version 9.0 SP2 of the CRC Compiler.

Testbench Directory Generated When You Create a Simulation Model
When you create a simulation model, the CRC compiler automatically creates a testbench directory in the project directory for you. If you follow the Running the Testbench Example steps in the CRC Compiler User Guide to create the generator and checker files, another testbench directory is created as a subdirectory of the initial testbench directory, resulting in the following directory structure:

\c:\altera\projects\crc_project\testbench\testbench

when the initial directory is
\c:\altera\projects\crc_project\testbench

Affected Configuration
All CRC MegaCore function variations are affected.

Design Impact
This issue has no design impact.

Workaround
The testbench subdirectory (testbench\testbench) of the initial \c:\altera\projects\crc_project\testbench directory may be deleted.

Solution Status
No change is planned currently.
5. DDR and DDR2 SDRAM Controller Compiler

Revision History

Table 5–1 shows the revision history for the DDR and DDR2 SDRAM Controller Compiler.

For more information about the new features, refer to the *DDR and DDR2 SDRAM Controller Compiler User Guide*.

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.0 SP2</td>
<td>July 2009</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>9.0 SP1</td>
<td>May 2009</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>9.0</td>
<td>March 2009</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>8.0 SP1</td>
<td>July 2008</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>Maintenance release.</td>
</tr>
</tbody>
</table>

Errata

Table 5–2 shows the issues that affect the DDR and DDR2 SDRAM Controller Compiler v9.0 SP2, 9.0 SP1, 9.0, 8.1 and 8.0.

Not all issues affect all versions of the DDR and DDR2 SDRAM Controller Compiler.

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Jul 09</td>
<td>Incorrect User Guide on ACDS</td>
<td>9.0 SP2 9.0 SP1 9.0 8.1 8.0 SP1 8.0</td>
</tr>
<tr>
<td>15 Mar 09</td>
<td>DDR and DDR2 SDRAM Controllers Verilog HDL Design Does Not Work</td>
<td>9.0 SP2 9.0 SP1 9.0 8.1 8.0 SP1 8.0</td>
</tr>
<tr>
<td></td>
<td>&quot;Cannot Find Source Node&quot; Error During Post-Compile Timing Analysis</td>
<td>9.0 SP2 9.0 SP1 9.0 8.1 8.0 SP1 8.0</td>
</tr>
<tr>
<td>01 Nov 08</td>
<td>VHDL Package Declaration Error When Upgrading the MegaCore Function</td>
<td>9.0 SP2 9.0 SP1 9.0 8.1 8.0 SP1 8.0</td>
</tr>
<tr>
<td>15 Jul 08</td>
<td>Read Requests Are Sometimes Discarded</td>
<td>9.0 SP2 9.0 SP1 9.0 8.1 8.0 SP1 8.0</td>
</tr>
<tr>
<td>15 Oct 07</td>
<td>Error: Can't Find the Clock Output Pins. Stop.</td>
<td>9.0 SP2 9.0 SP1 9.0 8.1 8.0 SP1 8.0</td>
</tr>
<tr>
<td>01 Jul 07</td>
<td>ODT Launches Off System Clock</td>
<td>9.0 SP2 9.0 SP1 9.0 8.1 8.0 SP1 8.0</td>
</tr>
<tr>
<td>01 Jun 06</td>
<td>Error Message When Recompiling a Project</td>
<td>9.0 SP2 9.0 SP1 9.0 8.1 8.0 SP1 8.0</td>
</tr>
</tbody>
</table>
Incorrect User Guide on ACDS

The user guide that is on the Altera Complete Design Suite (ACDS) is an out-of-date version.

Affected Configurations

This issue affects no configurations.

Design Impact

There is no design impact.

Workaround

Download the latest DDR and DDR2 SDRAM Controller Compiler User Guide from the Altera website.

Solution Status

This issue is fixed in version 9.0 SP2 of the DDR and DDR2 SDRAM Compiler.

DDR and DDR2 SDRAM Controllers Verilog HDL Design Does Not Work

If you generate a Verilog HDL instance of the DDR or DDR2 SDRAM Controller version 8.1, the design will not work in hardware or simulation.

Affected Configurations

This issue affects all Verilog HDL instances of the Insert extra pipeline registers in datapath option enabled. The VHDL designs are not affected.

Design Impact

Your design will not work in hardware or simulation.

Workaround

If you require a Verilog HDL instance of the DDR or DDR2 SDRAM Controller, you can use one of the following workarounds:

- Continue to use your existing version 8.0 instance. There are no functional changes between versions 8.0 and 8.1 of the DDR or DDR2 SDRAM Controller, so you are not required to upgrade.

- If you choose to upgrade to version 8.1 or if you do not have a version 8.0 instance, edit the `<variation name>_auk_ddr_sdram.v` file to change all instances of the line:

```vhdlelse if (0)
toelse if (1)```

Solution Status

This issue is fixed in version 9.0 of the DDR and DDR2 SDRAM Controller Compiler.
“Cannot Find Source Node” Error During Post-Compile Timing Analysis

The post-compile timing script may report the following error:

```
Cannot find source node
'variation':variation_ddr_sdram...variation_auk_ddr_datapath:ddr_io
variation_auk_ddr_dqs_group|g_datapath:0:g_ddr_io|dq_enable_reset[0]' 
```

**Affected Configurations**
Some Stratix II and Stratix II GX designs.

**Design Impact**
You cannot successfully complete the post-compile timing analysis.

**Workaround**
Add an "Auto Shift Register Replacement" constraint to the following node in your Quartus II project using the Assignment editor, and set the value to Off.

```
<variation>:<variation>_ddr_sdram|<variation>_auk_ddr_sdram:<variation>_auk_ddr_sdram_inst|<variation>_auk_ddr_datapath:ddr_io 
```

**Solution Status**
This issue is fixed in version 9.0 of the DDR and DDR2 SDRAM Controller Compiler.

**VHDL Package Declaration Error When Upgrading the MegaCore Function**

If you upgrade an existing custom variation of the MegaCore function, the following error may occur:

```
Error (10624): VHDL Package Declaration error at
auk_ddr_tb_functions.vhd(23): package "auk_ddr_tb_functions" already exists in the work library 
```

IP Toolbench adds files to your Quartus II project when you generate your custom variation. When you upgrade your MegaCore function, the same files from the previous and current versions are present in the same Quartus II project, which causes a VHDL error.

**Affected Configurations**
This issue affects all designs that were created in a previous version of the MegaCore function.

**Workaround**
From your Quartus II project, remove the Device Design Files that were added by the earlier version of the MegaCore function. These files can be identified by the files’ directory names.

**Design Impact**
You cannot compile your Quartus II project until you remove the duplicate files.
**Solution Status**
This issue is fixed in version 8.1 of the DDR and DDR2 SDRAM Controller Compiler.

**Read Requests Are Sometimes Discarded**
Some read requests on the local interface may be discarded and not sent to the memory, particularly the first read to a bank that has not yet been activated.

**Affected Configurations**
All configurations are affected.

**Design Impact**
Your design may fail to operate correctly.

**Workaround**
Regenerate your controller instance in the latest version of the DDR and DDR2 SDRAM Controller Compiler.

**Solution Status**
This issue is fixed in version 8.0 SP1 of the DDR and DDR2 SDRAM Controller Compiler.
Error: Can’t Find the Clock Output Pins. Stop.

The post-compile timing script reports the following error:
'Couldn't find the clock output pins. Stop.'

Affected Configurations

This issue affects designs using the DDR SDRAM controller, when the PLL counters have been reordered or the clocks for the DDR SDRAM interface are not on global clocks. This issue may occur automatically in the Fitter if there is pressure on global clock resources.

Design Impact

The design fails.

Workaround

Make the following two assignments:

<table>
<thead>
<tr>
<th>Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>ddr_pll_stratixii:g_stratixpll_ddr_pll_inst Preserve PLL Counter Order On</td>
</tr>
<tr>
<td>ddr_pll_stratixii:g_stratixpll_ddr_pll_inst</td>
</tr>
</tbody>
</table>

Replace the file names of the PLL with those in your DDR SDRAM controller design.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controller Compiler.

ODT Launches Off System Clock

In designs with a separate address and command clock, the ODT output launches from the system clock, not from this address and command clock.

Affected Configurations

This issue affects the following configurations:

- DDR2 SDRAM controller (not DDR SDRAM)
- ODT is turned on
- CAS latency is set to three
- The design uses a separate address and command clock and not the default system clock

Design Impact

This issue has no design impact.

Workaround

Use a CAS latency of four, which means one extra cycle of read latency, or use the DDR2 SDRAM High-Performance controller, which uses the ALTMEMPHY megafuction to transfer all the address and command outputs to the correct clock.
**Solution Status**
This issue will never be fixed.

**Error Message When Recompiling a Project**
If you move the directory containing your Quartus II project, or rename your Quartus II project and recompile it without regenerating the DDR or DDR2 SDRAM Controller, you may receive the following error:

*Error: DDR timing cannot be verified until project has been successfully compiled.*

This error indicates that some of the settings files contain references to the previous location or project name and the verify timing script is unable to find the current project.

**Affected Configurations**
This issue affects all configurations.

**Design Impact**
The timing script does not verify your design.

**Workaround**
Regenerate your controller in IP Toolbench and recompile the project. The timing analysis script now completes correctly.

**Solution Status**
This issue will never be fixed.

**Pin Planner HDL Syntax Error**
There is an HDL syntax error in Pin Planner-generated top-level design files that contain a DDR or DDR2 SDRAM Controller variation.

**Affected Configurations**
Pin Planner-generated top-level design files that use a design that contains a DDR or DDR2 SDRAM Controller variation.

**Design Impact**
If you import the DDR or DDR2 SDRAM Controller Pin Planner file into Pin Planner and then generate a top-level design file for your design, it contains an HDL syntax error and does not compile in the Quartus II software. You cannot use this top-level design file for IO Assignment Analysis.

**Workaround**
Use the IP Toolbench top-level example design and automatically assigned constraints to verify your pin and IO assignments.

**Solution Status**
This issue will never be fixed.
Revision History

Table 6–1 shows the revision history for the DDR and DDR2 SDRAM High-Performance Controller MegaCore function.

Table 6–1. DDR and DDR2 SDRAM High-Performance Controller MegaCore Function Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.0 SP2</td>
<td>July 2009</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>9.0 SP1</td>
<td>May 2009</td>
<td>Preliminary support for HardCopy III and HardCopy IV E devices.</td>
</tr>
<tr>
<td>9.0</td>
<td>March 2009</td>
<td>- Preliminary support for Arria II GX devices.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Optional support for Altera PHY interface (AFI) Controller-PHY Interface.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Optional multiple controller clock sharing in an SOPC Builder-generated design.</td>
</tr>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>- Reduced controller latency and improved efficiency.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Improved example top-level design.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Support for multiple synchronous controllers in an SOPC Builder-generated design.</td>
</tr>
<tr>
<td>8.0 SP1</td>
<td>July 2008</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>- Preliminary support for Stratix IV devices.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Optional support for self-refresh and power-down commands.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Optional support for auto-precharge read and auto-precharge write commands.</td>
</tr>
</tbody>
</table>

Errata

Table 6–2 shows the issues that affect the DDR and DDR2 SDRAM Controller High-Performance Controllers v9.0 SP2, 9.0 SP1, 9.0, 8.1, 8.0 SP1, and 8.0.

Not all issues affect all versions of the DDR and DDR2 SDRAM Controller High-Performance Controller.

Table 6–2. DDR and DDR2 SDRAM High-Performance Controller MegaCore Function Errata (Part 1 of 2)

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Jul 09</td>
<td>Incorrect User Guide on ACDS</td>
<td>Fixed</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>9.0 SP2</th>
<th>9.0 SP1</th>
<th>9.0</th>
<th>8.1</th>
<th>8.0 SP1</th>
<th>8.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fixed</td>
<td>✔</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>
Table 6–2. DDR and DDR2 SDRAM High-Performance Controller MegaCore Function Errata (Part 2 of 2)

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 May 09</td>
<td>DDR2 Controller Designs with ODT Setting and Registered DIMM Options Enabled Cannot Be Generated</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>Simulation Fails When test_incomplete_writes Signal is Asserted</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>DDR2 Full Rate Controller Designs with Error Correction Coding (ECC) Fail to Meet Timing</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>DDR2 Full Rate Controller Designs in AFI Mode Do Not Meet Specified Maximum Supported Frequency (Fmax)</td>
<td>Fixed</td>
</tr>
<tr>
<td>15 Mar 09</td>
<td>Designs with Error Correction Coding (ECC) Do Not Work After Subsequent Reset</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>Incorrect Controller Latency Information in User Guide</td>
<td>—</td>
</tr>
<tr>
<td>01 Feb 09</td>
<td>Intermittent Read Failure After Calibration</td>
<td>✓</td>
</tr>
<tr>
<td>01 Dec 08</td>
<td>SOPC Builder Does Not Recognize Decimal Points</td>
<td>✓</td>
</tr>
<tr>
<td>01 Nov 08</td>
<td>Inefficient Write Request to An Open Bank</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>Unnecessary Warning During Generation</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>Memory Timing Parameter tWR Is Set Incorrectly</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>Unable to Deliberately Corrupt the ECC Data When Using the Native Interface</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>DDR or DDR2 SDRAM High-Performance Controllers May Not Appear in SOPC Builder</td>
<td>—</td>
</tr>
<tr>
<td>15 Jul 08</td>
<td>Possibility of Calibration Failure</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>Precharge All Command Not Always Issued Before Auto-Refresh Command</td>
<td>—</td>
</tr>
<tr>
<td>15 May 08</td>
<td>RTL Simulation May Fail When Dedicated Memory Clock Outputs Are Selected</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>Gate Level Simulation Fails</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>VHDL Simulation Fails When DDR CAS Latency 2.0 or 2.5 Is Selected</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>Memory Presets Contain Some Incorrect Memory Timing Parameters</td>
<td>✓</td>
</tr>
<tr>
<td>15 Oct 07</td>
<td>Mimic Path Incorrectly Placed</td>
<td>✓</td>
</tr>
<tr>
<td>01 Dec 06</td>
<td>Simulating with the NCSim Software</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>Simulating with the VCS Simulator</td>
<td>✓</td>
</tr>
</tbody>
</table>

Incorrect User Guide on ACDS

The user guide that is on the Altera Complete Design Suite (ACDS) is an out-of-date version.

Affected Configurations

This issue affects no configurations.
Design Impact

There is no design impact.

Workaround

Download the latest DDR and DDR2 SDRAM High-Performance Controller MegaCore Function User Guide from the Altera website.

Solution Status

This issue is fixed in version 9.0 SP2 of the DDR and DDR2 SDRAM High-Performance Controller.

DDR2 Controller Designs with ODT Setting and Registered DIMM Options Enabled Cannot Be Generated

Designs that use DDR2 SDRAM High-Performance Controllers with Memory on-die termination (ODT) setting and Registered DIMM option for Memory format turned on cannot be generated using the MegaWizard interface.

Affected Configurations

This issue affects all designs with DDR2 SDRAM high-performance controllers that have the Memory on-die termination (ODT) setting and Registered DIMM options turned on.

Design Impact

Your design cannot be generated in the MegaWizard interface.

Workaround

Perform the following steps to generate the DDR2 SDRAM High-Performance Controller MegaCore in the Quartus II software:

1. Generate a top variant file in the MegaWizard interface with valid options, for example, RDIMM, ODT disabled, CL 5.

2. After generating, modify the top variant file to the option that you want. In this case, change the value of ODT to a value that you prefer.

   Change the following code:

   ```xml
   // Retrieval info: <PRIVATE name = "mem_odt" value="Disabled" type="STRING" enable="1" />
   ```

   to:

   ```xml
   // Retrieval info: <PRIVATE name = "mem_odt" value="50" type="STRING" enable="1" />
   ```

3. Type the following command in the terminal:

   `qmegawiz -silent <variant file name>`
If you want to generate the core with a simulation model, type:

```
qmegawiz -silent OPTIONAL_FILES=SIM_NETLIST
INTENDED_DEVICE_FAMILY=<family name> <variant file name>
```

For example, if you are using a Stratix III device and your variant file name is `ddr2hp.v`, your command should look like the following:

```
qmegawiz -silent OPTIONAL_FILES=SIM_NETLIST
INTENDED_DEVICE_FAMILY=stratixiii ddr2hp.v
```

**Solution Status**

This issue will be fixed in a future version of the DDR2 SDRAM High-Performance Controller.

**Simulation Fails When test_incomplete_writes Signal is Asserted**

Simulation for DDR and DDR2 SDRAM high-performance controllers fails when `test_incomplete_writes` signal is asserted.

**Affected Configurations**

This issue affects all designs that use DDR and DDR2 SDRAM high-performance controllers with the `MAX_ROW` parameter set to 8191.

**Design Impact**

Your design fails to simulate at test incomplete writes mode when the `test_incomplete_writes` signal is asserted.

**Workaround**

Replace the `reached_max_address` assignment code in the example driver with the following assignment code:

- **Verilog HDL**

  ```
  assign reached_max_address = ((test_dm_pin_mode | test_addr_pin_mode) & (row_addr == MAX_ROW_PIN)) || ((test_seq_addr_mode | test_incomplete_writes_mode) & (col_addr == max_col_value) & (row_addr == MAX_ROW) & (bank_addr == MAX_BANK) & (cs_addr == MAX_CHIPSEL));
  ```

- **VHDL**

  ```
  reached_max_address <= (((test_dm_pin_mode OR test_addr_pin_mode)) AND to_std_logic(((row_addr = MAX_ROW_PIN))) OR (((((test_seq_addr_mode OR test_incomplete_writes_mode) AND to_std_logic(((col_addr = (max_col_value))))) AND to_std_logic(((row_addr = MAX_ROW))) AND to_std_logic(((bank_addr = MAX_BANK)))) AND to_std_logic(((std_logic'(cs_addr) = std_logic'(MAX_CHIPSEL))))));
  ```

**Solution Status**

This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controllers.
DDR2 Full Rate Controller Designs with Error Correction Coding (ECC) Fail to Meet Timing

Some designs with DDR2 SDRAM High-Performance Controllers DRAM High-Performance Controllers at 200MHz that target Stratix II devices do not meet timing on the ECC path at 200MHz.

**Affected Configurations**
This issue affects some designs that use DDR2 SDRAM high-performance controllers that have the **Enable error detection and correction logic** option turned on, targeting Stratix II devices.

**Design Impact**
Your design may not meet timing at 200MHz.

**Workaround**
Add registers for `local_rdata_valid` and `local_rdata` signals at the user logic.

**Solution Status**
This issue will be fixed in a future version of the DDR2 SDRAM High-Performance Controller.

DDR2 Full Rate Controller Designs in AFI Mode Do Not Meet Specified Maximum Supported Frequency (F_{max})

Some designs with the full-rate DDR2 SDRAM High-Performance Controllers in AFI mode do not meet the specified F_{max}.

**Affected Configurations**
This issue affects designs that use full-rate DDR and DDR2 SDRAM high-performance controllers in AFI mode running maximum frequency, targeting Arria II GX, Cyclone III, and Stratix II devices. Designs that target Arria GX, Stratix III, and Stratix IV are not affected.

**Design Impact**
Your design does not meet the required F_{max} in Timing Analysis.

**Workaround**
Use the non-AFI mode instead.

**Solution Status**
This issue is fixed in version 9.0 SP1 of the DDR and DDR2 SDRAM High-Performance Controllers.

Designs with Error Correction Coding (ECC) Do Not Work After Subsequent Reset

Some designs with DDR or DDR2 SDRAM High-Performance controllers do not work with the **Enable error detection and correction logic** option enabled.
**Affected Configurations**
This issue affects all designs that use DDR and DDR2 SDRAM high-performance controllers that have the Enable error detection and correction logic option turned on.

**Design Impact**
Your design does not work properly in both simulation and hardware after the subsequent reset.

**Workaround**
None.

**Solution Status**
This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controllers.

**Incorrect Controller Latency Information in User Guide**
The controller latency information in Tables C1 to C9 in the DDR and DDR2 SDRAM High-Performance Controllers User Guide 8.1 is incorrect.

The correct controller latency for DDR and DDR2 SDRAM high-performance controllers is five for half-rate controller and four for full-rate controller.

**Solution Status**
This issue is fixed in version 9.0 of the DDR and DDR2 SDRAM High-Performance Controllers User Guide.

**Intermittent Read Failure After Calibration**
The ALTMEMPHY megafuction leads to intermittent read failure after calibration.

**Affected Configurations**
This issue affects all designs that use DDR and DDR2 SDRAM high-performance controllers (versions 8.1 and previous) in full-rate mode and DQS-based capture.

**Design Impact**
Your design may fail in hardware at low frequency.

**Workaround**
Apply the patch provided at http://www.altera.com/support/kdb/solutions/rd12182008_673.html, and recompile your design.

**Solution Status**
This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controllers.
SOPC Builder Does Not Recognize Decimal Points

If you assign the PLL clock with a value with decimals, SOPC Builder takes only the whole number and does not recognize the value after the decimal point. When you generate the system, the “The PLL reference clock of <value> does not match the clock frequency input to refclk” error message appears.

Affected Configurations
This issue affects all designs that have a PLL clock value with decimals.

Design Impact
Your system cannot be generated.

Workaround
Ignore the error message, and generate the system by holding down the Ctrl key on the keyboard while clicking Generate in SOPC Builder.

Solution Status
This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controllers.

Inefficient Write Request to An Open Bank

If your design requests consecutive write commands to the same open row, the controller will stall every eight clock cycles. It should be able to accept consecutive write accesses to the same open row until the next auto-refresh command is scheduled.

Affected Configurations
This issue only affects DDR2 SDRAM controllers configured for CAS latency of five or greater.

Design Impact
Your design will not be as efficient as it should be.

Workaround
Reduce the CAS latency setting to four.

Solution Status
This issue is fixed in version 8.1 of the DDR and DDR2 SDRAM High-Performance Controllers.

Unnecessary Warning During Generation

If you have not enabled the Generate simulation model option, you will see the following warning when generating your controller variation:

Warning: <your design directory>/<variation>_auk_ddr_hp_controller_wrapper.vho doesn't exist but should have been created by IPToolbench.
Affected Configurations
This issue affects designs that have the Generate simulation model option turned off.

Design Impact
None. You can ignore this warning.

Workaround
None required.

Solution Status
This issue is fixed in version 8.1 of the DDR and DDR2 SDRAM High-Performance Controllers.

Memory Timing Parameter tWR Is Set Incorrectly
The tWR memory timing parameter is set to twice the number of clock cycles that it should be if the Local interface clock frequency setting is set to Half.

Affected Configurations
This issue affects designs that have the Native interface option turned on.

Design Impact
Your design may be less efficient than expected.

Workaround
Edit the <variation_name>_auk_ddr_hp_controller_wrapper.v file (for both Verilog HDL or VHDL) and change the value assigned to the mem_twr signal to half of the original value, rounding up to the nearest integer. For example, if the MegaWizard interface applied a value of 3 cycles to the tWR parameter, change the assignment from

assign mem_twr = 3'b011;

to

assign mem_twr = 3'b010;

This change will only affect the design in hardware. The simulation model will still use the value set by the MegaWizard interface.

Solution Status
This issue is fixed in version 8.1 of the DDR and DDR2 SDRAM High-Performance Controllers.

Unable to Deliberately Corrupt the ECC Data When Using the Native Interface
When the Native interface option is turned on, you cannot enable the deliberate corruption of ECC data which tests the functionality of the ECC logic. You must choose the Avalon Memory-Mapped interface option to be able to generate corrupted ECC data.
**Affected Configurations**
This issue affects designs that have the Native interface option turned on.

**Design Impact**
You cannot fully test the ECC functionality in the selected configuration.

**Workaround**
Change the local interface protocol to Avalon Memory-Mapped interface.

**Solution Status**
This issue is fixed in version 8.1 of the DDR and DDR2 SDRAM High-Performance Controllers.

---

**DDR or DDR2 SDRAM High-Performance Controllers May Not Appear in SOPC Builder**

In some circumstances, the DDR or DDR2 SDRAM High-Performance Controllers may not appear in SOPC Builder due to an indexing issue.

**Affected Configurations**
This issue affects SOPC Builder designs that use DDR or DDR2 SDRAM High-Performance Controllers.

**Design Impact**
The DDR or DDR2 SDRAM High-Performance Controllers may not appear in SOPC Builder when it is first launched.

**Workaround**
To regenerate the index and make the DDR or DDR2 SDRAM High-Performance Controllers appear, follow these steps:

1. Close the SOPC Builder and the Quartus II software.
2. Delete the C:\Documents and Settings\<username>\altera.quartus\ip_cache directory if you are using Windows or $HOME/altera.quartus/ip_cache if you are using Linux or Solaris.
3. Restart the SOPC Builder and the Quartus II software.

**Solution Status**
This issue is fixed in version 8.1 of the DDR and DDR2 SDRAM High-Performance Controllers.

---

**Possibility of Calibration Failure**

Designs with the DDR or DDR2 SDRAM High-Performance Controller IP created in the Quartus II software version 8.0 that target DDR or DDR2 SDRAM could fail to calibrate correctly in hardware under certain conditions.

**Affected Configurations**
This issue affects all variations and device families.
Design Impact
Your design may fail to operate correctly in hardware.

Workaround
Regenerate the memory controller with the Quartus II software version 8.0 SP1.

Solution Status
This issue is fixed in version 8.0 SP1 of the DDR and DDR2 SDRAM High-Performance Controllers.

Precharge All Command Not Always Issued Before Auto-Refresh Command
If your design has eight chip selects and no reads or writes have happened to the lower four chip selects since the last auto-refresh command, the controller will issue an auto-refresh command without first issuing a precharge all command.

Affected Configurations
This issue only affects controllers with eight chip selects.

Design Impact
Your design may fail to operate correctly.

Workaround
Regenerate your controller instance in the latest version of the DDR and DDR2 SDRAM High-Performance Controller.

Solution Status
This issue is fixed in version 8.0 SP1 of the DDR and DDR2 SDRAM High-Performance Controllers.

RTL Simulation May Fail When Dedicated Memory Clock Outputs Are Selected
The example testbench RTL simulation may not simulate correctly when a dedicated memory clock phase is selected because clock net delay between the PLL and the clock output pins is not modelled in the RTL.

Affected Configurations
This issue affects designs that enable the Use dedicated PLL outputs to drive memory clocks option and set a value for the Dedicated memory clock phase parameter.

Design Impact
The design does not simulate correctly.
Workaround

Add `MEM_CLK_DELAY` to `clk_to_ram` signal at example top-level testbench, to compensate for the on-chip clock net delay to `mem_dqs` which is not present in the RTL simulation.

```
parameter DED_MEM_CLK = 1;
parameter real DED_MEM_CLK_PHASE = <value for dedicated memory clock phase>
parameter real mem_clk_ratio = ((360.0*DED_MEM_CLK_PHASE)/360.0);
parameter MEM_CLK_DELAY = mem_clk_ratio*CLOCK_TICK_IN_PS * (DED_MEM_CLK ? 1 : 0);
wire clk_to_ram0, clk_to_ram1, clk_to_ram2;
assign #(MEM_CLK_DELAY/4.0) clk_to_ram2 = clk_to_sdram[0];
assign #(MEM_CLK_DELAY/4.0) clk_to_ram1 = clk_to_ram2;
assign #(MEM_CLK_DELAY/4.0) clk_to_ram0 = clk_to_ram1;
assign #((MEM_CLK_DELAY/4.0)) clk_to_ram = clk_to_ram0;
//Replace testbench clk_to_ram assignment by adding MEM_CLK_DELAY
//assign clk_to_ram = clk_to_sdram[0];
```

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controllers.

Gate Level Simulation Fails

Gate level simulation of the example design and example testbench fails when Use differential DQS is enabled in the DDR2 High-Performance Controller.

Affected Configurations

This issue affects DDR2 SDRAM High-Performance Controller designs in Stratix III and Stratix IV devices that have the Use differential DQS option enabled.

Design Impact

Gate level simulation of the example design does not behave correctly.

Workaround

You can use the following options:

1. To connect `dqs_n` example top-level design:
   ```
   .mem_dqsn(mem_dqsn)
   ```
2. To connect `dqs_n` in memory model:
   ```
   .DQSN mem_dqsn[index])
   ```

Solution Status

This issue will be fixed in a future version of the DDR2 SDRAM High-Performance Controller.

VHDL Simulation Fails When DDR CAS Latency 2.0 or 2.5 Is Selected

VHDL generated sequencer block for CAS latency 2.0 and 2.5 designs using DDR SDRAM High-Performance Controller results in simulation failure. The issue is due to delta cycle delays on a clock net.
Affected Configurations
This issue affects DDR SDRAM High-Performance Controller CAS latency 2.0 and 2.5 designs.

Design Impact
This issue only affects simulation on VHDL and does not affect the functionality of the design.

Workaround
To workaround this issue, follow these steps:

1. Open the `<variation_name>_phy.vho` file in the project directory.

2. Search for the `altsyncram` instantiation for the postamble block (this can be done by searching for " altsyncram" —note the white space). This should be the `altsyncram` component with a label that includes the word "postamble".

3. Search for the signal that is attached to the clock1 port to find the point in the design where this signal is assigned to (in a test case, this is on line 4043).

4. Change the assignment as shown below. The signal inside not(..) should be the same as the signal on clock0 port of a second instance of the `altsyncram` component which is associated to the read datapath (with "read_dp" in the label).

   ```
   wire_<variation_name>_phy_<variation_name>_phy_alt_mem_phy_sii_<variation_name>_phy_alt_mem_phy_siiInst_<variation_name>_phy_alt_mem_phy_postamble_sii_poa_altsyncram_half_rate_ram_gen_altsyncram_inst_19557_clock1 <= not (wire_<variation_name>_phy_<variation_name>_phy_alt_mem_phy_sii_<variation_name>_phy_alt_mem_phy_pll_sii_pll_19462_c4);
   ```

   This step removes a delta delay for simulation but leaves the code unchanged. The right side of the assignment above is taken as the right side of the assignment to the signal which is previously assigned to the "wire_<variation_name>_phy_<variation_name>_phy_alt_mem_phy_sii_<variation_name>_phy_alt_mem_phy_postamble_sii_poa_altsyncram_half_rate_ram_gen_altsyncram_inst_19557_clock1" signal.

5. If the `<variation_name>_phy` component is recompiled in your simulator, the design should now pass.

Solution Status
This issue will be fixed in a future version of the DDR SDRAM High-Performance Controller.
Memory Presets Contain Some Incorrect Memory Timing Parameters

The memory presets contain incorrect data for the $t_{DSa}$ and $t_{DHa}$ memory timing parameters.

Affected Configurations

This issue affects all configurations.

Design Impact

Timing analysis results for write and address/command paths may be incorrect.

Workaround

Make sure that the memory timing parameters in the MegaWizard Plug-In Manager match the datasheet of the target memory device. The output edge rate and the use of single-ended versus differential DQS may affect certain memory parameters.

Solution Status

This issue will be fixed in a future version of the DDR2 SDRAM High-Performance Controller.

Mimic Path Incorrectly Placed

The Quartus II software may fail to place the mimic path correctly. The report timing script then indicates a timing setup failure on the mimic path.

Affected Configurations

This issue affects all designs.

Design Impact

Your design may fail.

Workaround

Manually edit the following parameter in the autogenerated Synopsis design constraint (.sdc) script to correct the timing analysis:

mimic_shift

Add a value of at least the worst case failed slack to the value already stated in the Synopsis design constraint file.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controllers.

Simulating with the NCSim Software

The DDR and DDR2 SDRAM High-Performance Controller MegaCore functions do not fully support the NCSim software.
**Affected Configurations**
This issue affects all configurations.

**Design Impact**
The design does not simulate.

**Workaround**
Set the \(-relax\) switch for all calls to the VHDL analyzer.

**Solution Status**
This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controllers.

---

**Simulating with the VCS Simulator**
The DDR and DDR2 SDRAM High-Performance Controller MegaCore functions do not fully support the VCS simulator.

**Affected Configurations**
This issue affects all configurations.

**Design Impact**
The design does not simulate.

**Workaround**
The following workarounds exist.

**VHDL**
Change the following code.

- In file \(<variation name>_example_driver.vhd\), change all when statements between lines 333 and 503 from `when std_logic_vector'("bit_pattern")` to `when "bit_pattern"`.

- In file `testbench\<example name>_tb`, change line 191 from `signal zero_one(gMEM_BANK_BITS -1 downto 0) := (0 => '1', others => '0')` to `signal zero_one(gMEM_BANK_BITS -1 downto 0) := ('1', others=> '0')`.

**Verilog HDL**
No changes are necessary. Calls to the Verilog analyzer sets the `+v2k` switch to enable Verilog 2000 constructs.

**Solution Status**
This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controllers.
7. DDR3 SDRAM High-Performance Controller

Revision History

Table 7–1 shows the revision history for the DDR3 SDRAM High-Performance Controller MegaCore function.

For more information about the new features, refer to the DDR3 SDRAM High-Performance Controller MegaCore Function User Guide.

Table 7–1. DDR3 SDRAM High-Performance Controller MegaCore Function Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.0 SP2</td>
<td>July 2009</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>9.0 SP1</td>
<td>May 2009</td>
<td>Preliminary support for HardCopy III and HardCopy IV E devices.</td>
</tr>
<tr>
<td>9.0</td>
<td>March 2009</td>
<td>■ Preliminary support for Arria II GX devices.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Full support for Stratix III devices.</td>
</tr>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>■ Reduced controller latency and improved efficiency.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Improved example top-level design.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Support for multiple synchronous controllers in an SOPC Builder-generated design.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>■ Preliminary support for Stratix IV devices.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Optional support for self-refresh and power-down commands.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Optional support for auto-precharge read and auto-precharge write commands.</td>
</tr>
</tbody>
</table>

Errata

Table 7–2 shows the issues that affect the DDR3 SDRAM Controller High-Performance Controller v9.0 SP2, 9.0 SP1, 9.0, 8.1, and 8.0.

Table 7–2. DDR3 SDRAM High-Performance Controller MegaCore Function Errata (Part 1 of 2)

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Jul 09</td>
<td>Address Mirroring Not Supported By Memory Simulation Model</td>
<td>9.0 SP2 9.0 SP1 9.0 8.1 8.0</td>
</tr>
<tr>
<td></td>
<td>Incorrect User Guide on ACDS</td>
<td>Fixed</td>
</tr>
<tr>
<td>15 Apr 09</td>
<td>Simulation Fails When test_incomplete_writes Signal is Asserted</td>
<td>9.0 SP2 9.0 SP1 9.0 8.1 8.0</td>
</tr>
<tr>
<td></td>
<td>Different Read Data Orders</td>
<td></td>
</tr>
<tr>
<td>15 Mar 09</td>
<td>Memory Preset Parameters Do Not Get Updated</td>
<td>9.0 SP2 9.0 SP1 9.0 8.1 8.0</td>
</tr>
<tr>
<td></td>
<td>Designs with Error Correction Coding (ECC) Do Not Work After Subsequent Reset</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Incorrect Controller Latency Information in User Guide</td>
<td></td>
</tr>
</tbody>
</table>

© 01 July 2009  Altera Corporation  Library Version 9.0  MegaCore IP Library Release Notes and Errata
Address Mirroring Not Supported By Memory Simulation Model

The default memory simulation model does not support address mirroring. When you generate your design in the example testbench with the address mirroring parameter enabled, your simulation fails. To simulate successfully, you must replace the current memory simulation model with a vendor memory model and mirror the address bits in the `<variation name>_example_top_tb.v` or `.vhd` file.

**Affected Configurations**

This issue affects the multiple chip selects DDR3 DIMM which require mirrored address bits.

**Design Impact**

The default memory simulation model does not support DDR3 DIMM multiple chip selects mirrored address bits. Your design fails to simulate.

**Workaround**

Use the vendor memory model and mirror the address bits in the example top for target chip selects by doing the following:

1. Regenerate the DDR3 testbench. After generating, in the top variant file, `<variation name>.v` or `.vhd`, look for the following code:

```vhdl
//Retrieval info: <PRIVATE name = "use_generated_memory_model" 
value="true" type="STRING" enable="1"/>
and change to:

//Retrieval info: <PRIVATE name = "use_generated_memory_model" 
value="false" type="STRING" enable="1"/>
```

2. Download the vendor memory model.

3. For the chip selects that require address mirroring, edit the `<variation name>_example_top_tb.v` or `.vhd` file by performing the following:

   a. Add the following lines:

   ```vhdl
   wire[gMEM_ADDR_BITS - 1:0] a_reversed;
   wire[gMEM_BANK_BITS - 1:0] ba_reversed;
   assign a_reversed[2:0] = a_delayed[2:0];
   assign a_reversed[3] = a_delayed[4];
   assign a_reversed[4] = a_delayed[3];
   assign a_reversed[5] = a_delayed[6];
   ```

---

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Nov 08</td>
<td>Unable to Deliberately Corrupt the ECC Data When Using the Native Interface</td>
<td>9.0 SP2 9.0 SP1 9.0 8.1 8.0 Fixed ✓</td>
</tr>
<tr>
<td></td>
<td>DDR3 SDRAM High-Performance Controller May Not Appear in SOPC Builder</td>
<td>9.0 SP2 9.0 SP1 9.0 8.1 8.0 Fixed ✓</td>
</tr>
</tbody>
</table>
assign a_reversed[6] = a_delayed[5];
assign a_reversed[7] = a_delayed[8];
assign a_reversed[8] = a_delayed[7];
assign a_reversed[gMEM_ADDR_BITS - 1:9] = a_delayed[gMEM_ADDR_BITS - 1:9];
assign ba_reversed[0] = ba_delayed[1];
assign ba_reversed[1] = ba_delayed[0];
assign ba_reversed[gMEM_BANK_BITS - 1:2] = ba_delayed[gMEM_BANK_BITS - 1:2];

b. Locate the following lines:
.ba (ba_delayed),
.addr (a_delayed[14-1: 0]),
and change to:
.ba (ba_reversed),
.addr (a_reversed),

Solution Status
This issue will be fixed in a future version of the DDR3 SDRAM High-Performance Controller.

Incorrect User Guide on ACDS

The user guide that is on the Altera Complete Design Suite (ACDS) is an out-of-date version.

Affected Configurations
This issue affects no configurations.

Design Impact
There is no design impact.

Workaround
Download the latest DDR3 SDRAM High-Performance Controller MegaCore Function User Guide from the Altera website.

Solution Status
This issue is fixed in version 9.0 SP2 of the DDR3 SDRAM High-Performance Controller.

Simulation Fails When test_incomplete_writes Signal is Asserted
Simulation for DDR3 SDRAM high-performance controller fails when test_incomplete_writes signal is asserted.
Affected Configurations

This issue affects all designs that use DDR3 SDRAM high-performance controllers with the MAX_ROW parameter set to 8191.

Design Impact

Your design fails to simulate at test incomplete writes mode when the test_incomplete_writes signal is asserted.

Workaround

Replace the reached_max_address assignment code in the example driver with the following assignment code:

- Verilog HDL

```verilog
assign reached_max_address = ((test_dm_pin_mode | test_addr_pin_mode) & (row_addr == MAX_ROW_PIN)) || ((test_seq_addr_mode | test_incomplete_writes_mode) & (col_addr == (max_col_value)) && (row_addr == MAX_ROW) && (bank_addr == MAX_BANK) && (cs_addr == MAX_CHIPSEL));
```

- VHDL

```vhdl
reached_max_address <= (((test_dm_pin_mode OR test_addr_pin_mode)) AND to_std_logic(((row_addr = MAX_ROW_PIN))))) OR (((((test_seq_addr_mode OR test_incomplete_writes_mode) AND to_std_logic(((col_addr = (max_col_value))))) AND to_std_logic(((row_addr = MAX_ROW)))) AND to_std_logic(((bank_addr = MAX_BANK)))) AND to_std_logic(((std_logic'(cs_addr) = std_logic'(MAX_CHIPSEL))));
```

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM High-Performance Controller.

Different Read Data Orders

A write followed by a read to an odd local address gives a different read data sequence.

Affected Configurations

This issue affects all DDR3 SDRAM high-performance controller designs that read from an odd local address when the local size is 2.

Design Impact

The read data sequence does not appear in your expected order when you read from an odd local address. The DDR3 SDRAM high-performance controller only works in an even starting local address when the local size is 2.

Workaround

Write and read to an even starting address to make sure the read data sequence is the same as the write data.

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM High-Performance Controller.
Memory Preset Parameters Do Not Get Updated

Some memory presets are changed in version 9.0 of the DDR3 SDRAM High-Performance Controller. If you migrate your existing design from version 8.1 to 9.0, your memory preset parameters do not get updated in version 9.0.

**Affected Configurations**
This issue affects all designs that are migrated to version 9.0.

**Design Impact**
The memory preset parameters in your design do not get updated in version 9.0, even if you regenerate the MegaCore function.

**Workaround**
In the MegaWizard GUI, choose any random memory presets, and then reselect your original presets (remember to redo any modifications to the preset such as DQ width, CAS latency, and so on). Click Finish to regenerate the MegaCore function.

**Solution Status**
This issue will be fixed in a future version of the DDR3 SDRAM High-Performance Controller.

Designs with Error Correction Coding (ECC) Do Not Work After Subsequent Reset

Some designs with DDR3 SDRAM High-Performance Controllers do not work with the Enable error detection and correction logic option enabled.

**Affected Configurations**
This issue affects all designs that use DDR3 SDRAM high-performance controllers that have the Enable error detection and correction logic option turned on.

**Design Impact**
Your design does not work properly in both simulation and hardware after the subsequent reset.

**Workaround**
None.

**Solution Status**
This issue will be fixed in a future version of the DDR3 SDRAM High-Performance Controllers.

Incorrect Controller Latency Information in User Guide

The controller latency information in Tables B2 and B3 in the DDR3 SDRAM High-Performance Controller User Guide 8.1 is incorrect.

The correct controller latency for DDR3 SDRAM high-performance controller is five.
Solution Status
This issue is fixed in version 9.0 of the DDR3 SDRAM High-Performance Controller User Guide.

Unable to Deliberately Corrupt the ECC Data When Using the Native Interface

When the Native interface option is turned on, you cannot enable the deliberate corruption of ECC data which tests the functionality of the ECC logic. You must choose the Avalon Memory-Mapped interface option to be able to generate corrupted ECC data.

Affected Configurations
This issue affects designs that have the Native interface option turned on.

Design Impact
You cannot fully test the ECC functionality in the selected configuration.

Workaround
Change the local interface protocol to Avalon Memory-Mapped interface.

Solution Status
This issue is fixed in version 8.1 of the DDR3 SDRAM High-Performance Controller.

DDR3 SDRAM High-Performance Controller May Not Appear in SOPC Builder

In some circumstances, the DDR3 SDRAM High-Performance Controller may not appear in SOPC Builder due to an indexing issue.

Affected Configurations
This issue affects SOPC Builder designs that use DDR3 SDRAM High-Performance Controller.

Design Impact
The DDR3 SDRAM High-Performance Controller may not appear in SOPC Builder when it is first launched.

Workaround
To regenerate the index and make the DDR3 SDRAM High-Performance Controller appear, follow these steps:

1. Close the SOPC Builder and the Quartus II software.
2. Delete the $C:\Documents and Settings\<username>\altera.quartus\ip_cache$ directory if you are using Windows or $HOME/altera.quartus/ip_cache$ if you are using Linux or Solaris.
3. Restart the SOPC Builder and the Quartus II software.

Solution Status
This issue is fixed in version 8.1 of the DDR3 SDRAM High-Performance Controller.
Revision History

Table 8–1 shows the revision history for the FFT MegaCore function.

For more information about the new features, refer to the FFT MegaCore Function User Guide.

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.0 SP1</td>
<td>May 2009</td>
<td>Preliminary support for HardCopy III and HardCopy IV E devices.</td>
</tr>
<tr>
<td>9.0</td>
<td>March 2009</td>
<td>Preliminary support for Arria II GX devices.</td>
</tr>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>Full support for Stratix III devices.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>Full support for Cyclone III devices.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Preliminary support for Stratix IV devices</td>
</tr>
</tbody>
</table>

Errata

Table 8–2 shows the issues that affect the FFT MegaCore function v9.0, 8.1, and 8.0.

Not all issues affect all versions of the FFT MegaCore function.

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 Mar 09</td>
<td>Example Design Fails Compilation</td>
<td>✓</td>
</tr>
<tr>
<td>01 Nov 08</td>
<td>Display Symbol Button in IP Toolbench is Missing</td>
<td>✓ ✓ —</td>
</tr>
<tr>
<td>01 Oct 07</td>
<td>Cannot Find Memory Initialization File if Not in Project Directory</td>
<td>✓ ✓ ✓</td>
</tr>
<tr>
<td></td>
<td>Floating-Point FFT Produces Non-Zero Output</td>
<td>✓ ✓ ✓</td>
</tr>
<tr>
<td>01 Dec 06</td>
<td>Simulation Errors—Synopsys VCS</td>
<td>✓ ✓ ✓</td>
</tr>
<tr>
<td></td>
<td>Simulation Errors—Incorrect Results</td>
<td>✓ ✓ ✓</td>
</tr>
<tr>
<td></td>
<td>Simulation Errors—MATLAB Model Mismatch</td>
<td>✓ ✓ ✓</td>
</tr>
<tr>
<td></td>
<td>Gate-Level Simulations</td>
<td>✓ ✓ ✓</td>
</tr>
</tbody>
</table>

Example Design Fails Compilation

The example top-level VHDL design with bit-reversal module (variable streaming FFT) cannot run compilation.

Affected Configurations

This issue affects variable streaming FFT designs.
Design Impact
There is no design impact.

Workaround
This issue has no workaround.

Solution Status
This issue will be fixed in a future version of the FFT MegaCore function.

Display Symbol Button in IP Toolbench is Missing
The Display Symbol button in IP Toolbench does not appear, even though the screenshot in the user guide implies it should appear.

Affected Configurations
This issue affects all designs.

Design Impact
There is no design impact.

Workaround
This issue has no workaround.

Solution Status
This issue will be fixed in a future version of the FFT MegaCore function.

Cannot Find Memory Initialization File if Not in Project Directory
The Quartus II software cannot find the memory initialization files (HEX files) required by the design and issues a critical warning of the form:

Critical Warning: Can't find Memory Initialization File or Hexadecimal (Intel-Format) File C:/temp/mlab_test/fir_test0_coef_0.hex -- setting all initial values to 0

Affected Configurations
This issue is observed when the generated IP files are not in the same directory as your project setting files .qsf and .qpf files. For example, if your project involves many submodules and each submodule resides in a separate subdirectory.

Design Impact
The Quartus II software issues critical warnings for the missing files and generates a functionally incorrect netlist because of the missing memory initialization files.

Workaround
Add the path of the folder containing your generated IP files to the user libraries parameter in the .qsf file. For example, if your top-level project directory is c:/myprojects/bigSystem and you have generated the FFT in c:/myprojects/bigSystem/FFTmodule/.
In your project’s .qsf file (in `c:/myprojects/bigSystem`), look for a line that starts
`set_global_assignment -name USER_LIBRARIES ...
Append the IP directory `c:/myprojects/bigSystem/FFTmodule` in the following code:

```
set_global_assignment -name USER_LIBRARIES
"C:/altera/72/ip/fft/lib;C:/myprojects/bigSystem/FFTmodule"
```

After you save your changes, recompile your project and check that the critical
warning is no longer displayed.

**Solution Status**
The issue will be fixed a future version of the FFT MegaCore function.

---

**Floating-Point FFT Produces Non-Zero Output**

When a DC signal is input to a floating-point variable streaming configuration of the
FFT, the output is an impulse response, where bin 0 contains the magnitude of the
impulse response and the other bins should be 0. The value in bin 0 is correct.
However, non-zero values are encountered in the other bins. These values have a
magnitude in the range of 10 to 39. More specifically, the exponent is zero, and the
mantissa contains a non-zero number. The IEEE754 floating point specification refers
to a number with a zero exponent and non-zero mantissa as denormalized. The
floating point FFT does not support denormalized numbers, therefore any number
with a zero exponent can be considered to have a zero mantissa.

Under these conditions, the MATLAB simulation model also produces output with a
zero exponent and non-zero mantissa. However, the value of the mantissa does not
match the value in simulation.

**Affected Configurations**
The issue affects all floating point variable streaming configurations of the FFT.

**Design Impact**
The design compiles but gives incorrect results under some circumstance. The
MATLAB simulation model does not match the simulation results.

**Workaround**
The mantissa bits should be zeroed if the exponent is zero.

**Solution Status**
The issue will be fixed in a future version of the FFT MegaCore function.

---

**Simulation Errors—Synopsys VCS**

When you use NativeLink to perform an RTL simulation using the generated Verilog
HDL testbench in the VCS simulator, you see the following error:

```
Error: VCS: to support this construct
Error: VCS: operator '**'.
```
**Affected Configurations**
This issue affects all Verilog HDL configurations.

**Design Impact**
There is no design impact; the design compiles correctly.

**Workaround**
In the Verilog HDL testbench `<variation name>_tb.v`, replace the power of operator `'*'` with the calculated value. Alternatively, compile with the `+v2k` option in the VCS simulator.

**Solution Status**
This issue will be fixed in a future version of the FFT MegaCore function.

**Simulation Errors—Incorrect Results**
When the input is defined as $N$ bit wide, the permissible input range is from $-2^{N-1} + 1$ to $2^{N-1} - 1$. If the input contains the value $-2^{N-1}$, the HDL output is incorrect, and does not match the MATLAB simulation result.

**Affected Configurations**
This issue affects all configurations.

**Design Impact**
The design compiles but gives incorrect results.

**Workaround**
If you expect your input signal to contain the value $-2^{N-1}$, you should add a block in front of the FFT, which maps the value $-2^{N-1}$ to $-2^{N-1} + 1$.

**Solution Status**
This issue will be fixed in a future version of the FFT MegaCore function.

**Simulation Errors—MATLAB Model Mismatch**
For one particular FFT parameter combination, the HDL output does not match the MATLAB simulation results (for some frames of data).

HDL simulation results are scaled down by a factor of two compared to the MATLAB simulation results. The exponent value produced by the HDL simulation is one less than the output of the MATLAB simulations. When the exponent is taken into account, the MATLAB and the HDL version may differ by one LSB.

**Affected Configurations**
This issue affects the following parameter combination:

- Transform length: 64
- I/O data flow: burst architecture
■ FFT engine architecture: quad output
■ Number of parallel engines: 2

**Design Impact**
There is no design impact; the design compiles and operates correctly.

**Workaround**
This issue has no workaround.

**Solution Status**
This issue will be fixed in a future version of the FFT MegaCore function.

**Gate-Level Simulations**

The testbench provided with the FFT MegaCore function is not suitable for gate-level simulations. The testbench assumes zero delays in post-fitting simulation models. Therefore, running gate-level simulations using the testbench may produce incorrect simulation results.

**Affected Configurations**
This issue affects all configurations.

**Design Impact**
There is no design impact; the design compiles correctly.

**Workaround**
Provide appropriate input and output constraints using the Quartus II Assignments Editor and create a testbench that matches these requirements.

**Solution Status**
This issue will be fixed in a future version of the FFT MegaCore function.
9. FIR Compiler

Revision History

Table 9–1 shows the revision history for the FIR Compiler.

For information about the new features, refer to the FIR Compiler User Guide.

Table 9–1. FIR Compiler Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.0 SP1</td>
<td>May 2009</td>
<td>Preliminary support for HardCopy III and HardCopy IV E devices.</td>
</tr>
<tr>
<td>9.0</td>
<td>March 2009</td>
<td>Preliminary support for Arria II GX.</td>
</tr>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>Full support for Stratix III.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Withdrawn support for UNIX.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>Full support for Cyclone III devices.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Preliminary support for Stratix IV devices.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Added option to automatically select memory block size for coefficient storage.</td>
</tr>
</tbody>
</table>

Errata

Table 9–2 shows the issues that affect the FIR Compiler v9.0, v8.1, and v8.0.

Not all issues affect all versions of the FIR Compiler.

Table 9–2. FIR Compiler Errata

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 Jun 09</td>
<td>Simulation Fails for the Coefficient Reloadable Filters</td>
<td>✔️ ✔️ ✔️</td>
</tr>
<tr>
<td>15 Apr 09</td>
<td>Incorrect Results for Multi-Bit Serial or Interpolation with Signed Binary Fractional</td>
<td>✔️ ✔️ ✔️</td>
</tr>
<tr>
<td></td>
<td>Cannot Select M9K Data or Coefficient Storage When Device Family is Cyclone III</td>
<td>✔️ ✔️ ✔️</td>
</tr>
<tr>
<td>15 Mar 09</td>
<td>Incorrect Output for Signed Binary Fractional Multi-Bit Serial or Interpolation Filter</td>
<td>✔️ ✔️ ✔️</td>
</tr>
<tr>
<td></td>
<td>Bit Serial Filter With 32-Bit Coefficients Does Not Work</td>
<td>Fixed ✔️ ✔️ ✔️</td>
</tr>
<tr>
<td></td>
<td>Half-Band Decimator and Symmetric Interpolator Do Not Support Unsigned Type</td>
<td>Fixed ✔️ ✔️ ✔️</td>
</tr>
<tr>
<td></td>
<td>Signed Binary Fraction Results in Output Bit Width Mismatch</td>
<td>Fixed ✔️ ✔️ ✔️</td>
</tr>
<tr>
<td></td>
<td>Incorrect Screenshot in the User Guide</td>
<td>Fixed ✔️ ✔️ ✔️</td>
</tr>
<tr>
<td>01 Nov 08</td>
<td>Some Gate Level Simulations are Incorrect</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>Cannot Find Memory Initialization File if Not in Project Directory</td>
<td>—</td>
</tr>
<tr>
<td>01 Oct 08</td>
<td>Block Memory Incorrectly Used When Logic Storage Selected</td>
<td>✔️ ✔️ ✔️</td>
</tr>
<tr>
<td>01 Oct 07</td>
<td>Simulation Result Incorrect Using MCV Interpolation Filters</td>
<td>✔️ ✔️ ✔️</td>
</tr>
<tr>
<td>01 May 07</td>
<td>Reloadable Coefficient Filters Fail for Some MCV Filters</td>
<td>✔️ ✔️ ✔️</td>
</tr>
<tr>
<td>01 Dec 06</td>
<td>Quartus II Simulation Vector File Not Generated</td>
<td>✔️ ✔️ ✔️</td>
</tr>
</tbody>
</table>
Simulation Fails for the Coefficient Reloadable Filters

The reloadable coefficient filters might not produce the right output if you use the IP functional simulation models for simulation.

Affected Configurations
This issue affects the reloadable coefficient filters.

Design Impact
The produced output does not match the expected output.

Workaround
None.

Solution Status
This issue will be fixed in a future version of the FIR Compiler.

Incorrect Results for Multi-Bit Serial or Interpolation with Signed Binary Fractional

Incorrect results when Structure is set to Distributed Arithmetic: Multi-Bit Serial Filter or the Rate Specification is set to Interpolation, and Signed Binary Fractional is specified for the data type.

Affected Configurations
Multi-bit serial structure or interpolation rate specification with the signed binary fractional data type.

Design Impact
The FIR filter produces incorrect results.

Workaround
Avoid using the multi-bit serial structure or interpolation filter type with signed binary fractional data types.

Solution Status
This issue will be fixed in a future version of the FIR Compiler.

Cannot Select M9K Data or Coefficient Storage When Device Family is Cyclone III

If you try to set M9K for Data Storage or Coefficient Storage when the Device Family is set to Cyclone III, an error message reports incorrectly that Cyclone III does not support M9K memory.

Affected Configurations
Any configuration when the Device Family is set to Cyclone III.

Design Impact
You cannot select M9K for Data Storage.
Workaround
Change the Device Family to Stratix III, select M9K for Data Storage (or Coefficient Storage), then change the Device Family back to Cyclone III.

Solution Status
This issue will be fixed in a future version of the FIR Compiler.

Incorrect Output for Signed Binary Fractional Multi-Bit Serial or Interpolation Filter

The FIR Compiler output data is incorrect if you choose Signed Binary Fractional data type with Multi-Bit Serial Filter structure or Interpolation rate specification.

Affected Configurations
Configurations that have a signed binary fractional data type with either a multi-bit structure or an interpolation filter rate specification.

Design Impact
The output data is incorrect.

Workaround
Avoid using a multi-bit serial structure or an interpolation filter rate specification with signed binary fractional data types.

Solution Status
This issue will be fixed in a future version of the FIR Compiler.

Bit Serial Filter With 32-Bit Coefficients Does Not Work

The generated netlist may be incorrect if the maximum coefficient width is 32.

Affected Configurations
All distributed arithmetic based architectures (fully serial, multi-bit serial, and fully parallel).

Design Impact
The generated netlist is incorrect.

Workaround
Limit the input precision to 31 bits and change the coefficient storage to logic cells. Alternatively, you can use a multicycle variable architecture which gives correct results for 32-bit coefficients.

Solution Status
This issue is fixed in version 9.0 of the FIR Compiler.
Half-Band Decimator and Symmetric Interpolator Do Not Support Unsigned Type

The half-band decimator and symmetric interpolator filters do not support unsigned input data type.

**Affected Configurations**
This issue affects half-band decimator and symmetric interpolator filter architectures.

**Design Impact**
The FIR filter produces incorrect results.

**Workaround**
The half-band decimator and symmetric interpolator filter architectures require signed input data types. To use unsigned data, design the filter with input ports 1-bit larger than the original value and connect the MSB bit of the \texttt{ast\_sink\_data} input port to 0.

**Solution Status**
This issue is fixed in version 9.0 of the FIR Compiler.

Signed Binary Fraction Results in Output Bit Width Mismatch

For signed binary fraction data types, some FIR filter variations fail Quartus II compilation and simulation model generation.

**Affected Configurations**
This issue affects all configurations with signed binary fraction data types.

**Design Impact**
Compilation fails in the Quartus II software.

**Workaround**
This issue is related to a user interface issue. In some cases, when you reopen the variation file using IP Toolbench and regenerate the filter, the issue is resolved. If it still fails compilation, use one of the other data types (Signed Binary or Unsigned Binary).

**Solution Status**
This issue is fixed in version 9.0 of the FIR Compiler.

Incorrect Screenshot in the User Guide

The IP Toolbench screenshot in Figure 2-3 of the user guide is out-of-date and shows the Display Symbol option although this feature is no longer supported.

**Solution Status**
This issue is fixed in version 9.0 of the *FIR Compiler User Guide*. 
Some Gate Level Simulations are Incorrect

The testbench for testing gate level simulation sometimes stimulates the FIR instantiation incorrectly and, as a result, the behavior of the testbench is not as expected.

Affected Configurations

This issue can potentially affect any gate-level simulation using the provided testbench.

Design Impact

The test bench behaves incorrectly.

Workaround

Apply a delay of a quarter of a clock cycle to the source startofpacket and endofpacket Avalon-ST signals to make the timing consistent with the other data and control signals.

Solution Status

This issue is fixed in version 8.1 of the FIR Compiler.

Cannot Find Memory Initialization File if Not in Project Directory

The Quartus II software cannot find the memory initialization (.hex) files required by the design and issues a critical warning of the form:

Critical Warning: Can't find Memory Initialization File or Hexadecimal (Intel-Format) File C:/temp/mlab_test/fir_test0_coef_0.hex -- setting all initial values to 0

Affected Configurations

This issue is observed when the generated IP files are not in the same directory as your project setting files .qsf and .qpf. For example, if your project involves many submodules and each submodule resides in a separate subdirectory.

Design Impact

The Quartus II software issues critical warnings for the missing files and generates a functionally incorrect netlist due to the missing memory initialization files.

Workaround

Add the path of the folder containing your generated IP files to the user libraries parameter in the Quartus II settings (.qsf) file. For example, if your top-level project directory is C:/myprojects/mySystem and you have generated the FIR filter in C:/myprojects/mySystem/FIRmodule/, look for a line in the .qsf file that starts with set_global_assignment -name USER_LIBRARIES ...

Append the IP directory C:/myprojects/bigSystem/FIRmodule as shown in the following code:

set_global_assignment -name USER_LIBRARIES "C:/altera/<ver>/ip/fir_compiler/lib;C:/myprojects/mySystem/FIRmodule"
After you save your changes, recompile your project and check that the critical warning is no longer displayed.

**Solution Status**
This issue is fixed in version 8.1 of the FIR Compiler.

**Block Memory Incorrectly Used When Logic Storage Selected**
For some instances of the FIR Compiler MegaCore function, if you select logic-based storage for data and coefficients, it is possible that the results of synthesis may include some block memory.

**Affected Configurations**
Configurations with FIR storage set to logic elements.

**Design Impact**
An unwanted block memory is used.

**Workaround**
Turn off Auto Shift Register Replacement in the Quartus II More Analysis and Synthesis Settings dialog box. This dialog box can be accessed by clicking More Settings in the Analysis & Synthesis Settings page of the Settings dialog box accessed from the Assignments menu in the Quartus II software.

**Solution Status**
This issue will be fixed in a future version of the FIR Compiler.

**Simulation Result Incorrect Using MCV Interpolation Filters**
Some multicycle variable interpolation filters with high interpolation factors may generate incorrect output.

**Affected Configurations**
This issue affects MCV interpolation filters with high interpolation factors and forced non-symmetric implementation where the pipelining level is set to greater than 1 for higher $f_{\text{MAX}}$.

**Design Impact**
The produced output does not match the expected output.

**Workaround**
Change the pipelining level to 1. This change may result in lower $f_{\text{MAX}}$ but the filter output will match the expected output.

**Solution Status**
This issue will be fixed in a future version of the FIR Compiler.
Reloadable Coefficient Filters Fail for Some MCV Filters

Some reloadable coefficient filters with multicycle variable architecture do not produce the right output when a new set of coefficients is reloaded.

**Affected Configurations**

This error is observed in some of the reloadable coefficient MCV filters.

**Design Impact**

The produced output does not match the expected output when the new coefficient set is reloaded.

**Workaround**

There are two separate problems which may cause this failure. If your target device is Cyclone III, change the device to Stratix II or Stratix III in the FIR Compiler GUI and regenerate the filter. (Your device selection in the Quartus II project should stay the same.) If the coefficient storage is set to logic cells, change to a block memory (such as M512, M9K, or Auto).

**Solution Status**

This issue will be fixed in a future version of the FIR Compiler.

Quartus II Simulation Vector File Not Generated

FIR Compiler does not create a vector file for Quartus II simulation.

**Affected Configurations**

This issue affects all configurations.

**Design Impact**

The design can be compiled, but there is no automatically generated vector file testbench available to simulate the design in the Quartus II software.

**Workaround**

Use NativeLink to simulate the VHDL testbench instead.

**Solution Status**

This issue will be fixed in a future version of the FIR Compiler.
10. HyperTransport

Revision History

Table 10–1 shows the revision history for the HyperTransport MegaCore function. For more information about the new features, refer to the HyperTransport MegaCore Function User Guide.

Table 10–1. HyperTransport MegaCore Function Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.0</td>
<td>March 2009</td>
<td>■ Maintenance release</td>
</tr>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>■ Maintenance release</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>■ Maintenance release</td>
</tr>
</tbody>
</table>

Errata

No known issues affect the HyperTransport MegaCore function in v9.0, v8.1, or v8.0.
11. NCO

Revision History

Table 11–1 shows the revision history for the NCO MegaCore function.

For information about the new features, refer to the NCO MegaCore Function User Guide.

Table 11–1. NCO MegaCore Function Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.0 SP1</td>
<td>May 2009</td>
<td>Preliminary support for HardCopy III and HardCopy IV E devices.</td>
</tr>
</tbody>
</table>
| 9.0     | March 2009 | ■ Preliminary support for Arria II GX.  
          |            | ■ Added frequency hopping design example.        |
| 8.1     | November 2008 | ■ Full support for Stratix III.  
          |            | ■ Withdrawn support for UNIX.                    |
| 8.0     | May 2008   | ■ Full support for Cyclone III devices.  
          |            | ■ Preliminary support for Stratix IV devices.    |

Errata

Table 11–2 shows the issues that affect the NCO MegaCore function v9.0, v8.1, and v8.0.

Not all issues affect all versions of the NCO MegaCore function.

Table 11–2. NCO MegaCore Function Errata

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 Mar 09</td>
<td>Cannot Implement Multiplier-Based Architecture using Multipliers for Arria II GX</td>
<td>✔️</td>
</tr>
<tr>
<td></td>
<td>Resource Estimate Displays LEs Instead of ALUTs for Arria II GX</td>
<td>✔️</td>
</tr>
<tr>
<td></td>
<td>Warning Message Displayed Twice</td>
<td>✔️</td>
</tr>
<tr>
<td>01 Oct 07</td>
<td>Mismatches Between Multiplier-Based MATLAB and RTL Models</td>
<td>✔️ ✔️ ✔️</td>
</tr>
<tr>
<td>01 May 07</td>
<td>Mismatches Between the MATLAB and RTL Models</td>
<td>✔️ ✔️ ✔️</td>
</tr>
<tr>
<td>01 Dec 06</td>
<td>The MATLAB Simulation File Cannot be Used on UNIX</td>
<td>✔️</td>
</tr>
</tbody>
</table>

Cannot Implement Multiplier-Based Architecture using Multipliers for Arria II GX

You cannot implement a multiplier-based architecture using dedicated multipliers for the Arria II GX device family.

Affected Configurations

Multiplier-based architectures with the target device family set to Arria II GX.
Design Impact
You cannot select the Use Dedicated Multipliers option in the Implementation tab of the Parameter Setting dialog box when the target device family is set to Arria II GX.

Workaround
None.

Solution Status
This issue will be fixed in a future version of the NCO MegaCore function.

Resource Estimate Displays LEs Instead of ALUTs for Arria II GX
The Resource Estimate tab of the Parameter Setting dialog box displays LEs instead ALUTs for the Arria II GX device family.

Affected Configurations
Multiplier-based architectures with the target device family set to Arria II GX.

Design Impact
None.

Workaround
None.

Solution Status
This issue will be fixed in a future version of the NCO MegaCore function.

Warning Message Displayed Twice
If you change the Clock Rate units to mHz in the Parameter Setting dialog box a warning message is displayed. After closing the warning message, if you then click on both the Clock Rate and the Desired Output Frequency boxes, two separate warning messages with the same content are displayed.

Affected Configurations
All configurations.

Design Impact
None.

Workaround
Close both of the warning messages.

Solution Status
This issue will be fixed in a future version of the NCO MegaCore function.
Mismatches Between Multiplier-Based MATLAB and RTL Models

For the multiplier-based architecture with throughput = 1 (output every clock cycle), there can be mismatches between the outputs of the MATLAB model and the RTL design for values of magnitude precision. These mismatches seem to be rounding errors for very large values.

Affected Configurations

Multiplier-based architecture with throughput = 1 of the NCO MegaCore function.

Design Impact

Comparison of the output values from the MATLAB model and RTL design during testing may show mismatches. However, the error margin is small in both absolute and relative terms. For example, the MATLAB model calculates -536,870,910, whereas the RTL calculates -536,870,911.

Workaround

The RTL design works correctly, but comparison between the MATLAB model and the RTL cannot be done automatically.

Solution Status

This issue will be fixed in a future version of the NCO MegaCore function.

Mismatches Between the MATLAB and RTL Models

For the multiplier-based architecture with throughput = ½ (output every 2nd clock cycle), and for the serial CORDIC architecture, there can be mismatches between the outputs of the MATLAB model and the RTL for certain parameter combinations. These mismatches occur because some initial output values are not covered by either the MATLAB model or the RTL design, while the other values match.

Affected Configurations

Multiplier-based architecture with halved throughput and serial CORDIC architectures of the NCO MegaCore function.

Design Impact

Automatic comparison of the output values from the MATLAB model and RTL design during testing may show mismatches.

Workaround

The RTL design works correctly, but comparison between MATLAB model and RTL cannot be done automatically.

Solution Status

This issue will be fixed in a future version of the NCO MegaCore function.
The MATLAB Simulation File Cannot be Used on UNIX

The MATLAB simulation file generated by a NCO MegaCore function can only be used on Windows and Linux.

**Affected Configurations**

UNIX configurations.

**Design Impact**

You cannot simulate a NCO MegaCore function in MATLAB on UNIX.

**Workaround**

None.

**Solution Status**

UNIX configurations are not supported by version 8.1 or later.
12. Nios II Processor

Revision History

Table 12–1 shows the revision history for the Nios II Processor MegaCore function.

For more information about the new features, refer to the Nios II Processor Reference Handbook. For information about new features and errata in the Nios II Embedded Design Suite, refer to the Nios II Embedded Design Suite Release Notes and Errata.

Table 12–1. Nios II Processor Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.0</td>
<td>March 2009</td>
<td>No changes</td>
</tr>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>No changes</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>■ Added memory management unit (MMU). Optionally enabled in Nios II MegaWizard** Plug-In Manager flow. Requires third party operating system support.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Added memory protection unit (MPU). Optionally enabled in Nios II MegaWizard Plug-In Manager flow. Supported by the Nios II software build tools.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Added support for advanced exceptions to catch illegal instructions, illegal memory access, and division errors.</td>
</tr>
</tbody>
</table>

Errata

Table 12–2 shows the issues that affect the Nios II Processor in versions 8.0 through 9.0.

Not all issues affect all versions of the Nios II Processor.

Table 12–2. Nios II Processor Errata

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 Mar 09</td>
<td>Design Assistant Error on Clock Signal Source in HardCopy Designs</td>
<td>9.0  8.1</td>
</tr>
<tr>
<td>01 Nov 08</td>
<td>Nios II MMU Micro TLBs Not Flushed</td>
<td>8.0 SP1 8.0</td>
</tr>
<tr>
<td>15 Jul 08</td>
<td>Hardware Breakpoints Not Supported with Nios II MMU and MPU</td>
<td></td>
</tr>
<tr>
<td>01 Apr 08</td>
<td>Nios II Ports Created Incorrectly</td>
<td>9.0  8.1</td>
</tr>
<tr>
<td>15 Oct 07</td>
<td>Errors Adding Custom Instruction to the Nios II Processor</td>
<td>9.0  8.1</td>
</tr>
<tr>
<td>01 Jun 06</td>
<td>Double-Precision Floating-Point Operations With Floating-Point Custom Instructions (1)</td>
<td>9.0  8.1</td>
</tr>
</tbody>
</table>

Note to Table 12–2: (1) This issue is documented in Appendix D. Floating Point Custom Instructions in the Nios II Custom Instruction User Guide.
Design Assistant Error on Clock Signal Source in HardCopy Designs

When you run the Quartus II Design Assistant on a HardCopy III or HardCopy IV design, the following error message might appear:

Rule C106: Clock signal source should not drive registers that are triggered by different clock edges ; clk ;

This error occurs because your HardCopy III or HardCopy IV design incorporates a Nios II/s processor core with a logic element (LE)-based multiplier.

Affected Configurations

HardCopy III and HardCopy IV designs incorporating the Nios II/s processor core with an LE-based multiplier.

Design Impact

You cannot compile a HardCopy III or HardCopy IV design incorporating the Nios II/s processor core with an LE-based multiplier.

Workaround

There is currently no workaround for this issue.

Solution Status

This issue will be fixed in a future release of the Nios II processor core.

Nios II MMU Micro TLBs Not Flushed

The micro translation lookaside buffer (TLB) entries in the Nios II MMU are not always flushed when required. This leads to unpredictable results with software using the MMU.

Affected Configurations

Nios II systems with the MMU enabled.

Workaround

Upgrade to the Altera Complete Design Suite version 8.1 or later.

Solution Status

Fixed in version 8.1.

Hardware Breakpoints Not Supported with Nios II MMU and MPU

Enabling the MMU and MPU sets the Nios II instruction and data address to 32 bits. The JTAG debug core, however, leaves the address equal to the size of the Nios II instruction and data master address signals. Because of this address size mismatch, data breakpoints cannot be set on a virtual address when using the MMU, or set on an address outside the address space when using the MPU.

Affected Configurations

Nios II systems with the MMU or MPU enabled.
**Workaround**
There is no workaround available at this time.

**Solution Status**
This issue will be fixed in a future release of the Nios II processor core.

**Nios II Ports Created Incorrectly**
A threading issue between SOPC Builder and the Nios II MegaWizard interface occasionally causes HDL file analysis to fail. This creates all ports as std_logic input with width 1.

**Affected Configurations**
Nios II processor systems with custom instructions.

**Design Impact**
Design fails to run in ModelSim.

**Workaround**
After adding your custom instruction, close and relaunch SOPC Builder.

**Solution Status**
This issue will be fixed in a future release of the Altera Complete Design Suite.

**Errors Adding Custom Instruction to the Nios II Processor**
You might get spurious errors after adding custom instruction slave ports through the Nios II MegaWizard interface.

**Affected Configurations**
Any Nios II system featuring custom instructions.

**Design Impact**
No design impact. The error messages are benign.

**Workaround**
Save your system in SOPC Builder. Close and then relaunch SOPC Builder.
13. PCI Compiler

Revision History

Table 13–1 shows the revision history for the PCI Compiler.

For more information about the new features, refer to the PCI Compiler User Guide.

Table 13–1. PCI Compiler Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.0 SP2</td>
<td>July 2009</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>9.0 SP1</td>
<td>May 2009</td>
<td>Preliminary support for HardCopy III and HardCopy IV E devices.</td>
</tr>
<tr>
<td>9.0</td>
<td>March 2009</td>
<td>Preliminary support for Arria II GX devices.</td>
</tr>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>Preliminary support for Stratix IV devices.</td>
</tr>
</tbody>
</table>

Errata

Table 13–2 shows the issues that affect the PCI Compiler v9.0 SP2, v9.0 SP1, 9.0, 8.1, and 8.0.

Not all issues affect all versions of the PCI Compiler.

Table 13–2. PCI Compiler MegaCore Function Errata

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Jul 09</td>
<td>Incorrect User Guide on ACDS</td>
<td>Fixed</td>
</tr>
<tr>
<td>15 May 09</td>
<td>F1152 Packages for HardCopy III and HardCopy IV-E Not Supported</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>Wirebond Packages for HardCopy III and HardCopy IV-E Not Supported</td>
<td>✓</td>
</tr>
<tr>
<td>15 Mar 09</td>
<td>Designs With Stratix III Devices Fail to Meet Timing</td>
<td>—</td>
</tr>
</tbody>
</table>
Table 13–2. PCI Compiler MegaCore Function Errata

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Nov 08</td>
<td>Designs With Stratix IV Devices Fail to Meet Timing</td>
<td>9.0 SP2</td>
</tr>
<tr>
<td></td>
<td>Device Support Incorrect in User Guide</td>
<td>9.0 SP1</td>
</tr>
<tr>
<td></td>
<td>Full Compilation Fails for Some Cyclone III Devices When Using</td>
<td>9.0</td>
</tr>
<tr>
<td></td>
<td>Recommended PCI Pin Assignments</td>
<td>8.1</td>
</tr>
<tr>
<td></td>
<td>TimeQuest Timing Analysis Fails for Stratix III Devices When Using</td>
<td>8.0</td>
</tr>
<tr>
<td></td>
<td>Recommended PCI Constraints at Lower Seed Number</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TimeQuest Timing Analysis Fails for HardCopy II Devices When Using</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Recommended PCI Constraints</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TimeQuest Timing Analysis Fails for Some Arria GX and Stratix II</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Devices When Using Recommended PCI Constraints</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TimeQuest Timing Analysis Fails for Some Cyclone Devices When Using</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Recommended PCI Constraints</td>
<td></td>
</tr>
<tr>
<td>15 May 08</td>
<td>PCI Bus Hangs on Write Transactions to the I/O BAR Address Spaces</td>
<td></td>
</tr>
</tbody>
</table>

**Incorrect User Guide on ACDS**

The user guide that is on the Altera Complete Design Suite (ACDS) is an out-of-date version.

**Affected Configurations**

This issue affects no configurations.

**Design Impact**

There is no design impact.

**Workaround**

Download the latest *PCI Compiler User Guide* from the Altera website.

**Solution Status**

This issue is fixed in version 9.0 SP2 of the PCI Compiler.

**F1152 Packages for HardCopy III and HardCopy IV-E Not Supported**

PCI Compiler does not support F1152 packages for HardCopy III and HardCopy IV-E.

**Affected Configuration**

All PCI Compiler configurations using the F1152 packages for HardCopy III and HardCopy IV-E.

**Design Impact**

The PCI Compiler designs with F1152 packages for HardCopy III and HardCopy IV-E fail to compile.
Workaround
None.

Solution Status
This issue will be fixed in a future version of the PCI Compiler.

Wirebond Packages for HardCopy III and HardCopy IV-E Not Supported
PCI Compiler does not support wirebond packages for HardCopy III and HardCopy IV-E.

Affected Configuration
All PCI Compiler configurations using the wirebond packages for HardCopy III and HardCopy IV-E.

Design Impact
The PCI Compiler designs with wirebond packages for HardCopy III and HardCopy IV-E fail to compile.

Workaround
None.

Solution Status
This issue will be fixed in a future version of the PCI Compiler.

Designs With Stratix III Devices Fail to Meet Timing
Timing fails when using Stratix III devices with any core combination at 66 MHz.

Affected Configuration
All PCI Compiler designs targeting the Stratix III EP3SL340 device family with the slowest speed grade, C4.

Design Impact
The PCI Compiler designs with some Stratix III devices may fail to meet timing.

Workaround
None.

Solution Status
This issue is fixed in version 9.0 of the PCI Compiler.

Designs With Stratix IV Devices Fail to Meet Timing
Timing fails when using Stratix IV devices with any core combination at 66 MHz.
Affected Configuration
All PCI Compiler designs targeting the Stratix IV devices with the slowest speed grade, C4.

Design Impact
The PCI Compiler designs with some Stratix IV devices may fail to meet timing.

Workaround
None.

Solution Status
This issue will not be fixed.

Device Support Incorrect in User Guide
The PCI Compiler User Guide 8.0 states an incorrect level of support for the following devices: Arria GX and Cyclone III family devices.
The correct device support level is full support.

Solution Status
This issue is fixed in version 8.1 of the PCI Compiler User Guide.

Full Compilation Fails for Some Cyclone III Devices When Using Recommended PCI Pin Assignments
A full compilation in the Quartus II software fails when using the recommended PCI pin assignments for the following Cyclone III devices: EP3C16Q240C8, EP3C25Q240C8, 3C40F780, 3C40Q240C8, and 3C120F780.
The Quartus II software displays the following error message:
Pin <PCI pinout name> is incompatible with I/O bank 1. It uses I/O standard 3.0-V PCI, which has VCCIO requirement of 3.0V. That requirement is incompatible with bank’s VCCIO setting or other output or bidirectional pins in the bank using VCCIO 3.3V.

Affected Configuration
All designs targeting the following Cyclone III devices: EP3C16Q240C8, EP3C25Q240C8, 3C40F780, 3C40Q240C8, and 3C120F780.

Workaround
Use the pin assignments generated during the fitting stage instead of the recommended PCI pin assignments. When adding the PCI constraints, use the option -no_pinouts to omit the recommended PCI pin assignments.

Design Impact
You cannot compile the design.
Solution Status
This issue is fixed in version 8.1 of the PCI Compiler.

TimeQuest Timing Analysis Fails for Stratix III Devices When Using Recommended PCI Constraints at Lower Seed Number

The TimeQuest timing analysis fails for Stratix III devices when using the recommended PCI constraints at lower seed number, and affects both slow and fast timing models.

Affected Configuration
All PCI Compiler designs with Stratix III devices.

Design Impact
The PCI Compiler designs with Stratix III devices may not meet timing requirements.

Workaround
Add one line of additional assignment to the Quartus settings file (.qsf) according to the PCI Compiler core selection.

For MT64:

```text
set_instance_assignment -name AUTO_PACKED_REGISTERS_STRATIXII OFF -to "pci_mt64:pci_mt64_inst|pcimt64_pk:parity_Chk|serr_or_*"
```
For MT32:

```
set_instance_assignment -name AUTO_PACKED_REGISTERS_STRATIXII OFF -to "pci_mt32:pci_mt32_inst|pcimt32_pk:parity_Chk|serr_or_*"
```

For T64:

```
set_instance_assignment -name AUTO_PACKED_REGISTERS_STRATIXII OFF -to "pci_t64:pci_t64_inst|pcit64_pk:parity_Chk|serr_or_*"
```

For T32:

```
set_instance_assignment -name AUTO_PACKED_REGISTERS_STRATIXII OFF -to "pci_t32:pci_t32_inst|pcit32_pk:parity_Chk|serr_or_*"
```

**Solution Status**

This issue is fixed in version 8.1 of the PCI Compiler.

---

**TimeQuest Timing Analysis Fails for HardCopy II Devices When Using Recommended PCI Constraints**

The TimeQuest timing analysis fails for HardCopy II devices when using the recommended PCI constraints.

**Affected Configuration**

All PCI Compiler designs with HardCopy II devices.

**Design Impact**

The PCI Compiler designs with HardCopy II devices may not meet timing requirements.

**Workaround**

Remove these two lines from the `<project_name/pci_name>.sdc` file before running the TimeQuest timing analysis.

```
set_input_delay -clock PCI_CLOCK -max 0 <reset_signal_name>
set_input_delay -clock PCI_CLOCK -min 100 < reset_signal_name >
```

**Solution Status**

This issue is fixed in version 8.1 of the PCI Compiler.

---

**TimeQuest Timing Analysis Fails for Some Arria GX and Stratix II Devices When Using Recommended PCI Constraints**

The TimeQuest timing analysis fails when using the recommended PCI constraints for the following Arria GX device: 1AGX90EF1152C6 and Stratix II devices: 2S130F780C5, 2S130F1020C5, and 2S130F1508C5, and affects only the slow timing model.

**Affected Configuration**

All PCI Compiler designs targeting the following Arria GX device: 1AGX90EF1152C6 and Stratix II devices: 2S130F780C5, 2S130F1020C5, and 2S130F1508C5.
Design Impact
The PCI Compiler designs with some Arria GX and Stratix II devices may not meet timing requirements.

Workaround
Use the fast timing model for TimeQuest timing analysis.

Solution Status
This issue is fixed in version 8.1 of the PCI Compiler.

TimeQuest Timing Analysis Fails for Some Cyclone Devices When Using Recommended PCI Constraints
The TimeQuest timing analysis fails when using the recommended PCI constraints for the following Cyclone devices: C4F400C7 and C20F324C8.

Affected Configuration
All PCI Compiler designs targeting the following Cyclone devices: C4F400C7 and C20F324C8.

Design Impact
The PCI Compiler designs with some Cyclone devices may not meet timing requirements.

Workaround
None.

Solution Status
This issue is fixed in version 8.1 of the PCI Compiler.

PCI Bus Hangs on Write Transactions to the I/O BAR Address Spaces
During write transactions to the I/O BAR Address spaces, the PCI bus hangs.

Affected Configuration
PCI Compiler designs that use the I/O BAR settings.

Design Impact
Transactions go to an infinite retry loop whenever a write transaction is initiated to the I/O BAR address space after a read transaction.

Workaround
Apply the patch provided at www.altera.com/support/kdb/solutions/rd04242008_431.html, regenerate your SOPC Builder system and recompile in the Quartus II software.
Alternatively, upgrade to version 8.0 of the Quartus II software.
Solution Status

This issue is fixed in version 8.0 of the PCI Compiler.
Revision History

Table 14–1 shows the revision history for the PCI Express Compiler.

For complete information about the new features, refer to the *PCI Express Compiler User Guide*.

### Table 14–1. PCI Express Compiler Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.0 SP2</td>
<td>July 2009</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>9.0 SP1</td>
<td>May 2009</td>
<td>Preliminary support for HardCopy III and HardCopy IV E devices.</td>
</tr>
</tbody>
</table>
| 9.0     | March 2009 | **Major release.** Introduces preliminary support for the Gen1 PCI Express protocol in Arria II GX devices in both the soft and hard IP implementations.  
          |            | **Introduces Gen2 support for the PCI Express protocol in a hard IP implementation for Stratix IV GX devices.**                                
          |            | **Introduces support for the Avalon Memory-Mapped (Avalon-MM) interface for the hard IP implementation in SOPC Builder.**                      
          |            | **Introduces reconfiguration block for the hard IP implementation to dynamically update read-only configuration space registers.**               
          |            | **Provides enhancements to the Altera-provided design example.**                                                                              |
| 8.1     | November 2008 | **Major release.** Introduces full support for root port designs in the Stratix IV GX devices and full support for endpoint or root port Gen2 ×8 designs in the Stratix IV GX devices.  
          |            | **Existing 8.0 PCI Express MegaCore functions targeting Stratix IV GX devices must be regenerated with the PCI Express 8.1 Compiler prior to compilation in the Quartus II software 8.1 or higher.**                                      
          |            | **The pinout of the 8.1 variant has changed. When regenerating an 8.0 PCI Express variant with version 8.1 of the PCI Express Compiler, there are two differences in the application signal interface:**  
          |            | - There is a new input pin, *gxb_powerdown*. The transceiver calibration module uses *gxb_powerdown* in Stratix II GX, Stratix IV GX, and Arria GX devices. It must be grounded if unused.  
          |            | - The input pin, *aer_msi*, which is only used for the root port variants, has been removed from the top-level of endpoint designs that use the hard IP implementation. |
| 8.0 SP1 | July 2008  | Maintenance release.                                                                                                                        |
| 8.0     | May 2008   | **Major release.** Introduces a hard IP implementation of the PCI Express Compiler with an Avalon Streaming (Avalon-ST) interface. Provides support for Gen2 endpoints. |
| 7.2 SP3 | April 2008 | Maintenance release.                                                                                                                        |
| 7.2 SP2 | January 2008 | Maintenance release.                                                                                                                        |
| 7.2 SP1 | December 2007 | Corrected error in SOPC Builder Avalon-MM base address assignments for PCI Express BARs.                                                      |
| 7.2     | October 2007 | Avalon-ST application interface.                                                                                                          |
|         |            | Single clock domain for Avalon Memory-Mapped (Avalon-MM) application interface.                                                            |
Errata

Table 14–2 shows the issues that affect the PCI Express Compiler in v9.0 SP1, v9.0, v8.1, and v8.0.

Not all issues affect all versions of the PCI Express Compiler.

Table 14–2. PCI Express Compiler Errata  (Part 1 of 3)

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Jul 09</td>
<td>When Using the Avalon-MM interface, Disabling the Master Bus Does Not Stop Requests</td>
<td>9.0 SP2 9.0 SP1 9.0 8.1 8.0 SP1 8.0</td>
</tr>
<tr>
<td></td>
<td>An Error Might Occur in Logging a Poisoned TLP</td>
<td></td>
</tr>
<tr>
<td></td>
<td>The tx_cred Signal Indicates Incorrect Non-Posted Credits Available for the Soft IP Implementation</td>
<td>Fixed 9.0 SP2 9.0 SP1 9.0 8.1 8.0 SP1 8.0</td>
</tr>
<tr>
<td></td>
<td>Hard IP Implementation Returns 0x00 when the Interrupt Pin Register Is Read</td>
<td>Fixed 9.0 SP2 9.0 SP1 9.0 8.1 8.0 SP1 8.0</td>
</tr>
<tr>
<td>15 Jun 09</td>
<td>PCI Express Compiler User Guide Provides Incorrect Speed Grade Information for Gen1</td>
<td>9.0 SP2 9.0 SP1 9.0 8.1 8.0 SP1 8.0</td>
</tr>
<tr>
<td>15 May 09</td>
<td>The tx_cred Signal Indicates Incorrect Non-Posted Credits Available in Hard IP Implementation</td>
<td>9.0 SP2 9.0 SP1 9.0 8.1 8.0 SP1 8.0</td>
</tr>
<tr>
<td></td>
<td>Description of the Completion Side Band Signals and Error Handling in the PCI Express Compiler User Guide Is Incomplete</td>
<td>9.0 SP2 9.0 SP1 9.0 8.1 8.0 SP1 8.0</td>
</tr>
<tr>
<td></td>
<td>The Receive Direction Transaction Layer Routing Rules are Incomplete in PCI Express Compiler User Guide</td>
<td>9.0 SP2 9.0 SP1 9.0 8.1 8.0 SP1 8.0</td>
</tr>
<tr>
<td></td>
<td>A x1 or x4 Soft IP Variation Might Incorrectly Issue a NAK</td>
<td>— Fixed 9.0 SP2 9.0 SP1 9.0 8.1 8.0 SP1 8.0</td>
</tr>
<tr>
<td></td>
<td>You Cannot Use the MegaWizard Plug-In Manager to Edit the SERDES in the Hard IP Implementation of the PCI Express MegaCore Function</td>
<td>— Fixed 9.0 SP2 9.0 SP1 9.0 8.1 8.0 SP1 8.0</td>
</tr>
<tr>
<td>15 Apr 09</td>
<td>Gate-Level Simulation Fails for Hard IP Variations</td>
<td>9.0 SP2 9.0 SP1 9.0 8.1 8.0 SP1 8.0</td>
</tr>
<tr>
<td>15 Mar 09</td>
<td>Incorrect Link Training for Stratix IV GX Gen2 ×8 Hard IP Implementation</td>
<td>9.0 SP2 9.0 SP1 9.0 8.1 8.0 SP1 8.0</td>
</tr>
<tr>
<td></td>
<td>The tx_cred Signal Indicates Incorrect Non-Posted Credits Available for the Soft IP Implementation</td>
<td>9.0 SP2 9.0 SP1 9.0 8.1 8.0 SP1 8.0</td>
</tr>
<tr>
<td></td>
<td>Guidelines for Passing the PCI Express Electrical Gold Test on the v2.0 Compliance Base Board (CBB)</td>
<td>9.0 SP2 9.0 SP1 9.0 8.1 8.0 SP1 8.0</td>
</tr>
<tr>
<td></td>
<td>Endpoints Using the Hard IP Implementation Incorrectly Handle CfgRd0</td>
<td>9.0 SP2 9.0 SP1 9.0 8.1 8.0 SP1 8.0</td>
</tr>
<tr>
<td></td>
<td>Endpoints Using the Soft IP Implementation Incorrectly Handle CfgRd0</td>
<td>— — Fixed 9.0 SP2 9.0 SP1 9.0 8.1 8.0 SP1 8.0</td>
</tr>
<tr>
<td></td>
<td>The Hard IP Implementation of the PCI Express Compiler May Be Unable to Exit the Disable State at the Gen2 Rate</td>
<td>9.0 SP2 9.0 SP1 9.0 8.1 8.0 SP1 8.0</td>
</tr>
<tr>
<td></td>
<td>Timing Closure for Chaining DMA Design Example Gen1×8 in Stratix IV C3 and C4 Speed Grades</td>
<td>9.0 SP2 9.0 SP1 9.0 8.1 8.0 SP1 8.0</td>
</tr>
</tbody>
</table>
Table 14–2. PCI Express Compiler Errata  (Part 2 of 3)

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 Mar 09</td>
<td>The ×8 Soft IP Implementation of PCI Express MegaCore Function Only Supports 4 KByte Expansion ROM BAR</td>
<td>— Fixed ✓ ✓ ✓ ✓ ✓</td>
</tr>
<tr>
<td></td>
<td>The Description of cfg_devcsr[31:0] in the PCI Express Compiler User Guide is Incorrect</td>
<td>✓ ✓ ✓ ✓ — —</td>
</tr>
<tr>
<td></td>
<td>Adding Two PCI Express Components to an SOPC Builder System May Cause a System Error</td>
<td>✓ ✓ ✓ ✓ ✓ ✓</td>
</tr>
<tr>
<td></td>
<td>License File for Soft IP Implementation of the PCI Express Compiler Does Not Work</td>
<td>— — Fixed ✓ — —</td>
</tr>
<tr>
<td></td>
<td>EDA Netlist Writer Does Not Write Netlist for Hard IP Implementation of PCI Express</td>
<td>— — Fixed ✓ — —</td>
</tr>
<tr>
<td></td>
<td>Stratix IV Projects with Pin Assignments Specified Using the Pin Planner May Fail Quartus II Compilation</td>
<td>— — Fixed ✓ — —</td>
</tr>
<tr>
<td></td>
<td>Simulation Fails when Using ModelSim AE for Stratix II GX MegaCore Functions with the Avalon-ST or Descriptor/Data Interfaces</td>
<td>— — Fixed ✓ — —</td>
</tr>
<tr>
<td></td>
<td>The Chaining DMA Design Example May Issue DMA Write Requests that Violate the 4 KByte Boundary Rule in the VHDL Version</td>
<td>— — Fixed ✓ ✓ ✓</td>
</tr>
<tr>
<td></td>
<td>Design Example in Hardware Might Require the RC Slave Module</td>
<td>— — Fixed ✓ ✓ ✓</td>
</tr>
<tr>
<td></td>
<td>Root Port BFM in Version 8.1 of the PCI Express Testbench is not Backwards Compatible</td>
<td>— — Fixed ✓ ✓ ✓</td>
</tr>
<tr>
<td>01 Nov 08</td>
<td>Incorrect Connection of SOPC Builder Interrupt Sources to PCI Express Components</td>
<td>✓ ✓ ✓ ✓ ✓ ✓</td>
</tr>
<tr>
<td></td>
<td>PCI Express Avalon-MM Tx Interface Deadlocks on a Read Request</td>
<td>— — — Fixed ✓ ✓</td>
</tr>
<tr>
<td></td>
<td>Unable to Compile the Example Design Successfully in Quartus II when using ECRC Forwarding</td>
<td>— — Fixed ✓ ✓</td>
</tr>
<tr>
<td>15 Aug 08</td>
<td>Chaining DMA Design Example Forwards Tx ECRC with Incorrect Alignment</td>
<td>— — — Fixed ✓ ✓</td>
</tr>
<tr>
<td>15 Jul 08</td>
<td>User Guide Incorrectly Documents the Number of Address Pages</td>
<td>— — — Fixed ✓ ✓</td>
</tr>
<tr>
<td></td>
<td>User Guide Incorrectly Documents rx_st_data and tx_st_data in 128-Bit Mode</td>
<td>— — — Fixed ✓ ✓</td>
</tr>
<tr>
<td></td>
<td>Address Translation Update Can Corrupt Outstanding Reads for MegaCore Functions Created in SOPC Builder</td>
<td>— — Fixed ✓ ✓ ✓</td>
</tr>
<tr>
<td></td>
<td>SOPC Builder does not Support Legacy Interrupts for PCI Express</td>
<td>— — — — Fixed ✓</td>
</tr>
</tbody>
</table>
When Using the Avalon-MM interface, Disabling the Master Bus Does Not Stop Requests

For PCI Express MegaCore functions using the Avalon-MM interface, clearing the bus master enable bit (bit 2 of the type 0 configuration space register at address 0x4), does not prevent the SOPC Builder endpoint from issuing upstream transactions.

Affected Configurations
This issue affects PCI Express MegaCore functions that use the Avalon-MM interface.

Workaround
Do not allow the software application to disable the master bus.

Solution Status
This issue will be fixed in a future version of the PCI Express MegaCore function.

An Error Might Occur in Logging a Poisoned TLP

When there is a poisoned TLP and automatic error reporting (AER) is enabled and the error is not masked, an error can occur in logging the poisoned TLP into the header log of the AER capability structure. The error occurs if there is an additional incoming packet immediately behind the poisoned TLP. When the error occurs, the TLP header long will be corrupt.

Affected Configurations
This issue affects all variants of the PCI Express MegaCore function when AER is enabled.

Workaround
You can mask the poisoned TLP error type so that it is not included in the error log. Alternatively, you can ignore the poisoned TLP errors that are logged.

Solution Status
This issue will be fixed in a future version of the PCI Express MegaCore function.
The tx_cred Signal Indicates Incorrect Non-Posted Credits Available for the Soft IP Implementation

For the Avalon Streaming (Avalon-ST) interface the tx_cred bus fields that indicate the available non-posted data credits (tx_cred[20:18]) and non-posted header credits (tx_cred[17:15]) can falsely indicate zero available credits when there really are credits available.

Affected Configurations
This issue affects the hard IP implementation of the PCI Express MegaCore function and the soft IP implementation that uses the Avalon-ST interface.

Workaround
You can disregard the tx_cred signal for non-posted header/data. The PCI Express Megacore function always does an accurate check of the available Tx credits available before starting transmission of a transaction layer packet (TLP) in order to obey the flow control protocol. If transmission of a TLP is held due to a lack of credits, the tx_st_ready signal will be deasserted.

Solution Status
This issue is fixed for the soft IP implementation in Quartus II Release 9.0 sp2.

Hard IP Implementation Returns 0x00 when the Interrupt Pin Register Is Read

For hard IP implementations of the PCI Express MegaCore function, when software reads the configuration space interrupt pin register, offset 0x3d, a value of 0x00 is returned instead of 0x01 which indicates legacy interrupt INTA is used by this function.

Affected Configurations
This issue affects hard IP implementations of the PCI Express compiler in the Stratix IV and Arria II GX device families.

Workaround
If possible, software should ignore the value returned with the interrupt pin register is read and assume a value of 0x01 instead. Alternatively, the register value can be altered by using the PCI Express reconfiguration block. Refer to the “PCI Express Reconfiguration Block” section of the PCI Express Compiler User Guide. Specifically, as noted in Table 4-9, the interrupt pin register value is set by bits [3:1] at address 0x97 of the PCI Express reconfiguration block.

Solution Status
This issue is fixed in Quartus II Release 9.0 sp2.

PCI Express Compiler User Guide Provides Incorrect Speed Grade Information for Gen1

Version 9.0 of the PCI Express Compiler User Guide incorrectly states that the Stratix IV GX hard IP Gen1 PCI Express MegaCore function is not available in the –4 speed grade; however, the PCI Express MegaCore function is available in the –4 speed grade for Gen1 variants.
Affected Configurations
This is a documentation error only.

Workaround
No workaround is required.

Solution Status
This issue will be fixed in a future version of the PCI Express Compiler User Guide.

The tx_cred Signal Indicates Incorrect Non-Posted Credits Available in Hard IP Implementation
For the Avalon Streaming (Avalon-ST) interface the tx_cred bus fields that indicate the available non-posted data credits (tx_cred[20:18]) and non-posted header credits (tx_cred[17:15]) can falsely indicate zero available credits when there really are credits available.

Affected Configurations
This issue affects the hard IP implementation of the PCI Express MegaCore function.

Workaround
You can disregard the tx_cred signal for non-posted header/data. The PCI Express Megacore function always does an accurate check of the available Tx credits available before starting transmission of a transaction layer packet (TLP) in order to obey the flow control protocol. If transmission of a TLP is held due to a lack of credits, the tx_st_ready signal will be deasserted.

Solution Status
This issue will be fixed in a future release of the PCI Express MegaCore function.

Description of the Completion Side Band Signals and Error Handling in the PCI Express Compiler User Guide is Incomplete
The descriptions of the cpl_err signals in “Completion Side Band Signals” on page 5-34 is incomplete. In addition, the definition of completer abort in Table4-36 on page 4-54 specifies the wrong bit of the cpl_err vector. This error is reported on cpl_error. The complete and corrected descriptions are given below.
## Transaction Layer

Table 14–3 describes errors detected by the transaction layer.

### Table 14–3. Errors Detected by the Transaction Layer (Part 1 of 3)

<table>
<thead>
<tr>
<th>Error</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
</table>
| Poisoned TLP received    | Uncorrectable (non-fatal) | This error occurs if a received transaction layer packet has the EP poison bit set.  
The received TLP is presented passed to the application and the application layer logic must take application appropriate action in response to the poisoned TLP. In PCI Express 1.1, this error is treated as an advisory error. |
| ECRC check failed        | Uncorrectable (non-fatal) | This error is caused by an ECRC check failing despite the fact that the transaction layer packet is not malformed and the LCRC check is valid.  
The MegaCore function handles this transaction layer packet automatically. If the TLP is a non-posted request, the MegaCore function generates a completion with completer abort status. In all cases the TLP is deleted in the MegaCore function and not presented to the application layer. |
| Unsupported request      | Uncorrectable (non-fatal) | This error occurs whenever a component receives any of the following unsupported requests:  
- Completion transaction for which the requester ID does not match the bus/device.  
- Unsupported message.  
- A type 1 configuration request transaction layer packet for the TLP from the PCIe link.  
- A locked memory read (MEMRDLK) on native endpoint.  
- A locked completion transaction.  
- A 64-bit memory transaction in which the 32 MSBs of an address are set to 0.  
- A memory or I/O transaction for which there is no BAR match.  
- A poisoned configuration write request (CfgWr0)  
If the TLP is a non-posted request, the MegaCore function generates a completion with unsupported request status. In all cases the TLP is deleted in the MegaCore function and not presented to the application layer. |
| Completion timeout       | Uncorrectable (non-fatal) | This error occurs when a request originating from the application layer does not generate a corresponding completion transaction layer packet within the established time. It is the responsibility of the application layer logic to provide the completion timeout mechanism. The completion timeout should be reported from the transaction layer using the cpl_err[0] signal. |
| Completer abort          | Uncorrectable (non-fatal) | The application layer reports this error using the cpl_err[2] signal when it aborts receipt of a transaction layer packet. |
Unexpected completion (non-fatal)

This error is caused by an unexpected completion transaction. The MegaCore function handles the following conditions:

- The requester ID in the completion packet does not match the configured ID of the endpoint.
- The completion packet has an invalid tag number. (Typically, the tag used in the completion packet exceeds the number of tags specified.)
- The completion packet has a tag that does not match an outstanding request.
- The completion packet for a request that was to I/O or configuration space has a length greater than 1 dword.
- The completion status is Configuration Retry Status (CRS) in response to a request that was not to configuration space.

In all of the above cases, the TLP is not presented to the application layer; the MegaCore function deletes it.

Other unexpected completion conditions can be detected by the application layer and reported through the use of the cpl_err[2] signal. For example, the application layer can report cases where the total length of the received successful completions do not match the original read request length.

Receiver overflow (fatal)

This error occurs when a component receives a transaction layer packet that violates the FC credits allocated for this type of transaction layer packet. In all cases the MegaCore function deletes the TLP and it is not presented to the application layer.

Flow control protocol error (FCPE) (fatal)

This error occurs when a component does not receive update flow control credits within the 200 μs limit.

Malformed TLP (fatal)

This error is caused by any of the following conditions:

- The data payload of a received transaction layer packet exceeds the maximum payload size.
- The TD field is asserted but no transaction layer packet digest exists, or a transaction layer packet digest exists but the TD bit of the PCI Express request header packet is not asserted.
- A transaction layer packet violates a byte enable rule. The MegaCore function checks for this violation, which is considered optional by the PCI Express specifications.
- A transaction layer packet in which the type and length fields do not correspond with the total length of the transaction layer packet.
- A transaction layer packet in which the combination of format and type is not specified by the PCI Express specification.
- A request specifies an address/length combination that causes a memory space access to exceed a 4 KByte boundary. The MegaCore function checks for this violation, which is considered optional by the PCI Express specification.
- Messages, such as Assert_INTx, power management, error signaling, unlock, and Set_Slot_power_limit, must be transmitted across the default traffic class.
Table 14–3. Errors Detected by the Transaction Layer (Part 3 of 3)

<table>
<thead>
<tr>
<th>Error</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Malformed TLP (cont)</td>
<td>Uncorrectable (fatal)</td>
<td>A transaction layer packet that uses an uninitialized virtual channel. The MegaCore function deletes the malformed TLP; it is not presented to the application layer.</td>
</tr>
</tbody>
</table>

Note to Table 14–3:
(1) Considered optional by the PCI Express Base Specification Revision 1.0a, 1.1 or 2.0.

Completion Side Band Signals

Table 14–5 describes the signals that comprise the completion side band for the Avalon-ST interface. The MegaCore function provides a completion error interface that the application can use to report errors, such as programming model errors, to it. When the application detects an error, it can assert the appropriate cpl_err bit to tell the MegaCore function what kind of error to log. The MegaCore function sets the appropriate status bits for the error in the configuration space, and automatically sends error messages in accordance with the PCI Express Base Specification. Note that the application is responsible for sending the completion with the appropriate completion status value for non-posted requests. Refer to “Error Handling” on page 4-53 for information on errors that are automatically detected and handled by the MegaCore Function.

Table 14–4. Completion Signals for Avalon-ST (Part 1 of 3)

<table>
<thead>
<tr>
<th>Signal</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>cpl_err[6:0]</td>
<td>I</td>
<td>Completion error. This signal reports completion errors to the configuration space. When an error occurs, the appropriate signal is asserted for one cycle.</td>
</tr>
<tr>
<td>cpl_err[0]: Completion timeout error with recovery. This signal should be asserted when a master-like interface has performed a non-posted request that never receives a corresponding completion transaction after the 50 ms timeout period when the error is correctable. The MegaCore function automatically generates an advisory error message that is sent to the root complex.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>cpl_err[1]: Completion timeout error without recovery. This signal should be asserted when a master-like interface has performed a non-posted request that never receives a corresponding completion transaction after the 50 ms time-out period when the error is not correctable. The MegaCore function automatically generates a non-advisory error message that is sent to the root complex.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>cpl_err[2]: Completer abort error. The application asserts this signal to respond to a posted or non-posted request with a completer abort (CA) completion. In the case of a non-posted request, the application generates and sends a completion packet with completer abort (CA) status to the requestor and then asserts this error signal to the MegaCore function. The MegaCore function automatically sets the error status bits in the configuration space register and sends error messages in accordance with the PCI Express Base Specification.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
■ cpl_err[3]: Unexpected completion error. This signal must be asserted when an application layer master block detects an unexpected completion transaction. Many cases of unexpected completions are detected and reported internally by the transaction layer of the MegaCore function. For a list of these cases, refer to “Errors Detected by the Transaction Layer” on page 4-54.

■ cpl_err[4]: Unsupported request error for posted TLP. The application asserts this signal to treat a posted request as an unsupported request (UR). The MegaCore function automatically sets the error status bits in the configuration space register and sends error messages in accordance with the PCI Express Base Specification. Many cases of unsupported requests are detected and reported internally by the transaction layer of the MegaCore function. For a list of these cases, refer to “Errors Detected by the Transaction Layer” on page 4-54.

■ cpl_err[5]: Unsupported request error for non-posted TLP. The application asserts this signal to respond to a non-posted request with an unsupported request (UR) completion. In this case, the application sends a completion packet with the unsupported request status back to the requestor, and asserts this error signal to the MegaCore function. The MegaCore automatically sets the error status bits in the configuration space register and sends error messages in accordance with the PCI Express Base Specification. Many cases of unsupported requests are detected and reported internally by the transaction layer of the MegaCore function. For a list of these cases, refer to “Errors Detected by the Transaction Layer” on page 4-54.

■ cpl_err[6]: Log header. When asserted, logs err_desc_func0 header. Used in both the soft IP and hard IP implementation of the MegaCore function that use the Avalon-ST interface.

When asserted, the TLP header is logged in the AER header log register if it is the first error detected. When used, this signal should be asserted at the same time as the corresponding cpl_err error bit (2, 3, 4, or 5). In the soft IP implementation, the application presents the TLP header to the MegaCore function on the err_desc_func0 bus. In the hard IP implementation, the application presents the header to the MegaCore function by writing the following values to 4 LMI registers before asserting cpl_err[6]:

- lmi_addr: 12’h81C, lmi_din: err_desc_func0[127:96]
- lmi_addr: 12’h820, lmi_din: err_desc_func0[95:64]
- lmi_addr: 12’h824, lmi_din: err_desc_func0[63:32]
- lmi_addr: 12’h828, lmi_din: err_desc_func0[31:0]

Refer to the LMI Signals—HARD IP Implementation in the PCI Express Compiler User Guide for more information about LMI signalling.

For the ×8 soft IP, only bits [3:1] of cpl_err are available. For the ×1, ×4 soft IP implementation and all widths of the hard IP implementation, all bits are available.
Errata

Affected Configurations
This is a documentation error only.

Workaround
No workaround is required.

Solution Status
This issue will be fixed in a future version of the PCI Express Compiler User Guide.

The Receive Direction Transaction Layer Routing Rules are Incomplete in PCI Express Compiler User Guide

The Transaction Layer Routing Rules given for the receive direction in the PCI Express Compiler User Guide are incomplete. The complete text is given below.

In the receive direction (from the PCI Express link), memory and I/O requests that match the defined base address register (BAR) contents and vendor-defined messages with or without data route to the receive interface. The application layer logic processes the requests and generates the read completions, if needed.

Affected Configurations
This is a documentation error only.

Workaround
No workaround is required.

Solution Status
This issue will be fixed in a future version of the PCI Express Compiler User Guide.

A ×1 or ×4 Soft IP Variation Might Incorrectly Issue a NAK

In some unusual circumstances, a ×1 soft IP implementation of the PCI Express MegaCore function or a ×4 soft IP implementation used in a ×1 slot or it might incorrectly issue a NAK to a valid TLP which has no LCRC error or framing error.

Table 14–4. Completion Signals for Avalon-ST (Part 3 of 3)

<table>
<thead>
<tr>
<th>Signal</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>err_desc_func0[127:0]</td>
<td>I</td>
<td>TLP Header corresponding to a cpl_err. Logged by the MegaCore function when cpl_err[6] is asserted. This signal is only available for the ×1 and ×4 soft IP implementation. In the hard IP implementation, this information can be written to the AER header log register through the LMI interface. If AER is not implemented in your variation this signal bus should be tied to a constant value, for example all 0’s.</td>
</tr>
<tr>
<td>cpl_pending</td>
<td>I</td>
<td>Completion pending. The application layer must assert this signal when a master block is waiting for completion, for example, when a transaction is pending. If this signal is asserted and low power mode is requested, the MegaCore function waits for the deassertion of this signal before transitioning into low-power state.</td>
</tr>
</tbody>
</table>
Affected Configurations
This issue affects the ×1 soft IP implementation of the PCI Express MegaCore function or a ×4 MegaCore function is plugged into a ×1 slot.

Workaround
There is no workaround.

Resolution
This issue is fixed in Release 9.0 SP1.

You Cannot Use the MegaWizard Plug-In Manager to Edit the SERDES in the Hard IP Implementation of the PCI Express MegaCore Function
For the hard IP implementation of the PCI Express Compiler, you cannot edit the SERDES variant using the ALTGX MegaWizard™ Plug-In Manager.

Affected Configurations
This issue affects the hard IP implementation of the PCI Express Compiler in version 9.0 of the Quartus II software.

Workaround
You can launch the ALTGX MegaWizard Plug-In Manager interface from the command line using the command given in Example 14–1. Be sure that the Use Auxiliary Transmitter (ATX) PLL option on the PLL/Ports page is turned off.

Example 14–1. Command to Edit the SERDES Variant for
```
qmegawiz IP_MODE=PCIE_HIP_8   -
wiz_override="gxb_analog_power=auto,tx_analog_power=auto,elec_idle_infer_enable=false, tx_allow_polarity_inversion=false,rx_cdrctrl_enable=true,rateswitchbaseclock, hip_tx_clkout,tx_pipemargin,tx_pipedemph,rx_elecidleinversel,fixedclk,rateswitch, reconfig_dprio_mode=1,reconfig_clk,reconfig_fromgxb,reconfig_togxb,enable_0ppm=false, rx_use_double_data_mode=false,tx_use_double_data_mode=false,rx_channel_width=8, tx_channel_width=8,rx_dwidth_factor=1,tx_dwidth_factor=1,rx_dataout,tx_datain, tx_ctrlenable,rx_ctrldetect,rx_patterndetect,rx_syncstatus" OPTIONAL_FILES="NONE" intended_device_family="stratixiv" starting_channel_number=0 <var>_serdes.v
```

Solution Status
This issue is fixed in Release 9.0 SP1.

Gate-Level Simulation Fails for Hard IP Variations
Due to simulation model issues running a post-compilation gate-level simulation of the PCI Express hard IP MegaCore function variations fails, stating incorrectly that the link does not train.

Affected Configurations
This issue affects the hard IP implementation of PCI Express MegaCore functions in the 9.0 release.
**Workaround**

Use the IP Functional Simulation models for simulation.

**Solution Status**

This issue will be fixed in a future release.

---

**Incorrect Link Training for Stratix IV GX Gen2 ×8 Hard IP Implementation**

The current clock distribution architecture in the Stratix IV GX ES silicon SERDES block could yield excessive inter-quad clock skew which prevents the link from training to Gen2 ×8. The link may train to Gen2 ×4.

For more details on the inter-quad clock skew issue, refer to the “PCI Express Gen2 ×8 functional mode with hard IP using CMU PLL or ATX PLL” heading in the “×8 and ×N Clock Line Timing Issue for Transceivers” section in the *Stratix IV GX ES Errata Sheet*.

**Affected Configurations**

This issue affects the hard IP implementation of the PCI Express Compiler in Stratix IV GX ES devices.

**Workaround**

The following possible workarounds are available:

- Run your hardware system at the Gen1 rate.
- Configure your system as two Gen2 ×4 links.

**Solution Status**

This issue will be fixed in a future version of the hard IP implementation of the PCI Express MegaCore function.

---

**Guidelines for Passing the PCI Express Electrical Gold Test on the v2.0 Compliance Base Board (CBB)**

The PCI Express electrical gold test requires the CBB v2.0 to measure the eye diagram on the transmit side of the serial transceiver at Gen1 and Gen2 rates. To run this test when using the hard IP implementation of the PCI Express Compiler, the Link Training and Status State Machine (LTSSM) must enter several polling compliance states, including: Gen1, Gen2–3.5dB, and Gen2–6dB. Altera recommends using an external hardware apparatus, such as a push-button switch, to trigger these LTSSM state changes. The push-button switch drives the testin[5] signal of the PCI Express MegaCore function. For more information about this signal, refer to Appendix B. Test Port Interface Signals in the *PCI Express Compiler User Guide*.

**Affected Configurations**

This issue affects the hard IP implementation of the PCI Express Compiler when performing compliance testing.
**Workaround**
You can use a push-button switch to trigger the required LTSSM state changes.

**Solution Status**
The current suggested solution of using a push-button switch to trigger the required state changes was successful at the PCI Sig during Workshop 65. This information will be included in a future version of the *PCI Express Compiler User Guide*.

**Endpoints Using the Hard IP Implementation Incorrectly Handle CfgRd0**

The hard IP implementation of the PCI Express endpoint incorrectly handles Type0 Configuration Reads (CfgRd0) when the CfgRd0 TLP's Bus or Device Number does not match the endpoint's current Bus and Device Number. The endpoint issues an unsupported request due to the mismatch. Section 7.1.3 of the *PCI Express Base Specification 1.1 or 2.0* states that, “Devices must respond to all Type 0 Configuration Read Requests, regardless of the Device Number specified in the Request.”

**Affected Configurations**
This issue affects the hard IP implementation of the PCI Express endpoint in Stratix IV GX ES devices.

**Workaround**
Do not issue a CfgRd0 with mismatched bus/device numbers.

**Solution Status**
This issue will be fixed in a future version of the hard IP implementation of the PCI Express Compiler.

**Endpoints Using the Soft IP Implementation Incorrectly Handle CfgRd0**

The soft IP implementation of the PCI Express endpoint incorrectly handles Type0 Configuration Reads (CfgRd0) when the CfgRd0 TLP's Bus or Device Number does not match the endpoint's current Bus and Device Number. The endpoint issues an unsupported request due to the mismatch. Section 7.1.3 of the *PCI Express Base Specification 1.1 or 2.0* states that, “Devices must respond to all Type 0 Configuration Read Requests, regardless of the Device Number specified in the Request.”

**Affected Configurations**
This issue affects the ×1 and ×4 variants of the soft IP implementation of the PCI Express endpoint in the 8.1 release of the PCI Express Compiler.

**Workaround**
Do not issue a CfgRd0 with mismatched bus/device numbers.

**Solution Status**
This issue is fixed in version 9.0 of the soft IP implementation of the PCI Express Compiler.
The Hard IP Implementation of the PCI Express Compiler May Be Unable to Exit the Disable State at the Gen2 Rate

The hard IP implementation of the PCI Express Compiler may be unable to exit the disable state after entering the disable state at the Gen2 rate.

Affected Configurations
This issue affects the hard IP implementation of the PCI Express Compiler when operating at the Gen2 rate.

Workaround
You can avoid this issue using either of the following workarounds:

- Make sure that you enter the disable state at the Gen1 rate.
- Program your application to detect entry to the Link Training and Status State Machine (LTSSM) disable state and then assert the hard IP reset (assertion of crst, srst, and npor) forcing the LTSSM to transition to the detect state. In this case, note that the LTSSM goes to detect state and eventually to the polling compliance state where the Tx line is no longer in idle state. Altera uses this workaround for the design example generated by the PCI Express Compiler.

Solution Status
This issue will be documented in a future version of the PCI Express Compiler User Guide.

Timing Closure for Chaining DMA Design Example Gen1×8 in Stratix IV C3 and C4 Speed Grades

When compiling the PCI Express Gen1 ×8 chaining DMA design example for the C3 and C4 speed grades of the Stratix IV family, the design fails to meet timing requirements.

Affected Configurations
This issue affects the C3 and C4 speed grades of the Stratix IV device family.

Workaround
Add the constraints in Example 14–2 to your Quartus II Settings File (.qsf) if you are compiling the chaining DMA design example for 250 MHz operation in the slower speed grades of the Stratix IV family.
Example 14–2. Constraints for C3 and C4 Speed Grade for Stratix IV Family

```vhdl
set_global_assignment -name OPTIMIZATION_TECHNIQUE SPEED
set_global_assignment -name PHYSICAL_SYNTHESIS_COMBO_LOGIC ON
set_global_assignment -name PHYSICAL_SYNTHESIS_REGISTER_DUPLICATION ON
set_global_assignment -name PHYSICAL_SYNTHESIS_COMBO_LOGIC_FOR_AREA ON
set_instance_assignment -name DUPLICATE_ATOM srst_duplicate -from "top_example_chaining_pipelnb:core|srst" -to "top_example_chaining_pipelnb:core|top:epmap"
set_instance_assignment -name AUTO_GLOBAL_REGISTER_CONTROLS OFF -to "top_example_chaining_pipelnb:core|srst"
set_instance_assignment -name PRESERVE_REGISTER ON -to "top_example_chaining_pipelnb:core|altpcieer_example_app_chaining:app|srst"
set_instance_assignment -name PRESERVE_REGISTER ON -to "top_example_chaining_pipelnb:core|crst"
set_instance_assignment -name PRESERVE_REGISTER ON -to "top_example_chaining_pipelnb:core|srst"
```

Solution Status
This issue will be fixed in a future version of the Quartus II software.

The ×8 Soft IP Implementation of PCI Express MegaCore Function Only Supports 4 KByte Expansion ROM BAR

The ×8 soft IP implementation of the PCI Express MegaCore function only supports a 4 KByte expansion ROM BAR, however, the MegaWizard Plug-In Manager erroneously allows the selection of all BAR Size options.

Affected Configurations
This issue affects the ×8 soft IP implementation of the PCI Express Compiler in all versions of the Quartus II software.

Workaround
There are three possible workarounds for this issue:

- Restrict the Expansion BAR size to 4 KBytes.
- Change from a ×8 to a ×4 configuration.
- Change to the ×8 hard IP implementation of the PCI Express MegaCore function which is available in Stratix IV GX and Arria II GX devices.

Solution Status
This issue will be fixed in a future version of the PCI Express Compiler.
The Description of \texttt{cfg\_devcsr[31:0]} in the PCI Express Compiler User Guide is Incorrect

Table 5-17 of the \textit{PCI Express Compiler User Guide} incorrectly states that \texttt{cfg\_devcsr[31:16]} is the device control field and \texttt{cfg\_devcsr[15:0]} is the device status field. The opposite is true. \texttt{cfg\_devcsr[31:16]} is the device status field and \texttt{cfg\_devcsr[15:0]} is the device control field.

**Affected Configurations**
This issue affects versions 8.1 and 9.0 of the \textit{PCI Express Compiler User Guide}.

**Workaround**
No workaround is required.

**Solution Status**
This issue will be fixed in a future version of the \textit{PCI Express Compiler User Guide}.

Adding Two PCI Express Components to an SOPC Builder System May Cause a System Error

Adding two or more additional PCI Express components to an SOPC Builder system may cause a Java stack overflow error (\texttt{StackOverflowError}).

**Affected Configurations**
This issue may affect SOPC Builder systems to which you add two or more PCI Express components consecutively.

**Workaround**
If you encounter this error, save your SOPC Builder system and exit SOPC Builder. Restart SOPC builder and load the saved \texttt{.sopc} file. You can now edit all instances of the PCI Express module.

**Solution Status**
This issue will be fixed in a future version of the Quartus II software.

License File for Soft IP Implementation of the PCI Express Compiler Does Not Work

The license file for the soft IP version of the PCI Express Compiler in 8.1 does not work.

**Affected Configurations**
This issue affects soft IP implementations of the PCI Express MegaCore function in version 8.1 of the Quartus II software.

**Workaround**
The workaround is to download and install the Quartus II 8.1 software patch contained in the following \texttt{.zip} file:

Solution Status
This issue is fixed in version 9.0 of the Quartus II software.

EDA Netlist Writer Does Not Write Netlist for Hard IP Implementation of PCI Express
The Quartus II EDA Netlist Writer does not write a Stratix IV GX functional simulation netlist for the hard IP implementation of the PCI Express MegaCore function because a license file has not been specified. However, the hard IP implementation does not require a license.

Affected Configurations
This issue affects hard IP implementations of the PCI Express MegaCore function in version 8.1 of the Quartus II software.

Workaround
The workaround is to download and install Quartus II 8.1 software patch contained in the following .zip file:

Solution Status
This issue will be fixed in a future release of the Quartus II software.

Stratix IV Projects with Pin Assignments Specified Using the Pin Planner May Fail Quartus II Compilation
If you specify pin assignments using the Pin Planner for Stratix IV projects, Quartus II compilation fails.

Affected Configurations
This issue affects PCI Express MegaCore functions that target the Stratix IV family.

Workaround
Change the definition for the I/O standard for the transceivers from 1.2 V PCML to 1.4 V PCML.

Solution Status
This issue is fixed in version 9.0 of the Quartus II software.

Simulation Fails when Using ModelSim AE for Stratix II GX MegaCore Functions with the Avalon-ST or Descriptor/Data Interfaces
If you simulate PCI Express MegaCore functions that use the Avalon-ST or descriptor/data interface and target Stratix II GX devices using ModelSim® AE, you get a compilation error.

Affected Configurations
This issue affects PCI Express MegaCore functions written in Verilog HDL that use the Avalon-ST or descriptor/data interface and target a Stratix II GX device.
Workaround
In the `<variation_name>_examples/chaining_dma/testbench/sim_filelist` file, modify the line specifying `<variation_name>_serdes.v` to specify `<variation_name>_serdes.vo`.

Solution Status
This issue is fixed in version 9.0 of the Quartus II software.

The Chaining DMA Design Example May Issue DMA Write Requests that Violate the 4 KByte Boundary Rule in the VHDL Version

The VHDL version of the chaining DMA design example may issue DMA writes that violate the 4 KByte boundary. If a request crosses the 4 KByte boundary, the DMA data is thrown away. Because there is no data checking in the version 8.1 test driver, the simulation does not fail.

Affected Configurations
This issue affects the VHDL version of the chaining DMA design example for 8.1.

Workaround
You can modify the test driver, `altpcietb_bfm_driver_chaining.vhd`, so that the write DMA does not transfer data across 4 KByte addresses.

Solution Status
This issue is fixed in version 9.0 of the PCI Express Compiler design example.

Design Example in Hardware Might Require the RC Slave Module

The default configuration of the Altera-provided design example described in the Testbench chapter of the PCI Express Compiler User Guide does not instantiate the RC Slave module. The RC Slave module acknowledges message TLPs and zero-length memory read TLPs from the root complex. Typically, commercial BIOS’s issue message TLPs; therefore, if you do not instantiate the RC Slave module in this design example, your hardware system may stall indefinitely.

Affected Configurations
This issue affects designs that use the PCI Express Development Kit and are recompiling the hardware design example with the 7.2 or 8.0 version of the PCI Express Compiler.

Workaround
Enable the RC Slave module when connecting to a commercial PCI Express platform.

Solution Status
This issue is fixed in version 9.0 of the PCI Express Compiler.
Root Port BFM in Version 8.1 of the PCI Express Testbench is not Backwards Compatible

Testbenches for PCI Express MegaCore functions generated in version 8.0 or earlier of the Quartus II software fail in version 8.1 of the Quartus II software.

Affected Configurations

This issue affects existing PCI Express MegaCore functions generated using version 8.0 or earlier of the PCI Express Compiler if you have upgraded to Quartus II 8.1 and want to regenerate the testbench using the Quartus II 8.1 software.

Workaround

If your design targets the Stratix IV family, you must regenerate your PCI Express MegaCore function using version 8.1 of the PCI Express Compiler.

If your design targets other device families, a workaround is to modify the runtb.do file in the testbench directory. Edit all lines that contain stratixiv to point to version 8.0 of the Altera MegaCore IP Library.

Example 14–3 shows the original and modified version for VHDL.

```
Example 14–3. Modifications for runtb.do—VHDL

# This is the original line that uses the _ROOTDIR variable
vcom -work stratixiv_pcie_hip $env(QUARTUS_ROOTDIR)/eda/sim_lib/stratixiv_pcie_hip_components.vhd

# This edited version points to version 8.0 of the Altera IP library
vcom -work stratixiv_pcie_hip c:/altera/80/quartus/eda/sim_lib/stratixiv_pcie_hip_components.vhd
```

Example 14–4 shows the original and edited versions for Verilog HDL.

```
Example 14–4. Modifications for runtb.do—Verilog HDL

# This is the original line that uses the QUARTUS_ROOTDIR variable
vlog -work stratixiv_hssi $env(QUARTUS_ROOTDIR)/eda/sim_lib/stratixiv_hssi_atoms.v

# This edited version points to version 8.0 of the Altera IP Library
vlog -work stratixiv_hssi c:/altera/80/quartus/eda/sim_lib/stratixiv_hssi_atoms.v
```

Solution Status

This issue is the result of incompatibilities between the high-speed serial interface (HSSI) design for version 8.1 of the Quartus II software and earlier versions. These incompatibilities cannot be resolved.

Incorrect Connection of SOPC Builder Interrupt Sources to PCI Express Components

In SOPC Builder systems containing a PCI Express component which masters interrupt senders on the other side of an Avalon-MM pipeline bridge or clock-crossing bridge, interrupt sources are not correctly wired to the PCI express component.

Affected Configurations

This issue affects PCI Express Compiler instances used in SOPC Builder systems containing an Avalon-MM pipeline bridge or clock-crossing bridge.
**Workaround**
Ensure that there is not an Avalon-MM pipeline bridge or clock-crossing bridge master between the PCI Express Rx master port and its slaves which produce interrupts.

**Solution Status**
This issue will be fixed in a future version of the Quartus II software.

---

**PCI Express Avalon-MM Tx Interface Deadlocks on a Read Request**

When the Rx completion buffer is almost fully allocated, a new read might be sent even if there is not enough space in the buffer to store the read data. When this new read is sent, the read credit counter rolls over erroneously indicating that buffer space is available and the buffer overflows. Eventually, the Avalon Tx interface deadlocks on a read request because the wait request signal is asserted.

**Affected Versions**

This issue affects versions 8.0 of the PCI Express Compiler and earlier that use the SOPC Builder design flow.

**Workaround**

There is no workaround for this issue; however, it is fixed in version 8.1 of the PCI Express Compiler.

**Solution Status**

This issue is fixed in version 8.1 of the PCI Express Compiler.

---

**Unable to Compile the Example Design Successfully in Quartus II when using ECRC Forwarding**

For Stratix IV PCI Express variations that enable ECRC forwarding, compilation of the example design may fail because the included version of the CRC Compiler variation is not enabled for the Stratix IV device family.

**Affected Configurations**

This issue occurs in version 8.0 of the PCI Express Compiler if you do not have a license for the 8.0 CRC Compiler and you are creating a Stratix IV variant of the PCI Express MegaCore function that uses ECRC forwarding.

**Workaround**

You can complete the following these steps to edit the CRC Compiler variation created in your design example directory to update it to 8.0:

1. Open the Quartus II project that contains the design example.
2. Launch MegaWizard Plug-In Manager from the Tools menu.
3. Select *Edit an existing custom megafunction variation*.
4. Click Next.

5. Select `atpcierd_rx_ecrc_64.v` or `.vhd` or `atpcierd_rx_ecrc_128.v` if using Avalon-ST 128.

6. In the Megafonction name list, select CRC Compiler 8.0.

7. Click Next.

8. Click Next.

9. Click Finish.

10. Repeat steps 5–9 for `atpcierd_tx_ecrc_64.v` or `.vhd` or `atpcierd_tx_ecrc_128.v` if using Avalon-ST 128.

**Solution Status**

This is fixed in version 8.1 of the PCI Express Compiler.

### Chaining DMA Design Example Forwards Tx ECRC with Incorrect Alignment

The chaining DMA design example incorrectly aligns the Tx ECRC, appending the ECRC to the dword immediately following the header regardless of address alignment, when the TLP does not include a payload data. The alignment is incorrect in two cases:

- With four dword headers, non-qword aligned addressing, and no payload data
- With three dword header, qword aligned addressing, and no payload data

For packets with payload, the ECRC should be appended to the end as an extra dword of payload. For packets without payload, the ECRC field should follow address alignment as if it were a one dword payload.

**Affected Configurations**

This issue effects the chaining DMA design example, not variants of the PCI Express MegaCore function.

**Workaround**

The out-of-the-box simulation example does not cause a simulation failure. If you have modified the simulation to use four dword headers, then you must modify the chaining DMA example code to correct the alignment.

**Solution Status**

This issue is fixed in version 8.1 of the PCI Express Compiler.

### User Guide Incorrectly Documents the Number of Address Pages

Table 3-6 of the *PCI Express Compiler User Guide* incorrectly states the choices for the Number of address pages. The correct number of pages available is $2^n$ from 1–512.

**Affected Configurations**

This is a documentation error only.
**Workaround**

No workaround is required.

**Solution Status**

This issue is fixed in version 8.1 of the *PCI Express Compiler User Guide*.

**User Guide Incorrectly Documents rx_st_data and tx_st_data in 128-Bit Mode**

In 128-bit mode, the qwords in the timing diagrams are swapped. The correct order for Rx or Tx data[127:0] is {H3, H2, H1, H0}. The *PCI Express Compiler User Guide* shows data[127:0] as {H1, H0, H3, H2}. In addition, the rx_st_empty0 and tx_st_empty0 signals indicate that the TLP ends in the lower words of data. The corrected diagrams and text are given here.

*Figure 14–1* shows the mapping of 128-bit Avalon-ST Rx packets to PCI Express TLPs for TLPs with a three dword header and qword aligned addresses.

*Figure 14–2* shows the mapping of 128-bit Avalon-ST Rx packets to PCI Express TLPs for TLPs with a three dword header and non-qword aligned addresses.

---

**Figure 14–1. 128-Bit Avalon-ST rx_st_data0 Cycle Definition for 3-DWord Header TLPs with QWord Aligned Addresses**

- clk
- rx_st_valid
- rx_st_data[127:96]
- Header2
- Data 3
- rx_st_data[95:64]
- Header 1
- Data 2
- rx_st_data[63:32]
- Header 0
- Data 1
- rx_st_data[31:0]
- Data (n)
- rx_st_sop
- rx_st_eop
- rx_st_empty

**Figure 14–2. 128-Bit Avalon-ST tx_st_data0 Cycle Definition for 3-DWord Header TLPs with non-QWord Aligned Addresses**

- clk
- tx_st_valid
- tx_st_data[127:96]
- Data 0
- Header 2
- Data 4
- tx_st_data[95:64]
- Header 1
- Data 3
- tx_st_data[63:32]
- Header 0
- Data 2
- tx_st_data[31:0]
- Data (n)
- tx_st_sop
- tx_st_eop
- tx_st_empty
Figure 14–3 shows the mapping of 128-bit Avalon-ST Rx packets to PCI Express TLPs for a four dword header with non-qword aligned addresses. In this example, \texttt{rx\_st\_empty} is low because the data ends in the upper 64 bits of \texttt{rx\_st\_data}.

**Figure 14–3.** 128-Bit Avalon-ST \texttt{rx\_st} Cycle Definition for 4-Dword Header TLPs with non-QWord Aligned Addresses

![Diagram](image1)

Figure 14–4 shows the mapping of 128-bit Avalon-ST Rx packets to PCI Express TLPs for a four dword header with qword aligned addresses.

**Figure 14–4.** 128-Bit Avalon-ST \texttt{rx\_st} Cycle Definition for 4-Dword Header TLPs with QWord Aligned Addresses

![Diagram](image2)

Figure 14–5 shows the mapping of 128-bit Avalon-ST Tx packets to PCI Express TLPs for a three dword header with qword aligned addresses.

**Figure 14–5.** 128-Bit Avalon-ST \texttt{tx\_st\_data} Cycle Definition for 3-Dword Header TLPs with QWord Aligned Addresses

![Diagram](image3)
Figure 14–6 shows the mapping of 128-bit Avalon-ST Tx packets to PCI Express TLPs for a 3 dword header with non-qword aligned addresses.

Figure 14–6. 128-Bit Avalon-ST tx_st_data Cycle Definition for 3-DWord Header TLPs with non-QWord Aligned Addresses

Figure 14–7 shows the mapping of 128-bit Avalon-ST Tx packets to PCI Express TLPs for a four dword header TLP with non-qword aligned addresses. In this example, tx_st_empty is low because the data ends in the upper 64 bits of tx_st_data.

Figure 14–7. 128-Bit Avalon-ST tx_st_data Cycle Definition for 4-DWord Header TLPs with non-QWord Aligned Addresses

**Affected Configurations**

This is a documentation error only.

**Workaround**

No workaround is required.

**Solution Status**

This issue is fixed in version 8.1 of the *PCI Express Compiler User Guide*. 
Address Translation Update Can Corrupt Outstanding Reads for MegaCore Functions Created in SOPC Builder

When an Avalon-MM master sends a request larger than the PCI Express Maximum payload size to the Tx slave port, the MegaCore function converts this large request into multiple PCIe requests of smaller size, depending on address boundaries and size. For each smaller payload packet sent, the address translation table is accessed to generate the address field of the packet. This process takes a number of clock cycles, and during that time, if the translation table entry is altered, the subsequent smaller request packets have the wrong address.

For write requests, it is safe to change the entry associated with a DMA after the last data is accepted for write. For read requests, it is safe to change the table entry after the first data for a DMA is returned. You should rotate among multiple entries in the Avalon-MM to PCIe address translation table in order to support more than one outstanding read request.

Affected Configurations
This issue affects PCI Express applications created in SOPC Builder.

Workaround
You must use the address translation tables as described in this errata.

Solution Status
This issue will be documented in a future version of the PCI Express Compiler User Guide.

SOPC Builder does not Support Legacy Interrupts for PCI Express

PCI Express applications created in SOPC Builder that run on top of Windows XP do not support legacy interrupts. Windows XP does not support MSI; consequently, no interrupt mechanism is available for these applications.

Affected Configurations
This issue affects PCI Express applications created in SOPC Builder that run on top of Windows XP.

Workaround
Two possible workarounds are to change to Windows Vista which supports MSI interrupts or use the PCIe Avalon-ST interface which supports legacy interrupts.

Solution Status
This issue is fixed in PCI Express Compiler version 8.0 SP1. The SOPC Builder PCI Express component now uses either MSI or Legacy interrupts automatically based on the standard interrupt controls in the PCI Express configuration space registers. The Interrupt Disable bit, which is bit 10 of the Command register, can be used to disable legacy interrupts. The MSI enable bit, which is bit 0 of the Message Control register in the MSI capability, can be used to enable MSI interrupts. Only one type of interrupt can be enabled at a time.


<table>
<thead>
<tr>
<th>Signal</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>cpl_err[5:4]</td>
<td>I</td>
<td>Completion error. This signal reports completion errors to the configuration space.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ cpl_err[5]: Unsupported request error for non-posted TLP. Used in soft IP Avalon-ST interface and the hard IP implementation.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ cpl_err[4]: Unsupported request error for posted TLP. Used in soft IP Avalon-ST interface and the hard IP implementation.</td>
</tr>
</tbody>
</table>

Affected Configurations
This is a documentation error only.

Workaround
No workaround is required.

Solution Status
This error is fixed version 8.1 of the PCI Express Compiler User Guide.

The Source Synchronous Output Clock Is Improperly Constrained for an External PHY

For an external PHY, the source synchronous output clock is not constrained to be placed in an I/O buffer.

Affected Configurations
This issue affects all PHYs with an output PIPE clock.

Workaround
Add the following constraint to the Quartus II Settings File (.qsf) for your project:
set_instance_assignment -name FAST_OUTPUT_REGISTER ON -to pipe_txclk

Solution Status
This issue is fixed in version 8.0 SP1 of the Quartus II software.

Compiler Does Not Create a Block Symbol File

The PCI Express Compiler does not automatically create a Block Symbol File (.bsf) for the PCI Express MegaCore function.

Affected Configurations
This issue affects all PCI Express MegaCore function variations in 8.0.
Workaround
You can use the Quartus II Block Editor to manually create a .bsf for the variation. Alternatively, you can use the quartus_map API at the command line to create a symbol, by typing the following command:

```
quartus_map --generate_symbol=<variation_name>.<v|vhd> <quartus II project name>
```

Solution Status
This issue will be fixed in a future version of the PCI Express Compiler.

**MegaWizard Interface Displays Incorrect Values**

PCI Express MegaWizard Interface displays incorrect values for the Credit Display Table of BufferSetup Page when the hard IP Implementation is selected. The displayed Rx Buffer Space Allocation (per VC) table displays incorrect values for the hard IP implementation of the PCI Express MegaCore function. Table 14–6 lists the correct values. The Desired performance for received requests setting has no effect. The credit allocations for the hard IP implementation are set to the values indicated in Table 14–6.

**Table 14–6. Rx Buffer Space Allocation (per VC) Hard IP Implementation**

<table>
<thead>
<tr>
<th>Credit Type</th>
<th>Number of Credits</th>
<th>Space Used (in Bytes)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Without ECRC Forwarding</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Posted header credit</td>
<td>50</td>
<td>800</td>
</tr>
<tr>
<td>Posted data credit</td>
<td>360</td>
<td>5760</td>
</tr>
<tr>
<td>Non-posted header credit</td>
<td>54</td>
<td>864</td>
</tr>
<tr>
<td>Completion header credit</td>
<td>112</td>
<td>1792</td>
</tr>
<tr>
<td>Completion data credit</td>
<td>448</td>
<td>7168</td>
</tr>
<tr>
<td>Total header credits</td>
<td>216</td>
<td>—</td>
</tr>
<tr>
<td>Rx buffer size</td>
<td>—</td>
<td>16384</td>
</tr>
<tr>
<td><strong>With ECRC Forwarding</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Posted header credit</td>
<td>50</td>
<td>1200</td>
</tr>
<tr>
<td>Posted data credit</td>
<td>336</td>
<td>5375</td>
</tr>
<tr>
<td>Non-posted header credit</td>
<td>54</td>
<td>1296</td>
</tr>
<tr>
<td>Completion header credit</td>
<td>112</td>
<td>1792</td>
</tr>
<tr>
<td>Completion data credit</td>
<td>420</td>
<td>6720</td>
</tr>
<tr>
<td>Total header credits</td>
<td>216</td>
<td>—</td>
</tr>
<tr>
<td>Rx buffer size</td>
<td>—</td>
<td>16384</td>
</tr>
</tbody>
</table>

**Affected Configurations**

The Rx Buffer Space Allocation information is incorrect for the hard IP implementation of the PCI Express MegaCore function which is available in Stratix IV GX devices.
**Workaround**

Refer to Table 14–6 for the correct values for Rx buffer space allocation.

**Solution Status**

This issue is fixed in version 8.1 of the PCI Express Compiler.

---

**Serial Simulation Is Unsuccessful for PCI Express Variants Targeting Stratix GX with refclk at 156.25 MHz**

Serial simulation fails because the root port bus functional model (BFM) cannot decode the serial data coming from the device under test (DUT).

**Affected Configurations**

All PCI Express MegaCore variants using the Stratix GX PHY of any lane width with refclk at 156.25 MHz. This issue does not affect Stratix GX PHYs that use a refclk at 100 MHz or 125 MHz.

**Workaround**

There is no workaround.

**Solution Status**

This issue is fixed in 8.0 SP1 version of the PCI Express Compiler.
15. POS-PHY Level 2 and 3 Compiler

Revision History

Table 15–1 shows the revision history for the POS-PHY Level 2 and 3 Compiler.

For more information about the new features, refer to the POS-PHY Level 2 and 3 Compiler User Guide.

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.0</td>
<td>March 2009</td>
<td>Preliminary support for Arria II GX devices.</td>
</tr>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>Full support for Stratix III devices.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>Full support for Cyclone III devices&lt;br&gt;Preliminary support for Stratix IV devices</td>
</tr>
</tbody>
</table>

Errata

Table 15–2 shows the issues that affect the POS-PHY Level 2 and 3 Compiler v9.0, 8.1, and 8.0.

Not all issues affect all versions of the POS-PHY Level 2 and 3 Compiler.

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Oct 07</td>
<td>Missing Timescale Directive in NativeLink Verilog HDL Testbench</td>
<td>✓    ✓    ✓</td>
</tr>
<tr>
<td></td>
<td>Compilation Error in NativeLink VHDL Flow for NCSim</td>
<td>✓    ✓    ✓</td>
</tr>
<tr>
<td>01 Dec 06</td>
<td>IP Toolbench Incorrect Behavior</td>
<td>✓    ✓    ✓</td>
</tr>
<tr>
<td></td>
<td>Errors with Pin Planner Top-Level File</td>
<td>✓    ✓    ✓</td>
</tr>
</tbody>
</table>

Missing Timescale Directive in NativeLink Verilog HDL Testbench

There is a timescale directive missing from the top-level Verilog HDL testbench.

Affected Configurations

This issue affects the example testbench for NativeLink simulation using VCS MX.

Design Impact

The testbench does not compile.
Workaround

Edit the \sim_lib\testbench\verilog\auk_pac_mtx_ref_tb.v file and add the following directive:

`timescale 1ns / 1ns

Solution Status

This issue will be fixed in a future version of the POS-PHY Level 2 and 3 Compiler.

Compilation Error in NativeLink VHDL Flow for NCSim

There is a compilation error because of an error in the file declaration format.

Affected Configurations

This issue affects NCSim simulation for the VHDL flow.

Design Impact

NCSim simulation does not work for the VHDL flow.

Workaround

The incorrect declaration lines are not required and can be commented out:

- Edit the \sim_lib\testbench\vhdl\auk_pac_mtx_ref_tb.vhd file and comment out lines 128 and 461.
- Edit the \sim_lib\testbench\vhdl\auk_pac_mrx_ref_tb.vhd file and comment out lines 130 and 474.

Solution Status

This issue will be fixed in a future version of the POS-PHY Level 2 and 3 Compiler.

IP Toolbench Incorrect Behavior

In the IP Toolbench Parameterize window, after you click Finish, if you click Parameterize to review your settings, the options show incorrect behavior.

Affected Configurations

This issue affects all configurations.

Design Impact

There is no design impact.

Workaround

When you click Finish, ensure you close IP Toolbench (which cancels any changes) or click Generate. You can view the Parameterize window again by reopening IP Toolbench.

Solution Status

This issue will be fixed in a future version of the POS-PHY Level 2 and 3 Compiler.
Errors with Pin Planner Top-Level File

When you compile a Quartus II Pin Planner-generated top-level file you receive errors.

Affected Configurations
This issue affects all configurations.

Design Impact
The design does not compile.

Workaround
Do not use Pin Planner with the POS-PHY Level 2 and 3 Compiler.

Solution Status
This issue will be fixed in a future version of the POS-PHY Level 2 and 3 Compiler.
Revision History

Table 16–1 shows the revision history for the POS-PHY Level 4 MegaCore function.

For more information about the new features, refer to the POS-PHY Level 4 MegaCore Function User Guide.

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.0</td>
<td>March  2009</td>
<td>Preliminary support for Arria II GX devices.</td>
</tr>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>Full support for Stratix III devices.</td>
</tr>
</tbody>
</table>
| 8.0     | May 2008   | Full support for Cyclone III devices  
          | Preliminary support for Stratix IV devices            |

Errata

The following sections addresses known errata and documentation issues for the POS-PHY Level 4 MegaCore function. Errata are functional defects or errors, which may cause the POS-PHY Level 4 MegaCore function to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

Table 16–2 shows the issues that affect the POS-PHY Level 4 MegaCore function v9.0, 8.1, and 8.0.

Not all issues affect all versions of the POS-PHY Level MegaCore function.

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 Jun 09</td>
<td>Demonstration Testbench Fails</td>
<td>✓</td>
</tr>
<tr>
<td>15 Mar 09</td>
<td>Demonstration Testbench Fails</td>
<td>✓</td>
</tr>
<tr>
<td>01 Sep 08</td>
<td>Incorrect Description of DIP-4 Out of Service Indication in User Guide</td>
<td>✓ ✓ ✓</td>
</tr>
<tr>
<td>15 Aug 08</td>
<td>Valid Range of Full Threshold High is Incorrect</td>
<td>✓ ✓ ✓</td>
</tr>
<tr>
<td>15 May 08</td>
<td>Errors when Editing Transmitters v7.2 or Earlier in v8.0</td>
<td>✓ ✓ ✓</td>
</tr>
<tr>
<td></td>
<td>Transmitter Sends Extra Idles with Burst Limit Enable</td>
<td>✓ ✓ ✓</td>
</tr>
<tr>
<td></td>
<td>Missing Constraint</td>
<td>✓ ✓ ✓</td>
</tr>
<tr>
<td></td>
<td>Training Interval is Greater than Specified</td>
<td>✓ ✓ ✓</td>
</tr>
<tr>
<td></td>
<td>Signal stat_rd_dip4_oos Goes to X in Simulation</td>
<td>— — Fixed</td>
</tr>
</tbody>
</table>
Table 16–2. POS-PHY Level 4 MegaCore Function Errata

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 May 07</td>
<td>Irrelevant Signals: err_ry_msop* &amp; err_ry_meop*</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>Warning Message: Pin ‘err_rd_dpa’ Stuck at GND</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>IP Toolbench Error After Changing the Device Family</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>IP Toolbench Fails to Generate IP Functional Simulation Models for HardCopy Stratix Devices</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>IP Toolbench Generation Fails if the Generation Is Cancelled and Restarted</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td></td>
<td>8.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>8.0</td>
</tr>
</tbody>
</table>

**Generation Appears to Fail**

Some transmitter variants take a long time to generate and appear to have failed to generate.

**Affected Configurations**

Transmitters with embedded addressing, a high number of ports, an Atlantic interface width greater than the data path width, using the Lite Transmitter option, or a data path width of 32 bits, may take a long time to generate.

**Workaround**

Some generation may take over 20 minutes to generate.

**Design Impact**

There is no design impact.

**Solution Status**

This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

**Demonstration Testbench Fails**

The demonstration testbench may fail with the following error message:

Core Failed to Train

**Affected Configurations**

Receiver configurations with DPA enabled, in Arria II GX devices

**Workaround**

This issue has no workaround.

**Design Impact**

There is no design impact.

**Solution Status**

This issue will be fixed in a future version of the Quartus II software.
Incorrect Description of DIP-4 Out of Service Indication in User Guide

The following paragraph is incorrect in the DIP-4 Out of Service section in the POS-PHY Level 4 MegaCore Function User Guide:

If the receiver is in service (the `stat_rd_dip4_oos` signal is low) and one or more DIP-4 errors are detected (up to 8 in 128-bit mode) in the current `rdint_clk` cycle, the bad counter is incremented. If the bad counter reaches the `bad_level` threshold, the receiver goes out of service by asserting the `stat_rd_dip4_oos` signal. If all of the DIP-4s received in the current cycle are good, the bad counter is cleared. If no control words are received, nothing happens.

The following paragraph is correct:

If the receiver is in service (the `stat_rd_dip4_oos` signal is low) and one or more DIP-4 errors are detected (up to 8 in 128-bit mode) in the current `rdint_clk` cycle, the bad counter is incremented. If the bad counter reaches the `bad_level` threshold, the receiver goes out of service by asserting the `stat_rd_dip4_oos` signal. If any of the DIP-4s received in the current cycle are good, the bad counter is cleared. If no control words are received, nothing happens.

In particular, the following sentence has the incorrect “all” replaced by the correct “any”:

If any of the DIP-4s received in the current cycle are good, the bad counter is cleared.

In addition, the following paragraph in the Receiver Options section is incorrect in a similar way:

If the `stat_rd_dip4_oos` signal is low, and any of the DIP-4s in the control words received in the current clock cycle (up to 8 in 128-bit mode) are errored, the bad counter is incremented by 1; otherwise it is reset to 0. If the bad counter reaches the `bad_level` threshold, the `stat_rd_dip4_oos` flag is asserted. A `bad_level` of 0 is invalid.

The following paragraph is correct:

If the `stat_rd_dip4_oos` signal is low, and all of the DIP-4s in the control words received in the current clock cycle (up to 8 in 128-bit mode) are errored, the bad counter is incremented by 1; otherwise it is reset to 0. If the bad counter reaches the `bad_level` threshold, the `stat_rd_dip4_oos` flag is asserted. A `bad_level` of 0 is invalid.

Figure 16–1 shows an example of the DIP-4 counter, where the receiver is in service state and bad threshold is 3.
**Figure 16–1. DIP-4 Counter  *(Note 1)*

![Diagram of DIP-4 Counter]

**Note to Figure 16–1:**
(1) Receiving a good and a bad DIP-4 in the same parallel cycle resets the counter (does not increment it), so that OOS does not trigger.

### Affected Configurations
This issue affects all receiver configurations.

### Design Impact
The core may need to receive more control word DIP-4 errors than the **DIP-4 Bad Threshold** parameter set in the wizard for `stat_rd_dip4_oos` to go high.

### Solution Status
This issue will be fixed in a future version of the **POS-PHY Level 4 MegaCore Function User Guide**.

### Valid Range of Full Threshold High is Incorrect
The valid range of the full threshold high (FTH) is dependent on many parameters such as the width of the internal bus. When changing the width of the bus, the wizard may allow the FTH out of the acceptable range and so you end up with an incorrect or non-existent choice for the FTH.

### Affected Configurations
This issue affects transmitters.

### Design Impact
There is no design impact.
Workaround
To work around the issue, if you change the bus width, for example the Atlantic data width, ensure you modify the FTH value on the Protocol Parameters tab of the wizard.

Solution Status
The incorrect paragraphs will be fixed in a future version of the POS-PHY Level 4 MegaCore Function User Guide.

Errors when Editing Transmitters v7.2 or Earlier in v8.0
If you edit a v7.2 or earlier 64 or 128-bit transmitter MegaCore variation in the v8.0 MegaWizard Plug-In, the PLL input frequency is set to 1 MHz, which is incorrect.

Affected Configurations
This issue affects 64- and 128-bit transmitters.

Design Impact
There is no design impact.

Workaround
To work around the issue, follow these steps:
1. Click in the LVDS Data Rate dialog box.
2. Press Enter.
   The PLL input frequency parameter resets to the correct value—data rate divided by deserialization factor.

Solution Status
This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

Transmitter Sends Extra Idles with Burst Limit Enable
The POS-PHY Level 4 MegaCore function transmitter sends up to four control words between two bursts when you turn on Burst Limit Enable.

Affected Configurations
This issue affects transmitters with a 32-bit data-path width when you turn on Burst Limit Enable.

Design Impact
There design bandwidth is decreased.

Workaround
In the <variation name>tx_core.v file, change the TXLITE parameter from 0 to 1.
   parameter TXLITE = 1;
**Solution Status**

This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

**Missing Constraint**

In designs targeting Stratix III and Stratix IV devices, the `derive_clock_uncertainty` Synopsis design constraint (SDC) for TimeQuest is missing.

**Affected Configurations**

This issue affects all Stratix III and Stratix IV designs.

**Design Impact**

There is no design impact.

**Workaround**

Add the `derive_clock_uncertainty` SDC for Stratix III and Stratix IV device designs.

**Solution Status**

This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

**Training Interval is Greater than Specified**

In corner cases, for example with datapath is 256 and a high number of ports and low burst length (`BURSTLEN`), the maximum training interval (`MaxT`) is greater than you specify.

**Affected Configurations**

This issue affects all designs.

**Design Impact**

There is no design impact.

**Workaround**

Add (or substract) another `BURSTLEN` to calculation, so $\text{MaxT} = \text{SET.MaxT} + 2 \times \text{BURSTLEN}$.

**Solution Status**

This issue will never be fixed.

**Signal stat_rd_dip4_oos Goes to X in Simulation**

Some signals go to X (for example, `stat_rd_dip4_oos`) during simulation.
**Affected Configurations**

Receiver configurations with DPA enabled, in the following device families:

- Stratix II devices
- HardCopy II devices
- Stratix III devices
- Stratix IV devices
- Stratix II GX devices
- Arria GX devices

**Workaround**

After you generate the functional simulation model, manually edit the model (*.vo or *.vho) to add a new parameter to the altlvds megafonction instantiation. To edit a Verilog HDL example, follow these steps:

1. Search for the altlvds_rx instantiation:

   ```
   altlvds_rx <instantiation name>
   ```

   Add the following parameter after the altlvds_rx //defparam list:

   ```
   <instantiation name>. x_on_bitslip = "OFF",
   ```

**Design Impact**

There is no design impact. However, the demonstration testbench simulation fails, as some signals go to X (for example, stat_rd_dip4_oos).

**Solution Status**

This issue is fixed in the Quartus II software version 8.0.

**Irrelevant Signals: err_ry_msop* & err_ry_meop**

After generation, the MegaCore function may include the following irrelevant output signals, which you can safely ignore:

- err_ry_msop*
- err_ry_meop*

**Affected Configurations**

This issue affects all designs.

**Design Impact**

There is no design impact.

**Workaround**

This issue has no workaround.
Solution Status
This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

Warning Message: Pin “err_rd_dpa” Stuck at GND
During compilation, the Quartus II software issues the following warning, which you can safely ignore:
Pin “err_rd_dpa” Stuck at GND

Affected Configurations
This issue affects all non-Stratix GX receivers with dynamic phase alignment (DPA) enabled.

Design Impact
There is no design impact.

Workaround
This issue has no workaround.

Solution Status
This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

The Calendar Length Value Cannot Equal 256
If the transmitter’s status interpretation mode is set to pessimistic, the programmable calendar length support parameter must be less than the maximum number of ports (< 256), unless the asymmetric port support parameter is enabled.

Affected Configurations
This issue affects all transmitter variations of the MegaCore function that use the pessimistic mode for status interpretation, and that do not have the asymmetric port support parameter enabled.

Design Impact
The status first-in first-out (FIFO) buffer may lock up. The scheduler in individual buffers variations of the MegaCore function may also lock up.

Workaround
If you turn on the programmable calendar length support in your variation, make sure that you set the calendar length value—via a pin or the Avalon Memory-Mapped (Avalon-MM) register—to less than the maximum calendar length (that is, 256); unless asymmetric port support is enabled, in which case you select the maximum calendar length in IP Toolbench.
Solution Status
This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

IP Toolbench Error After Changing the Device Family
If you change the device family when editing an existing custom megafuction variation (POS-PHY Level 4 MegaCore function variation) without first changing the device family in the Quartus II project, an error may occur when generating the MegaCore function. This results in a MegaCore function generation error message. This issue also applies when creating a new custom megafuction variation, if you use a different device family to that specified in the Quartus II project.

Affected Configurations
This issue can affect all configurations.

Design Impact
You may not be able to generate a MegaCore function.

Workaround
Before using the MegaWizard Plug-In Manager to create or edit a POS-PHY Level 4 custom megafuction variation, make sure that a Quartus II project exists and that the required device family is set in the project. To set the device family, in the Quartus II software, on the Assignments menu click **Device**.

When using the MegaWizard Plug-In Manager to create or edit the megafuction variation, set the device family to be the same as the device family set in the Quartus II project. You can set the device family in the **Basic Parameters** tab when parameterizing the MegaCore function.

Solution Status
This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

IP Toolbench Fails to Generate IP Functional Simulation Models for HardCopy Stratix Devices
If you select **HardCopy Stratix** in the MegaWizard Plug-In Manager and you turn on **Generate Simulation Model** and generate a MegaCore function variation, IP Toolbench fails with an error.

Affected Configurations
This issue affects all configurations.

Design Impact
You cannot generate an IP functional simulation model.

Workaround
Select the Stratix family in the MegaWizard Plug-In Manager.
Solution Status
This issue will never be fixed.

IP Toolbench Generation Fails if the Generation Is Cancelled and Restarted

By clicking the IP Toolbench Generate button, you start generating a POS-PHY Level 4 MegaCore function variation. If, during generation, you click the Cancel button (Generation window) and click the IP Toolbench Generate button again to restart the generation, IP Toolbench fails and produces the following error message:

Figure 16–2. IP Toolbench Generation Error Message

Affected Configurations
This issue affects all variations of the MegaCore function.

Design Impact
IP Toolbench does not generate any files.

Workaround
To cancel a generation and avoid this error, follow these steps:
1. Click the Cancel button in the Generation window.
2. Close IP Toolbench by clicking the × in the upper right corner.
3. Relaunch IP Toolbench from the MegaWizard Plug-In Manager (Tools menu).

Refer to the Getting Started chapter of the POS-PHY Level 4 MegaCore Function User Guide for instructions on using IP Toolbench.

Solution Status
This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.
17. RapidIO

Revision History

Table 17–1 shows the revision history for the RapidIO MegaCore function.

For more information about the new features, refer to the RapidIO MegaCore Function User Guide.

Table 17–1. RapidIO MegaCore Function Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.0 SP2</td>
<td>July 2009</td>
<td>Maintenance release</td>
</tr>
<tr>
<td>9.0 SP1</td>
<td>May 2009</td>
<td>Preliminary support for HardCopy III and HardCopy IV E devices.</td>
</tr>
<tr>
<td>9.0</td>
<td>March 2009</td>
<td>• Preliminary support for Arria II GX devices</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Support for outgoing multicast-event symbol generation</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Support for 16-bit device ID</td>
</tr>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>• Full support for Stratix III devices</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Support for incoming multicast transactions</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Support to enable or disable destination ID checking</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Support to set transceiver starting channel number</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Requirement to configure a dynamic reconfiguration block with any Stratix IV transceivers, to enable offset cancellation</td>
</tr>
<tr>
<td>8.0 SP1</td>
<td>July 2008</td>
<td>Maintenance release</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>• Support for 1× mode 3.125 GBAud variations in Arria GX devices</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Preliminary support for Stratix IV devices</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Support to set reference clock frequency for Stratix II GX and Stratix IV GX internal transceivers</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Support to set VCCH for Stratix II GX internal transceivers</td>
</tr>
</tbody>
</table>

Errata

Table 17–2 shows the issues that affect the RapidIO MegaCore function v9.0 SP2, v9.0 SP1, v9.0, v8.1, v8.0 SP1, and v8.0.

Not all issues affect all versions of the RapidIO MegaCore function. Altera recommends upgrading to the latest available version of the MegaCore IP Library.

For SOPC Builder errata, which might affect the RapidIO MegaCore function and other SOPC Builder components, refer to the Quartus II Software Release Notes.
**Table 17–2. RapidIO MegaCore Function Errata (Part 1 of 2)**

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>01 Jul 09</strong></td>
<td>Error Response Packet Can Be Sent Twice if the io_m_rd_readerror Signal is Asserted</td>
<td>✓ ✓ ✓ ✓ ✓ ✓</td>
</tr>
<tr>
<td></td>
<td>Stratix III Device Support Level is Reported as Preliminary</td>
<td>Fixed</td>
</tr>
<tr>
<td><strong>15 May 09</strong></td>
<td>Response Packet is Sent for Request Packet with Reserved Transaction Type</td>
<td>✓ ✓ ✓ ✓ ✓ ✓</td>
</tr>
<tr>
<td></td>
<td>User Guide Description of Direction of io_s_rd_read Signal is Incorrect</td>
<td>✓ ✓ ✓ ✓ ✓ ✓</td>
</tr>
<tr>
<td></td>
<td>SOPC Builder Testbench May Fail on 1× Stratix GX Variations at 1.25 Gbaud</td>
<td>✓ ✓ — — — —</td>
</tr>
<tr>
<td></td>
<td>Transport Layer Can Drop Outgoing Packets if Physical Layer Transmit Buffer Fills</td>
<td>— Fixed ✓ ✓ ✓ ✓</td>
</tr>
<tr>
<td></td>
<td>Testbench Fails on Some Stratix GX Variations</td>
<td>— Fixed ✓ ✓ ✓ ✓</td>
</tr>
<tr>
<td></td>
<td>Some Variations With Reference Clock Frequency 390.625 MHz do Not Meet Timing</td>
<td>— Fixed ✓ ✓ ✓ ✓</td>
</tr>
<tr>
<td><strong>15 Apr 09</strong></td>
<td>The packet_transmitted Output Signal is Not Reliable — Cancelled</td>
<td>— — — — — —</td>
</tr>
<tr>
<td><strong>15 Mar 09</strong></td>
<td>Migration of Existing RapidIO MegaCore Function May Generate Warning Message</td>
<td>✓ ✓ ✓ ✓ ✓ ✓</td>
</tr>
<tr>
<td></td>
<td>SourceID Can Be Incorrectly Set to Zero in NWRITE_R Response Packets</td>
<td>— — Fixed ✓ ✓ — —</td>
</tr>
<tr>
<td></td>
<td>A Cancelled Packet Can Be Processed As a Normal Packet</td>
<td>— — Fixed ✓ ✓ ✓ ✓</td>
</tr>
<tr>
<td></td>
<td>Asserting io_m_wr_waitrequest During a Burst Transfer When io_m_wr_write is Not Asserted Can Cause Deadlock</td>
<td>— — Fixed ✓ ✓ ✓ ✓</td>
</tr>
<tr>
<td></td>
<td>Four Back-to-Back Short Incoming Packets Can Cause Miscalculation of the Following Packet Sizes</td>
<td>— — Fixed ✓ ✓ ✓ ✓</td>
</tr>
<tr>
<td></td>
<td>An Errored Incoming Packet Can Cause Miscalculation of the Following Packet Sizes</td>
<td>— — Fixed ✓ ✓ ✓ ✓</td>
</tr>
<tr>
<td></td>
<td>Timeout Logic Can Incorrectly Extend Doorbell Transaction Timeout Period</td>
<td>— — Fixed ✓ ✓ ✓ ✓</td>
</tr>
<tr>
<td></td>
<td>Doorbell Transaction Can Be Transmitted With Invalid Transaction ID</td>
<td>— — Fixed ✓ ✓ ✓ ✓</td>
</tr>
<tr>
<td></td>
<td>User Guide Description of Default Value of EF_ID Field in PHEAD0 Register is Incorrect</td>
<td>— — Fixed ✓ ✓ ✓ ✓</td>
</tr>
<tr>
<td></td>
<td>SOPC Builder Systems May Have Incorrectly Clocked Reset or Incorrect Calibration Clock Driver</td>
<td>— — Fixed ✓ ✓ ✓ ✓</td>
</tr>
</tbody>
</table>
Error Response Packet Can Be Sent Twice if the io_m_rd_readerror Signal is Asserted

If the `io_m_rd_readerror` signal is asserted, an error response packet can be sent twice.

Affected configurations

All RapidIO variations that implement an Input/Output Avalon-MM master Logical layer module.

Design impact

If a read response with ERROR status is transmitted twice, the link partner receives it twice. In that case, the link partner detects an unexpected error response.
Workaround
To avoid this issue, perform one of the following workarounds:

■ Do not assert the io_m_rd_readerror signal.
■ Ensure that reception of an unexpected response packet by the link partner has only benign effects.

Solution Status
This issue will be fixed in a future version of the RapidIO MegaCore function.

Stratix III Device Support Level is Reported as Preliminary
The RapidIO MegaCore function v9.0 includes full support for Stratix III devices. However, when you target a design with a RapidIO MegaCore function v9.0 to a Stratix III device in the Quartus II software v9.0, an error message indicates support is preliminary rather than full.

Affected Configurations
All RapidIO variations targeted to a Stratix III device.

Design Impact
None.

Workaround
Ignore the warning message about the support level.

Solution Status
This issue is fixed in version 9.0 SP2 of the RapidIO MegaCore function.

Response Packet is Sent for Request Packet with Reserved Transaction Type
If the RapidIO MegaCore function receives a Type 2 (request class) Input/Output request packet with a reserved transaction type, the Input/Output Avalon-MM master Logical layer module generates an ERROR response packet.

Affected Configurations
All RapidIO variations that implement an Input/Output Avalon-MM master Logical layer module.

Design Impact
The link partner receives a potentially unexpected response packet, which may cause it to incorrectly detect an error in the RapidIO MegaCore function.

Workaround
Avoid sending Type 2 request packets with a reserved transaction type to the RapidIO MegaCore function.
Solution Status
This issue will be fixed in a future version of the RapidIO MegaCore function.

User Guide Description of Direction of io_s_rd_read Signal is Incorrect

The Input/Output Avalon-MM slave Logical layer signal io_s_rd_read is listed incorrectly in the RapidIO MegaCore Function User Guide as an output signal. This read enable signal is an input signal to the Input/Output Avalon-MM slave Logical layer module.

Affected Configurations
All RapidIO variations that implement an Input/Output Avalon-MM master Logical layer module.

Design Impact
Relying on the io_s_rd_read read enable signal of an Input/Output Avalon-MM slave Logical layer module to be driven by that module leads to incorrect results.

Workaround
Expect this signal to be an input signal to the Input/Output Avalon-MM slave Logical layer module.

Solution Status
This issue will be fixed in a future version of the RapidIO MegaCore Function User Guide.

SOPC Builder Testbench May Fail on 1× Stratix GX Variations at 1.25 GBaud

For some 1× RapidIO variations at 1.25 GBaud that use the built-in high-speed transceivers on Stratix GX devices, simulation of the SOPC Builder customer testbench fails, because the testbench dictates a clock frequency that does not match the transceiver clock setting. The problem exists only for the testbench generated for a RapidIO variation with Physical, Transport, and Logical layers.

Affected Configurations
Some 1× RapidIO variations that use the built-in high-speed transceivers on Stratix GX devices.

Design Impact
SOPC Builder system testbench simulation fails for the affected configurations.

Workaround
In the Quartus II project directory, open the file <RapidIO variation name>_hookup.iv in a text editor, and locate the following code:

```
forever begin
    # <wait time number>;
    clk <= ~clk;
end
```

Replace <wait time number> in this code with the value 8.
Solution Status
This issue will be fixed in a future version of the RapidIO MegaCore function.

Transport Layer Can Drop Outgoing Packets if Physical Layer Transmit Buffer Fills
If packets are transferred back-to-back from a Logical layer module to the Transport layer—the end-of-packet word of one packet is followed immediately by the start-of-packet word of another packet—and the value of the Physical layer transmit buffer output signal \( \text{atxwlevel} \) becomes 10 in the same cycle in which the end-of-packet word is transferred from the Logical layer to the Transport layer, the following packet is dropped silently.

Affected Configurations
All RapidIO variations that implement a Logical layer module.

Design Impact
Outgoing packets might be lost. The problem has been observed only with packets whose data payload is approximately 80 bytes.

Workaround
To avoid the problem, perform one of the following workarounds:

- Ensure that the Physical layer transmit buffer \( \text{atxwlevel} \) signal value remains greater than 10.
- Ensure a gap of at least one clock cycle between packets from the same Logical layer module to the Transport layer.

Solution Status
This issue is fixed in version 9.0 SP1 of the RapidIO MegaCore function.

Testbench Fails on Some Stratix GX Variations
For some variations that use the built-in high-speed transceivers on Stratix GX devices, simulation of either customer testbench fails, because the testbench dictates a clock frequency that does not match the transceiver clock setting. The problem exists for both the Physical-layer-only testbench and the testbench generated for a RapidIO variation with Physical, Transport, and Logical layers.

Affected Configurations
The following RapidIO variations that use the built-in high-speed transceivers on Stratix GX devices are affected:

- \( \times 1 \) variation at 3.125 GBaud
- \( \times 4 \) variation at 1.25 GBaud
- \( \times 4 \) variation at 3.125 GBaud

Design Impact
Testbench simulation fails for the affected configurations. The problem exists for both the Physical-layer-only testbench and the SOPC Builder system testbench.
Workaround
In the Quartus II project directory, open the file <RapidIO variation name>_hookup.iv in a text editor, and locate the following code:

```
foret begin
   # <wait time number>
   clk <= ~clk;
end
```

Replace <wait time number> in this code according to Table 17–3:

Table 17–3. Correct <wait time number> Values

<table>
<thead>
<tr>
<th>Number of Channels</th>
<th>Data Rate (GBaud)</th>
<th>Correct &lt;wait time number&gt; Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>3.125</td>
<td>3.2</td>
</tr>
<tr>
<td>4</td>
<td>1.25</td>
<td>8</td>
</tr>
<tr>
<td>4</td>
<td>3.125</td>
<td>3.2</td>
</tr>
</tbody>
</table>

Solution Status
This issue is fixed in version 9.0 SP1 of the RapidIO MegaCore function.

Some Variations With Reference Clock Frequency 390.625 MHz do Not Meet Timing

Some RapidIO MegaCore function variations do not meet timing requirements initially.

Affected Configurations
4× RapidIO variations with reference clock frequency 390.625 MHz that use high-speed transceivers and are targeted to Arria II GX and Stratix IV devices.

Design Impact
Because these variations do not meet timing requirements, a design that contains one of these variations cannot compile successfully.

Workaround
To avoid this issue, perform the following workaround to regenerate the high-speed transceiver:

1. In the Quartus II software, on the Tools menu, click MegaWizard Plug-In Manager.
2. In the MegaWizard Plug-In Manager, turn on Edit an existing custom megafonction variation.
3. Click Next.
4. In the File name field, select the file <RapidIO_instance_name>_riophy_gxb.v.
5. Click Next.
6. On the Parameter Settings tabs, click Next repeatedly until you reach the RX Analog tab.
7. To regenerate the RapidIO MegaCore function high-speed transceiver with the issue resolved, click Finish.

You can now compile your design without encountering this problem in your RapidIO MegaCore variation.

Solution Status
This issue is fixed in version 9.0 SP1 of the RapidIO MegaCore function.

The packet_transmitted Output Signal is Not Reliable — Cancelled

This erratum is incorrect: the problem does not exist and has never existed in the RapidIO MegaCore function.

The packet_transmitted output signal might be pulsed twice for each transmitted packet in any 4x RapidIO variation.

Affected Configurations
No RapidIO variations are affected.

Design Impact
None. The packet_transmitted signal can be used to determine the exact count of transmitted packets.

Workaround
None needed.

Solution Status
This issue has been determined to be a non-issue. The problem does not exist and has never existed in the RapidIO MegaCore function.

Migration of Existing RapidIO MegaCore Function May Generate Warning Message

When you migrate your design between device families, you must change the high-speed transceiver types of your RapidIO MegaCore functions to match the new device family. Doing so generates a warning message and does not modify the intended device for the RapidIO MegaCore function as a whole. Modifying the device for the MegaCore function requires that you edit an HDL file.

Affected Configurations
All RapidIO variations.

Design Impact
Changing the high-speed transceiver type of your RapidIO MegaCore function without implementing the workaround causes compilation to fail, because the RapidIO MegaCore function target device and its high-speed transceiver target device are different.
Workaround

To modify the target device for your RapidIO MegaCore function and for its high-speed transceiver, perform the following workaround:

1. In a text editor, open the file `<RapidIO_instance_name>.v` or `<RapidIO_instance_name>.vhd` for editing.
2. Search for the following two lines in the file:
   ```
   //Retrieval info:<PRIVATE name = "intended_family" value ="<family>"
type="STRING" enable="1" />
   
   and
   
   //Retrieval info:<PRIVATE name = "phy_selection" value ="<PHY>"
type="STRING" enable="1" />
   ```
3. In these two lines of code, substitute the new target device family value for `<family>` and `<PHY>` according to Table 17–4.
4. Save and close the file.
5. In the Quartus II software, on the Tools menu, click MegaWizard Plug-In Manager.
6. In the MegaWizard Plug-In Manager, turn on Edit an existing custom megafuction variation.
7. Click Next.
8. In the File name field, select the file `<RapidIO_instance_name>.v`.
9. Click Next.
10. To regenerate the RapidIO MegaCore function and its high-speed transceiver for the new target device family, click Finish.

Solution Status

This issue will be fixed in a future version of the RapidIO MegaCore function.

SourceID Can Be Incorrectly Set to Zero in NWRITE_R Response Packets

The SourceID field in an NWRITE_R response packet might be set to zero instead of being set to the destination ID received in the request packet.

Affected Configurations

All RapidIO variations that implement an Input/Output Avalon-MM master Logical layer module.
Design Impact
If a link partner sends an NWRITE_R request and detects an erroneous SourceID in the response on the link, it might not recognize the response to the request.

Workaround
To avoid this issue, perform one of the following workarounds:
- Generate NWRITE or SWRITE requests instead of NWRITE_R requests.
- Precede each sequence of NWRITE_R requests to the same destination ID with an NREAD request to that destination ID.
- Program the link partner to accept response packets regardless of their SourceID.

Solution Status
This issue is fixed in version 9.0 of the RapidIO MegaCore function.

A Cancelled Packet Can Be Processed As a Normal Packet
If a packet received over the RapidIO link contains a stomp control symbol, and this packet is immediately followed by a start-of-packet control symbol, the first packet might be processed as if it were not cancelled.

Affected Configurations
All 4x RapidIO variations.

Design Impact
The final two bytes of the cancelled packet are treated as the CRC of the cancelled packet. In most cases, a CRC error is detected, the packet is dropped, and the error recovery process is initiated. In the rare case that the final two bytes form a valid CRC for the packet, the partial packet is processed as if it were not cancelled.

Workaround
None known.

Solution Status
This issue is fixed in version 9.0 of the RapidIO MegaCore function.

Asserting io_m_wr_waitrequest During a Burst Transfer When io_m_wr_write is Not Asserted Can Cause Deadlock
If a slave driven by an Avalon-MM I/O master asserts the io_m_wr_waitrequest signal during a burst transfer when io_m_wr_write is not asserted, the Avalon-MM I/O master module will not assert the io_m_wr_write signal until io_m_wr_waitrequest is deasserted. In this case, the Avalon-MM interface deadlocks.

Affected Configurations
All RapidIO variations that implement an Avalon-MM I/O master write interface.
Design Impact
If the slave waits for the assertion of `io_m_wr_write` before deasserting the `io_m_wr_waitrequest` signal, and the master waits for the deassertion of `io_m_wr_waitrequest` before asserting `io_m_wr_write`, the module deadlocks.

Workaround
Do not assert `io_m_wr_waitrequest` indefinitely, or avoid asserting `io_m_wr_waitrequest` after a burst transfer has started.

Solution Status
This issue is fixed in version 9.0 of the RapidIO MegaCore function.

Four Back-to-Back Short Incoming Packets Can Cause Miscalculation of the Following Packet Sizes

If four short packets are transferred back-to-back from the Physical layer to the Transport layer, the size of subsequent packets can be miscalculated. This problem occurs only following a complex sequence of events followed by the receipt of four short back-to-back packets on the RapidIO link, and is therefore unlikely to occur.

Affected Configurations
All 4× RapidIO variations that implement a Transport layer.

Design Impact
If this problem occurs, the resulting erroneous packet sizes can cause Input/Output modules to reject valid packets, or to issue Avalon-MM transactions with incorrect burstcounts, among other possible impacts.

Workaround
To reduce the chance of encountering this issue, you can modify your application to reduce the number of back-to-back packet transfers from the Physical layer to the Transport layer, by preventing received packets from accumulating in the Physical layer Receive buffer.

For example, either of the following two modifications helps to avoid the accumulation of packets in the Physical layer Receive buffer:

- Run the system clock at the nominal clock frequency or higher.
- To decrease the back pressure that occurs when the Avalon-MM wait-request signals are asserted, do not assert these signals.

Solution Status
This issue is fixed in version 9.0 of the RapidIO MegaCore function.
An Errored Incoming Packet Can Cause Miscalculation of the Following Packet Sizes

If a packet marked as errored is transferred from the Physical layer to the Transport layer immediately following a valid packet, with no gap between the end of the first packet and the start of the second packet, the size of subsequent packets can be miscalculated.

Affected Configurations

All RapidIO variations that implement a Transport layer.

Design Impact

Erroneous packet sizes can cause Input/Output modules to reject valid packets, or to issue Avalon-MM transactions with incorrect burstcounts, among other possible impacts.

Workaround

You can modify your application to reduce the chance of encountering this issue, and you can perform a workaround that avoids the issue.

To reduce the chance of encountering this issue, you can modify your application in one or both of the following ways:

- Reduce the bit-error rate to reduce the number of errored packets received by the Transport layer.
- Reduce the number of back-to-back packet transfers from the Physical layer to the Transport layer, by preventing received packets from accumulating in the Physical layer Receive buffer. Either of the following two modifications helps to avoid the accumulation of packets in the Physical layer Receive buffer:
  - Run the system clock at the nominal clock frequency or higher.
  - To decrease the back pressure that occurs when the Avalon-MM wait-request signals are asserted, do not assert these signals.

To avoid the issue, perform the following workaround:

1. Use the MegaWizard interface to specify the parameters of your RapidIO MegaCore function.
2. Perform one of the following steps:
   - In SOPC Builder, click Generate to generate the SOPC Builder system.
   - In the MegaWizard Plug-In Manager, click Finish to generate the RapidIO MegaCore function.

   The MegaWizard interface generates the Transport layer Verilog HDL file transport.v.
3. Open the newly generated transport.v file for editing.
4. Replace
   ```
   _Fstart_waddr = waddr ;
   with
   _Fstart_waddr = waddr + wren;
   ```
Solution Status
This issue is fixed in version 9.0 of the RapidIO MegaCore function.

Timeout Logic Can Incorrectly Extend Doorbell Transaction Timeout Period
When a DOORBELL transaction is transmitted, it is assigned a timeout value based on the Port Response Time-Out Control register (offset 0x124) and a free-running counter. When the counter reaches the timeout value, if the DOORBELL transaction has not yet received a response, the transaction times out. In the slowest case, the free-running counter increments every 64 Avalon clock cycles.

If DOORBELL transactions are transmitted fewer than 64 Avalon clock cycles apart, multiple transactions might be assigned the same timeout value. If processing the timeout for the previous DOORBELL transactions with the same timeout value takes too long, a DOORBELL transaction’s timeout might not be processed before the counter increments. In this case, the timeout is not recognized until the counter rolls over again to the same value. In addition, the timeout logic processes the pending transactions in FIFO order, and therefore does not examine the remaining pending DOORBELL transactions before the counter rolls over again.

Affected Configurations
All RapidIO variations that implement a Doorbell module.

Design Impact
A DOORBELL transaction might not time out when expected, holding up the timeout queue and preventing the Doorbell module from transmitting new transactions in a timely manner.

Workaround
To avoid this issue, ensure a wait of at least 64 Avalon clock cycles between transmission of DOORBELL transactions.

Solution Status
This issue is fixed in version 9.0 of the RapidIO MegaCore function.

Doorbell Transaction Can Be Transmitted With Invalid Transaction ID
A 17th pending DOORBELL transaction can have an invalid transaction ID. After reset, a counter generates 16 transaction IDs for the first 16 DOORBELL transactions. When a Doorbell response packet arrives at the Doorbell module, the transaction ID for the originating transaction is recycled through a FIFO and made available for a new pending DOORBELL transaction. However, a 17th pending DOORBELL transaction may use an underflowed TID FIFO output and be assigned a random value for its transaction ID.

Affected Configurations
All RapidIO variations that implement a Doorbell module.
Design Impact
A DOORBELL transaction can be transmitted with an invalid transaction ID. In this case, its response may not be identified correctly, and the Doorbell module can deadlock.

Workaround
To avoid this issue, ensure that 15 or fewer DOORBELL transactions are pending responses before you transmit the 17th DOORBELL transaction.

Solution Status
This issue is fixed in version 9.0 of the RapidIO MegaCore function.

User Guide Description of Default Value of EF_ID Field in PHEAD0 Register is Incorrect

The default value of the EF_ID field in the PHEAD0 register (offset 0x100), is listed incorrectly in the RapidIO MegaCore Function User Guide. The correct value is 0x0001.

Affected Configurations
All RapidIO variations.

Design Impact
Relying on the default value for the EF_ID field in the PHEAD0 register to be the value specified in the RapidIO MegaCore Function User Guide leads to incorrect results.

Workaround
Expect the default value 0x0001 in this register field.

Solution Status
This issue is fixed in version 9.0 of the RapidIO MegaCore function.

SOPC Builder Systems May Have Incorrectly Clocked Reset or Incorrect Calibration Clock Driver

A RapidIO transceiver-based system created in SOPC Builder might generate RTL with the source reset clock in the incorrect clock domain, or might connect the calibration clock port incorrectly.

Affected Configurations
All RapidIO variations with high-speed transceivers in SOPC Builder systems with multiple clocks.

Design Impact
If the calibration clock is driven by the wrong clock, transceiver calibration can fail, leading to hardware failures.
If the reset is driven by an incorrect clock, intermittent hardware failures may occur.
Workaround

If your design allows, you can avoid this issue by using a single clock for all components in your SOPC Builder system. However, cal_blk_clk runs at a maximum frequency of 125 MHz, and all transceiver-based designs in your system must have the same calibration clock. Therefore, not all designs admit this solution.

If you must implement multiple clocks in your design, perform the following alternate workaround to ensure your design is not impacted by this issue.

To determine whether the clock connections in your design are impacted by this issue, and fix them if needed, perform the following steps:

1. Open your SOPC Builder project.
2. In SOPC Builder, click Generate.
   
   SOPC Builder writes the top-level system file <SOPC_system_name>.v or <SOPC_system_name>.vhd, depending on the HDL you use.
3. Click Exit.
4. Open the newly generated top-level system .v or .vhd file for editing.
5. Search for the string the_rapidio to locate all your RapidIO MegaCore function instances.
6. For each instance, examine the signal connected to the cal_blk_clk port. In Verilog HDL, the relevant code line is similar to the following:
   `.cal_blk_clk (cal_blk_clk),
7. If the name in parentheses is not that of the calibration clock you want to connect to this port, replace it with your intended calibration clock.
8. For each instance, examine the signal connected to the reset_n port. In Verilog HDL, the relevant code line is similar to the following:
   `.reset_n (clk_0_reset_n),
9. If the clock name in the signal name in parentheses is not that of the clock connected to the Avalon system clock, replace it with the Avalon system clock. The following code line results:
   `.reset_n (<sysclk_name>_reset_n),

Solution Status

This issue is fixed in version 9.0 of the RapidIO MegaCore function.

Stratix IV Simulations May Fail With ModelSim 6.3g Compiler Optimizations Enabled

Simulation of a RapidIO MegaCore function targeted to a Stratix IV device using ModelSim 6.3g with compiler optimizations enabled, may fail. Compiler optimizations are enabled by default in this version of ModelSim.

Affected Configurations

All RapidIO variations that target a Stratix IV device.
Design Impact
The IP functional simulation model of an affected configuration may produce data errors if simulated using ModelSim 6.3g.

Workaround
To avoid this issue, perform one of the following workarounds:

- Disable the ModelSim compiler optimizations by adding the `--novopt` switch to the `vsim` command, in the `<variant>_run_modelsim.tcl` script or when you call `vsim` from the command line.
- Use ModelSim 6.4a.

Solution Status
This issue will be fixed in a future version of the RapidIO MegaCore function. The issue is fixed in ModelSim 6.4a.

RapidIO MegaCore Function v8.0 Targeting Arria GX Device and Generated in Quartus II v8.1 Software Cannot Simulate With the v8.0 Demo Testbench

If a RapidIO MegaCore function v8.0 instance that targets an Arria GX device is generated using the Quartus II software v8.1, it cannot simulate with the demonstration testbench. The testbench targets Stratix II GX libraries, but the generated IP functional simulation model requires Arria GX libraries.

Affected Configurations
All RapidIO MegaCore function v8.0 instances that target an Arria GX device and are compiled in the Quartus II software v8.1.

Design Impact
The demonstration testbench simulation does not run correctly with the affected configurations.

Workaround
To avoid this issue, perform one of the following workarounds:

- Upgrade to the RapidIO MegaCore function v8.1 and regenerate your configuration.
- If you are unable to upgrade to the RapidIO MegaCore function v8.1, perform the following steps:
  a. In your Quartus II project, open the generated `<variant>_run_modelsim.tcl` script in a text editor.
  b. In the Quartus Libraries section of the file, replace
     `append libraries {stratixiigx_stratixiigx_hssi}`
     `append lib_files {{stratixiigx_atoms.v} {stratixiigx_hssi_atoms.v}}`
     with

append libraries { stratixiigx stratixiigx_stratixiigx_hssi arriagx\ arriagx_hssi }
append lib_files {{stratixiigx_atoms.v} {stratixiigx_hassi_accounts.v} \ {arriagx_atoms.v} {arriagx_hassi_accounts.v}}

Solution Status
This issue is fixed in version 8.1 of the RapidIO MegaCore function.

SOPC Builder Systems Can Lose Read Data Returned From I/O Avalon-MM Slave Module

In a system generated using SOPC Builder, when more than eight outstanding reads are issued from the system interconnect fabric to the RapidIO I/O Avalon-MM slave module, the read data for some of the reads can be lost. Although the RapidIO I/O Avalon-MM slave module can accept 14 outstanding reads, the interconnect fabric cannot track more than 8 outstanding read requests to this module.

Affected Configurations
All RapidIO variations that implement an Avalon-MM I/O slave interface in an SOPC Builder system.

Design Impact
In the affected configurations, read data returned from the RapidIO link can be lost.

Workaround
Perform the following workaround:
1. Open your SOPC Builder project.
2. In the SOPC Builder, click Generate.
   SOPC Builder writes the generation system peripheral template file <SOPC_system_name>.ptf.
3. Click Exit.
4. Open the newly generated .ptf file for editing.
5. Under the definition for the io_read_slave, replace
   Maximum_Pending_Read_Transactions = "8";
   with
   Maximum_Pending_Read_Transactions = "14";
7. Open the Nios II EDS Command Shell.
8. Navigate to the directory in which your .ptf file is located.
9. Type sopc_builder --classic --generate to generate the new system.

Solution Status
This issue is fixed in version 8.1 of the RapidIO MegaCore function.
**Tx Port Write Control Register Priority Field Can Be Written to Invalid Value 2’b11**

A write of the value 2’b11 to the Tx Port Write Control register PRIORITY field is not overwritten to 2’b10 as stated in the RapidIO MegaCore Function User Guide. Instead, the invalid value 2’b11 remains and can cause incorrect scheduling of packets.

**Affected Configurations**
All RapidIO variations with the **Port Write Tx enable** option selected.

**Design Impact**
Incorrect scheduling of packets can occur if the value 2’b11 is written to the Tx Port Write Control register PRIORITY field.

**Workaround**
Avoid writing the value 2’b11 to the Tx Port Write Control register PRIORITY field.

**Solution Status**
This issue is fixed in version 8.1 of the RapidIO MegaCore function.

**Valid NREAD Requests Cause Unexpected Illegal Transaction Decode Error to Be Declared**

When an **NREAD** is the first received transaction or an **NREAD** follows a write transfer that has a smaller packet size than the **NREAD** transaction, the **NREAD** transaction can incorrectly flag the illegal transaction decode error bit (ILL_TRAN_DECODE) in the Logical/Transport Layer Error Detect CSR.

**Affected Configurations**
All RapidIO variations that implement an I/O Avalon-MM master module.

**Design Impact**
The illegal transaction decode error bit (ILL_TRAN_DECODE) in the Logical/transport Layer Error Detect CSR can be set incorrectly.

**Workaround**
Ignore the illegal transaction decode error bit (ILL_TRAN_DECODE) in the Logical/Transport Layer Error Detect CSR.

**Solution Status**
This issue is fixed in version 8.1 of the RapidIO MegaCore function.
sys_mnt_s_waitrequest is Asserted Intermittently When sys_mnt_s_chipselect is Asserted

The system maintenance Avalon-MM slave module intermittently asserts the sys_mnt_s_waitrequest signal when sys_mnt_s_chipselect is asserted, even if neither sys_mnt_s_read nor sys_mnt_s_write is asserted. In addition, if sys_mnt_s_read or sys_mnt_s_write is asserted while sys_mnt_s_waitrequest is asserted, the read or write transaction might not complete normally.

Affected Configurations
All RapidIO variations that implement a System Maintenance Avalon-MM slave module.

Design Impact
If sys_mnt_s_read or sys_mnt_s_write is asserted while sys_mnt_s_waitrequest is asserted, the read or write transaction might not complete correctly.

Workaround
Ensure that you assert the sys_mnt_s_chipselect signal only when sys_mnt_s_read or sys_mnt_s_write is asserted.

Solution Status
This issue is fixed in version 8.1 of the RapidIO MegaCore function.

Simultaneous Read and Write to the Doorbell Rx FIFO May Cause Doorbell Interrupt to Reset

If the Rx FIFO in the Doorbell module contains one outstanding DOORBELL message, a write to this FIFO is in process, and a read of this FIFO occurs at the same time as the write operation or a few clock cycles afterward, the drbell_s_irq signal may be inadvertently reset.

Affected Configurations
All RapidIO variations that implement a Doorbell module.

Design Impact
A DOORBELL message may remain in the Doorbell module Rx FIFO with no outstanding interrupt signal to indicate its presence to the Avalon-MM interface.

Workaround
After you detect a Doorbell interrupt on the drbell_s_irq line, read the Doorbell module Rx Doorbell Status register FIFO_LEVEL field to determine the number of outstanding messages in the Doorbell module Rx FIFO. Ensure that you process this number of messages. After you process all these outstanding messages, read the FIFO_LEVEL again to confirm the Doorbell module Rx FIFO is empty.
**Solution Status**
This issue is fixed in version 8.1 of the RapidIO MegaCore function.

**Writing 0xFFFF to the Host Base Device ID Lock CSR Locks the Register**

The `HOST_BASEDEVICE_ID` field of the Host Base Device ID Lock CSR resets to 0xFFFF when the lock is relinquished. However, if the value 0xFFFF is written to this register, the value incorrectly acquires the lock.

**Affected Configurations**
All RapidIO variations that implement a Transport layer.

**Design Impact**
If the register’s current value is 0xFFFF, write operations to the Host Base Device ID Lock CSR might be unsuccessful.

**Workaround**
After writing your base device ID to the HOST_BASEDEVICE_ID field of the Host Base Device ID Lock CSR, check that the value you wrote appears in the register. If the register contains the value 0xFFFF, write 0xFFFF to the register to unlock it, and then write your base device ID to the register again.

**Solution Status**
This issue is fixed in version 8.1 of the RapidIO MegaCore function.

**Cancelling a Packet Might Cause the Following Packet to be Lost**

If a Stomp control symbol arrives on the RapidIO link, followed too quickly by a Restart-from-retry control symbol, the first packet that follows the Restart-from-retry symbol can be lost. When this packet is received, a Packet-not-accepted control symbol is incorrectly sent, and the Link-request and Link-response control symbol exchange that ensues incorrectly indicates an incremented AckID for the packet that is rejected.

**Affected Configurations**
All serial RapidIO variations.

**Design Impact**
If this issue affects a request packet that does not require a response, the packet is dropped silently. If the issue affects a response packet or a request packet that requires a response, the remote endpoint times out waiting for the response.

**Workaround**
To avoid this issue or its design impact, perform one of the following workarounds:

- To avoid the issue, prevent link congestion, so that Stomp and Restart-from-retry control symbols are not issued.
To avoid a dropped packet caused by this issue, generate only request packets that require a response, such as WRITE_R transactions, and ensure that request packets are resubmitted after a timeout occurs.

**Solution Status**
This issue is fixed in version 8.1 of the RapidIO MegaCore function.

**Doorbell Interrupt Status Register TX_CPL_OVERFLOW Bit Cannot Be Cleared**
After the TX_CPL_OVERFLOW bit in the Doorbell Interrupt Status register is set, it cannot be reset.

**Affected Configurations**
All RapidIO variations that implement a Doorbell module.

**Design Impact**
The TX_CPL_OVERFLOW bit in the Doorbell Interrupt Status register cannot be reset. After it is set, therefore, any subsequent overflow conditions cannot be detected.

**Workaround**
To mitigate this issue, perform one of the following three workarounds:

- Send fewer than sixteen DOORBELL transactions at a time, and ensure that the Doorbell module Tx Completion buffer is read as soon as each DOORBELL transaction completes. This workaround avoids overflow of the Tx Completion buffer.

- Disable the TX_CPR_OVERFLOW bit in the Doorbell Interrupt Status register by clearing the TX_CPL_OVERFLOW bit in the Doorbell Interrupt Enable register. This workaround avoids notification if the Tx Completion buffer overflows.

- Avoid use of the Tx Completion buffer for successful outbound DOORBELL messages by clearing the COMPLETED bit of the Tx Doorbell Status Control register.

**Solution Status**
This issue is fixed in version 8.1 of the RapidIO MegaCore function.

**Problems After a Read Transaction Address is Outside the Enabled Address Mapping Windows**
After a read transaction to an address outside the enabled address mapping windows is attempted on the Input/Output Avalon-MM slave interface, the RapidIO MegaCore function can send two or more request packets with the same transaction ID or it can continuously assert the io_s_rd_waitrequest or io_s_wr_waitrequest signal.

**Affected Configurations**
All RapidIO variations that implement an Input/Output Avalon-MM slave interface.
Design Impact
A response packet might be matched with the wrong request packet, or the Input/Output Avalon-MM read or write slave interface might stall by asserting the wait-request signal indefinitely.

Workaround
Avoid submitting Avalon-MM read transactions with addresses outside the enabled address mapping windows to the Input/Output Avalon-MM read slave interface. For example, you can define and enable an address mapping window that includes all possible addresses.

Solution Status
This issue is fixed in version 8.1 of the RapidIO MegaCore function.

RapidIO MegaWizard Interface Does Not Set Transceiver VCCH to 1.2 V
If VCCH is set to 1.2 V in the RapidIO MegaWizard interface, the value remains at the default setting of 1.5 V in the transceiver.

Affected Configurations
All Stratix II GX RapidIO variations that implement a transceiver with a VCCH setting of 1.2 V.

Design Impact
The RapidIO MegaWizard interface cannot be used to implement a transceiver with VCCH set to 1.2 V.

Workaround
To set the RapidIO transceiver VCCH to 1.2 V, perform the following workaround:
1. Generate the RapidIO MegaCore function using the MegaWizard interface.
2. In a text editor, open the generated transceiver wrapper file, <variation_name>_riophy_gxb.v.
3. In the alt2gxb component defparm section, replace
   alt2gxb_component.tx_analog_power="1.5v"
   with
   alt2gxb_component.tx_analog_power="1.2v"

Solution Status
This issue is fixed in version 8.0 SP1 of the RapidIO MegaCore function.
Receipt of a Write Request for 5, 6, or 7 Bytes by the I/O Master Causes an Invalid Avalon-MM Burst Transaction

If a RapidIO Input/Output Avalon-MM master Logical layer module in a 1× (32-bit wide) RapidIO MegaCore variation receives an NWRITE or NWRITE_R write request for 5, 6, or 7 bytes of data, the module creates an invalid Avalon-MM burst transaction. The module translates the request to a burst with burstcount value 2 but with different byteenable values in the two cycles. The Avalon-MM interface specification requires that a burst have a uniform byteenable value.

Affected Configurations

All RapidIO 1× variations that implement an Input/Output Avalon-MM master Logical layer module.

Design Impact

When this violation of the Avalon-MM interface specification occurs, the behavior of an Avalon-MM slave connected to this Avalon-MM master is undefined.

Workaround

Avoid sending write requests for 5, 6, or 7 bytes in the system, or add a small adapter to translate these two-word bursts to two single-word transfers.

Solution Status

This issue will be fixed in a future release of the RapidIO MegaCore function.

Incorrect I/O Logical Layer Avalon-MM Slave Write Request Packets

The RapidIO Input/Output Logical layer Avalon-MM slave can generate an incorrect write request packet if an invalid combination of burstcount, byteenable, and address is applied to the datapath write Avalon-MM slave interface.

Affected Configurations

This issue affects all variations that include the Input/Output logical layer module.

Design Impact

An incorrect write request packet can be sent. This incorrect packet may cause further complications in the attached devices.

Workaround

Avoid using invalid combinations of burstcount, byteenable, and address. The valid combinations are described in the "Avalon-MM Burstcount and Byteenable Encoding in RapidIO Packets" section in the Functional Description chapter of the RapidIO MegaCore Function User Guide.
**Solution Status**

RapidIO MegaCore function versions 7.1 and beyond check for several invalid combinations, and do not generate a write request on the RapidIO link in these cases. Future versions of the RapidIO MegaCore function will check for additional invalid combinations. However, Altera recommends that you avoid the use of invalid combinations of burstcount, byteenable, and address in any version of the RapidIO MegaCore function.
Revision History

Table 18–1 shows the revision history for the QDRII SRAM MegaCore function.

For more information about the new features, refer to the *QDRII SRAM MegaCore Function User Guide*.

Table 18–1. QDRII SRAM MegaCore Function Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.0 SP2</td>
<td>July 2009</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>9.0 SP1</td>
<td>May 2009</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>9.0</td>
<td>March 2009</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>Maintenance release.</td>
</tr>
</tbody>
</table>

Errata

Table 18–2 shows the issues that affect the QDRII SRAM MegaCore function v9.0 SP2, 9.0 SP1, 9.0, 8.1, and 8.0.

Not all issues affect all versions of the QDRII SRAM MegaCore function.

Table 18–2. QDRII SRAM MegaCore Function Errata

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Jul 09</td>
<td>Incorrect User Guide on ACDS</td>
<td>Fixed</td>
</tr>
<tr>
<td>15 May 08</td>
<td>Termination Error When Compiling Design</td>
<td>✓</td>
</tr>
<tr>
<td>01 Dec 06</td>
<td>Incorrect IP Toolbench Latency Behavior</td>
<td>✓</td>
</tr>
<tr>
<td>01 Nov 06</td>
<td>Simulating with the VCS Simulator</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>TimeQuest Timing Analyzer Failure</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>PLL Placement</td>
<td>✓</td>
</tr>
<tr>
<td>01 Nov 05</td>
<td>Constraints Errors With Companion Devices</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>Supported Device Families</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>Compilation Error (Stratix II Series &amp; HardCopy II Devices Only)</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>Gate-Level Simulation Filenames</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>The ModelSim Simulation Script Does Not Support Companion Devices</td>
<td>✓</td>
</tr>
</tbody>
</table>
Incorrect User Guide on ACDS

The user guide that is on the Altera Complete Design Suite (ACDS) is an out-of-date version.

**Affected Configurations**
This issue affects no configurations.

**Design Impact**
There is no design impact.

**Workaround**
Download the latest *QDRII SRAM MegaCore Function User Guide* from the Altera website.

**Solution Status**
This issue is fixed in version 9.0 SP2 of the QDRII SRAM MegaCore function.

Termination Error When Compiling Design

The Fitter reports the following error: “Error Bidirectional I/O “cq” uses the parallel termination but does not have dynamic termination control.”

**Affected Configurations**
This issue affects designs using the QDRII SRAM Controller.

**Design Impact**
The design fails to fit.

**Workaround**
At top-level design, change the pin direction from inout to input for
- `qdrii_cq_<index>; qdrii_cqn_<index>`.

**Solution Status**
This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

Incorrect IP Toolbench Latency Behavior

When you open the IP Toolbench Parameterize window, you can select any latency for the default QDRII, but it only supports 1.5.

**Affected Configurations**
This issue affects all QDRII SRAM configurations.

**Design Impact**
IP Toolbench does not generate a variation and gives the following error message:
MegaCore Function Generation Error
IP Functional Simulation creation Failed. The following error was returned:
Error: Top-level design entity
"qdr_auk_qdrii_sram_avalon_controller_ipfs_wrap" is undefined.

Workaround
For longer latency, select QDRII+.

Solution Status
This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

Simulating with the VCS Simulator
The QDRII SRAM Controller MegaCore function does not support the VCS simulator.

Affected Configurations
This issue affects all configurations.

Design Impact
The design does not simulate.

Workaround
There is no workaround for VHDL simulations. For Verilog HDL simulations. Change line 154 in the qdrii_model.v file to:

begin : f1
Also, change line 417 to:

begin : f2

Solution Status
This issue will not be fixed.

TimeQuest Timing Analyzer Failure
When you use the Quartus II TimeQuest timing analyzer, it reports a recovery issue, because the reset is not in the same clock domain as the system clock.

Affected Configurations
This issue affects all configurations.

Design Impact
This issue has no design impact.

Workaround
Change the reset sequence for the signals clocked on the CQ clock, before you run the TimeQuest timing analyzer.
**Solution Status**

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

**PLL Placement**

The IP Toolbench-generated example design uses a PLL phase shift of 90°, which can cause the design to fail hold timing analysis. The source synchronous PLL for the read capture should have a location constraint to place it on the same side of the device as the Q pins; otherwise, the source synchronous compensation does not compensate for the expected delays.

**Affected Configurations**

This issue affects all configurations.

**Design Impact**

The design fails hold timing analysis.

**Workaround**

The PLL must be located on the same side of the device as the CQ/CQn groups, for the PLL to compensate properly.

**Solution Status**

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

**Constraints Errors With Companion Devices**

When you change the device in your project or add a HardCopy II companion device to a Stratix II project and you reopen the variation with IP Toolbench, the constraints editor sometimes does not show all previously set byte groups in the floorplan. The constraints editor only shows the constraints applied to byte groups that are valid for the current device.

**Affected Configurations**

This issue affects all configurations.

**Design Impact**

The design fails.

**Workaround**

Reassign the byte groups for the new device in the constraints editor.

**Solution Status**

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.
Supported Device Families

The QDRII SRAM Controller MegaCore function only supports Stratix and Stratix II series, and HardCopy II devices. However, if you choose an unsupported device for your Quartus II project and subsequently start the MegaWizard Plug-In Manager, you can choose a different device family in the MegaWizard Plug-In Manager, which allows you to choose the QDRII SRAM Controller MegaCore function. There are no error messages when you perform this illegal operation.

Affected Configurations
This issue affects all configurations.

Design Impact
You cannot compile a design.

Workaround
Ensure you choose a supported device family for the Quartus II project.

Solution Status
This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

Compilation Error (Stratix II Series & HardCopy II Devices Only)

The IP Toolbench Constraints window allows the illegal situation where you can share DQ groups on the top and bottom banks for Stratix II series and HardCopy devices. When you compile your design the Quartus II software issues a no fit error.

Affected Configurations
This issue affects all DQS mode QDRII SRAM controllers on Stratix II series and HardCopy II devices.

Design Impact
When you choose Start Compilation, there is an error message and the design does not compile.

Workaround
If you are targeting Stratix II series or HardCopy II devices, in the Constraints window ensure you choose bytegroups on either the top or the bottom of the device, but not both.

Solution Status
This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.
Gate-Level Simulation Filenames

Various Quartus II software options may cause it to generate a netlist with a different filename than that expected by the gate-level simulation script. The simulation script expects `<project name>.vho` or `.vo` and `<project name>_v` or `_vhd.sdo` files to be present.

Affected Configurations
This issue affects all configurations.

Design Impact
You cannot run gate-level simulations.

Workaround
For VHDL gate-level simulations, in the `simulation/modelsim` directory follow these steps:

1. Rename `<filename>.vho` file to `<project name>.vho`.
2. Rename `<filename>.sdo` file to `<project name>_vhd.sdo`.

For Verilog HDL gate-level simulations, in the `simulation/modelsim` directory follow these steps:

1. Rename the `<filename>.vo` file to `<project name>.vo`.
2. Rename the `<filename>.sdo` file to `<project name>_v.sdo`.
3. In the `<project name>.vo` file change the following line to point to the `<project name>_v.sdo` file:
   ```
   initial $sdf_annotate("<project name>_v.sdo");
   ```

Solution Status
This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

The ModelSim Simulation Script Does Not Support Companion Devices

If you have a HardCopy II companion device in a Stratix II project, be aware that the ModelSim simulation scripts do not work if you change to your companion device.

Affected Configurations
This issue affects designs with companion devices.

Design Impact
The simulation script does not run.

Workaround
Edit the ModelSim script to include the correct libraries.

Solution Status
This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.
19. Reed-Solomon Compiler

Revision History

Table 19–1 shows the revision history for the Reed-Solomon Compiler.

For more information about the new features, refer to the Reed-Solomon Compiler User Guide.

Table 19–1. Reed-Solomon Compiler Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.0 SP1</td>
<td>May 2009</td>
<td>Preliminary support for HardCopy III and HardCopy IV E devices.</td>
</tr>
<tr>
<td>9.0</td>
<td>March 2009</td>
<td>Preliminary support for Arria II GX devices.</td>
</tr>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>Full support for Stratix III devices.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>■ Full support for Cyclone III devices</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Preliminary support for Stratix IV devices</td>
</tr>
</tbody>
</table>

Errata

Table 19–2 shows the issues that affect the Reed-Solomon Compiler v9.0, 8.1, and 8.0.

Not all issues affect all versions of the Reed-Solomon Compiler.

Table 19–2. Reed-Solomon Compiler Errata

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 Mar 09</td>
<td>User Guide Link from IP Toolbench is Inactive</td>
<td>9.0  8.1  8.0</td>
</tr>
<tr>
<td>01 Nov 08</td>
<td>Verilog HDL Simulation Fails</td>
<td>✔    ✔    —</td>
</tr>
<tr>
<td></td>
<td>RS Decoder Fails When Number of Check Symbols and Symbols are Similar</td>
<td>✔    ✔    —</td>
</tr>
<tr>
<td></td>
<td>Display Symbol Button in IP Toolbench is Missing</td>
<td>✔    ✔    —</td>
</tr>
<tr>
<td></td>
<td>Verilog HDL Designs Do Not Simulate in Synopsys VCS</td>
<td>—    Fixed ✔</td>
</tr>
<tr>
<td></td>
<td>No Symbol In IP Toolbench Symbol Window</td>
<td>—    Fixed ✔</td>
</tr>
<tr>
<td></td>
<td>File Summary Does Not List All Generated Files</td>
<td>—    Fixed ✔</td>
</tr>
<tr>
<td>01 Oct 07</td>
<td>Cannot Find Memory Initialization File If Not in Project Directory</td>
<td>✔    ✔    ✔</td>
</tr>
</tbody>
</table>

User Guide Link from IP Toolbench is Inactive

In IP Toolbench, if you click the Document tab the link to the Reed-Solomon User Guide is inactive.

Affected Configurations

This issue affects all variable decoder designs.
Design Impact
This issue has no design impact.

Workaround
You can access the current Reed-Solomon Compiler User Guide from the Altera website.

Solution Status
This issue will be fixed in a future version of the Reed-Solomon Compiler.

Verilog HDL Simulation Fails
Running a simulation with the Verilog HDL testbench results in an empty summary_output.txt file.

Affected Configurations
This issue affects all Verilog HDL configurations.

Design Impact
You cannot use the summary_output.txt file to evaluate the functionality of the design. But you can evaluate the functionality by looking at the simulation waveform.

Workaround
Run the simulation with a VHDL design and use the VHDL testbench.

Solution Status
This issue will be fixed in a future release of the Reed-Solomon Compiler.

RS Decoder Fails When Number of Check Symbols and Symbols are Similar
With the variable decoder, when the Number of check symbols and Symbols per codeword values are similar, for example, 5 and 6, respectively, the Avalon-ST interface on the source side fails and the sop and eop overlap.

Affected Configurations
This issue affects all variable decoder designs.

Design Impact
The design fails.

Workaround
This issue has no workaround.

Solution Status
This issue will be fixed in a future version of the Reed-Solomon Compiler.
Display Symbol Button in IP Toolbench is Missing

The Display Symbol button in IP Toolbench does not appear, even though the screenshot in the user guide implies it should appear.

Affected Configurations
This issue affects all designs.

Design Impact
There is no design impact.

Workaround
This issue has no workaround.

Solution Status
This issue will be fixed in a future version of the Reed-Solomon Compiler.

Verilog HDL Designs Do Not Simulate in Synopsys VCS

When you simulate a Reed-Solomon Verilog HDL design in Synopsys VCS (2006.06-SP1), you receive an error message.

Affected Configurations
This issue affects all Verilog HDL designs.

Design Impact
You cannot simulate a Verilog HDL design in VCS.

Workaround
There is currently no workaround.

Solution Status
This issue will be fixed in a future release of the Reed-Solomon Compiler.

No Symbol In IP Toolbench Symbol Window

When you click Display Symbol, IP Toolbench does not always display a symbol.

Affected Configurations
This issue affects all configurations.

Design Impact
There is no design impact.

Workaround
To see a symbol, click Step 1: Parameterize, click Finish, click Display Symbol.
**Solution Status**
This issue will be fixed in a future version of the Reed-Solomon Compiler.

**File Summary Does Not List All Generated Files**
The file summary on the IP Toolbench Generate window does not always list all the generated files.

**Affected Configurations**
This issue affects all configurations.

**Design Impact**
There is no design impact.

**Workaround**
In the Parameterize window, when you finish parameterizing your variation, do not click Finish, just go to IP Toolbench and click Generate.

**Solution Status**
This issue will be fixed in a future version of the Reed-Solomon Compiler.

**Cannot Find Memory Initialization File if Not in Project Directory**
The Quartus II software cannot find the memory initialization files (HEX files) required by the design and issues a critical warning of the form:

```
Critical Warning: Can't find Memory Initialization File or Hexadecimal (Intel-Format) File C:/temp/mlab_test/fir_test0_coef_0.hex -- setting all initial values to 0
```

**Affected Configurations**
This issue is observed when the generated IP files are not in the same directory as your project setting files .qsf and .qpf files. For example, if your project involves many submodules and each submodule resides in a separate subdirectory.

**Design Impact**
The Quartus II software issues critical warnings for the missing files and generates a functionally incorrect netlist due to the missing memory initialization files.

**Workaround**
Add the path of the folder containing your generated IP files to the user libraries parameter in the .qsf file. For example, if your top level project directory is C:/myprojects/bigSystem and you have generated the Reed Solomon module in C:/myprojects/bigSystem/RSmodule/.

In your project’s .qsf file (in C:/myprojects/bigSystem), look for a line that starts set_global_assignment -name USER_LIBRARIES ...
Append the IP directory \texttt{C:/myprojects/bigSystem/RSmodule} with the following code:

\begin{verbatim}
set_global_assignment -name USER_LIBRARIES
"C:/altera/72/ip/reed_solomon/lib;C:/myprojects/bigSystem/RSmodule"
\end{verbatim}

After you save your changes, recompile your project and check that the critical warning is no longer displayed.

**Solution Status**

This issue will be fixed a future version of the Reed-Solomon Compiler.
Revision History

Table 20–1 shows the revision history for the RLDRAM II MegaCore function.

For more information about the new features, refer to the *RLDRAM II MegaCore Function User Guide*.

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.0 SP2</td>
<td>July 2009</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>9.0 SP1</td>
<td>May 2009</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>9.0</td>
<td>March 2009</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>8.1</td>
<td>15 November 2008</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>8.0</td>
<td>15 May 2008</td>
<td>Maintenance release.</td>
</tr>
</tbody>
</table>

Errata

Table 20–2 shows the issues that affect the RLDRAM II MegaCore function v9.0 SP2, 9.0 SP1, 9.0, 8.1, and 8.0.

Not all issues affect all versions of the RLDRAM II MegaCore function.

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Jul 09</td>
<td>Incorrect User Guide on ACDS</td>
<td>Fixed</td>
</tr>
<tr>
<td>15 Mar 09</td>
<td>RLDRAM II Verilog HDL Design Does Not Work</td>
<td>—</td>
</tr>
<tr>
<td>01 Nov 08</td>
<td>Error When Upgrading</td>
<td>—</td>
</tr>
<tr>
<td>01 Dec 06</td>
<td>NativeLink Fails with the ModelSim Simulator</td>
<td>✓</td>
</tr>
<tr>
<td>01 Nov 06</td>
<td>Add an RLDRAM II Controller to a Project with Other Memory Controllers</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>Simulating with the NCSim Software</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>Simulating with the VCS Simulator</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>Multiple Instances of the auk_ddr_functions.vhd File</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>Gate-Level Simulation Filenames</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>Unpredictable Results for Gate-Level Simulations (HardCopy II Devices Only)</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>Editing the Custom Variation (non-DQS Mode)</td>
<td>✓</td>
</tr>
</tbody>
</table>
Incorrect User Guide on ACDS

The user guide that is on the Altera Complete Design Suite (ACDS) is an out-of-date version.

**Affected Configurations**

This issue affects no configurations.

**Design Impact**

There is no design impact.

**Workaround**

Download the latest *RLDRAM II MegaCore Function User Guide* from the Altera website.

**Solution Status**

This issue is fixed in version 9.0 SP2 of the RLDRAM II MegaCore function.

RLDRAM II Verilog HDL Design Does Not Work

If you generate a Verilog HDL instance of the RLDRAM II Controller version 8.1, the design will not work in hardware or simulation.

**Affected Configurations**

This issue affects all Verilog HDL configurations. VHDL designs are not affected.

**Workaround**

If you require a Verilog HDL instance of the RLDRAM II Controller MegaCore function, you can use one of the following workarounds:

- Continue to use your existing version 8.0 instance. There are no functional changes between versions 8.0 and 8.1 of the RLDRAM II Controller MegaCore function, so you are not required to upgrade.
If you choose to update your existing instance or if you do not have a version 8.0 instance, change all instances of the line:

```plaintext
else if (0)
```
to

```plaintext
else if (1)
```
in the following files:

- `<variation name>_auk_rldramii_addr_cmd_reg.v`
- `<variation name>_auk_rldramii_dqs_group.v`
- `<variation name>_auk_rldramii_pipeline_addr_cmd.v`
- `<variation name>_auk_rldramii_pipeline_qvld.v`
- `<variation name>_auk_rldramii_pipeline_rdata.v`
- `<variation name>_auk_rldramii_pipeline_wdata.v`

Some files may only require editing if pipeline options are enabled in your RLDRAM II Controller MegaCore variation.

**Design Impact**

Your design will not work in hardware or simulation.

**Solution Status**

This issue is fixed in version 9.0 of the RLDRAM II Controller MegaCore function.

**Error When Upgrading**

If you upgrade an existing custom variation of the RLDRAM II MegaCore function to a newer version, for example from v7.1 to v7.2, the following error occurs:

```
Error (10430): VHDL Primary Unit Declaration error at
auk_rldramii_functions.vhd(5): primary unit "auk_rldramii_functions"
already exists in library "work"
```

IP Toolbench adds files to your Quartus II project when you generate your custom variation. When you upgrade your MegaCore function, the same files from the previous and current versions are present in the same Quartus II project, which causes a VHDL error.

**Affected Configurations**

This issue affects all designs that were created in a previous version of the MegaCore function and then upgraded.

**Workaround**

From your Quartus II project, remove the Device Design Files that were added by the earlier version of the MegaCore function. These files can be identified by the files’ directory names.

**Design Impact**

You cannot compile your Quartus II project until you remove the duplicate files.
Solution Status
This issue is fixed in version 8.1 of the RLDRAM II Controller MegaCore function.

NativeLink Fails with the ModelSim Simulator
When using NativeLink to run VHDL gate-level simulations using the ModelSim software, the simulation fails with the following error message:

```
# ** Error: (vcom-19) Failed to access library 'altera' at "altera".
```

Affected Configurations
The issue affects VHDL gate-level simulations.

Design Impact
The design does not simulate.

Workaround
The following lines need to be added to the NativeLink-generated gate-level simulation script:

```
vlib vhdl_libs/altera
vmap altera vhdl_libs/altera
vcom -work altera <Quartus installation directory>/libraries/vhdl/altera/altera_europa_support_lib.vhd
```

Solution Status
This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

Add an RLDRAM II Controller to a Project with Other Memory Controllers
If you try to generate a new RLDRAM II controller in a project that already contains a DDR, DDR2, QDRII, or RLDRAM II controller, the example design gets corrupted and the compilation fails.

Affected Configurations
This issue affects all configurations.

Design Impact
The design does not compile.

Workaround
To workaround this issue, follow these steps:

1. Generate the RLDRAM II controller in a new project and update the required project to instantiate the new RLDRAM II controller.
2. Copy the constraints from the new RLDRAM II project to the target project.
3. Copy the new RLDRAM II design files into the target project directory.
**Solution Status**
This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

**Simulating with the NCSim Software**
The RLDRAM II Controller MegaCore function does not fully support the NCSim software.

**Affected Configurations**
This issue affects all configurations.

**Design Impact**
The design does not simulate.

**Workaround**
Set the `-relax` switch for all calls to the VHDL or Verilog HDL analyzer.

**Solution Status**
This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

**Simulating with the VCS Simulator**
The RLDRAM II Controller MegaCore function does not fully support the VCS simulator.

**Affected Configurations**
This issue affects all configurations.

**Design Impact**
The design does not simulate.
Workaround

For VHDL simulations, in the `<variation name>_example_driver.vhd` file, change all `when` statements from:

```vhdl
   when std_logic_vector’("<bit_pattern>")
```

to:

```vhdl
   when "<bit_pattern>"
```

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

Multiple Instances of the auk_ddr_functions.vhd File

When a project contains multiple memory MegaCore functions, the Quartus II project has multiple instances of the `auk_ddr_functions.vhd` file (one per MegaCore function).

Affected Configurations

This issue affects all configurations.

Design Impact

The Quartus II project fails during compilation.

Workaround

Remove the `auk_ddr_functions.vhd` file associated with the RLDRAM II controller from the list of files added to the Quartus II project, by choosing Add/Remove Files from Project on the Project menu. Keep only the `auk_ddr_functions.vhd` file associated with the DDR or DDR2 SDRAM controller.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

Gate-Level Simulation Filenames

Various Quartus II software options may cause the Quartus II software to generate a netlist with a different filename than that expected by the gate-level simulation script. The simulation script expects `<project name>.vho` or `.vo` and `<project name>_v` or `_vhd.sdo` files to be present.

Affected Configurations

This issue affects all configurations.

Design Impact

You cannot run gate-level simulations.
Workaround
For VHDL gate-level simulations, in the simulation/modelsim directory, follow these steps:
1. Rename `<filename>.vho` file to `<project name>.vho`.
2. Rename `<filename>.sdo` file to `<project name>_vhd.sdo`.

For Verilog HDL gate-level simulations, in the simulation/modelsim directory, follow these steps:
1. Rename the `<filename>.vo` file to `<project name>.vo`.
2. Rename the `<filename>.sdo` file to `<project name>_v.sdo`.
3. In the `<project name>.vo` file, change the following line to point to the `<project name>_v.sdo` file:
   ```
   initial sdf_annotate("<project name>_v.sdo");
   ```

Solution Status
This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

Unpredictable Results for Gate-Level Simulations (HardCopy II Devices Only)
Gate-level simulations may not work as expected on HardCopy II devices, because HardCopy II timing is preliminary in the Quartus II software.

Affected Configurations
This issue affects all configurations on HardCopy II devices.

Design Impact
This issue has no design impact.

Workaround
None.

Solution Status
This issue will be fixed in a future version of the Quartus II software.

Editing the Custom Variation (non-DQS Mode)
When you generate a non-DQS mode custom variation with large databus widths, you may encounter one of the following characteristics when you try to edit the custom variation:

- IP Toolbench does not reload
- IP Toolbench reloads, but the databus width and constraints are set to the default for the selected RLDRAM II device
- IP Toolbench reloads, but the databus width is set to the default value for the selected RLDRAM II device and the constraints floorplan shows no chosen byte groups
Affected Configurations
This issue affects non-DQS mode designs only.

Design Impact
This issue has no design impact if you implement the workaround.

Workaround
Use one of the following workarounds:

- If IP Toolbench does not reload, you must regenerate a new custom variation and re-enter your parameters
- If IP Toolbench reloads, but the databus width and constraints are set to the default, reselect the databus width and rechoose the byte groups in the constraints floorplan
- If IP Toolbench reloads, but the databus width is set to the default and the constraints floorplan shows no byte groups, reselect the databus width and rechoose the byte groups in the constraints floorplan

Solution Status
This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.
21. SDI

Revision History

Table 21–1 shows the revision history for the SDI MegaCore function.

For more information about the new features, refer to the SDI MegaCore Function User Guide.

Table 21–1. SDI MegaCore Function Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.0 SP2</td>
<td>July 2009</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>9.0 SP1</td>
<td>May 2009</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>9.0</td>
<td>March 2009</td>
<td>Preliminary support for Arria II GX devices.</td>
</tr>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>■ Preliminary support for Stratix IV devices.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Added GX transceiver based core for Arria GX devices.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Improved receiver lock algorithm—minimization of resets between standards changes and improved tolerance of corrupt SDI streams.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Updated 425MB support.</td>
</tr>
</tbody>
</table>

Errata

Table 21–2 shows the issues that affect the SDI MegaCore function v9.0 SP2, 9.0 SP1, 9.0, 8.1, and 8.0.

Not all issues affect all versions of the SDI MegaCore function.

Table 21–2. SDI MegaCore Function Errata

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Jul 09</td>
<td>Incorrect User Guide on ACDS</td>
<td>Fixed</td>
</tr>
<tr>
<td>15 Jun 09</td>
<td>No Support for IP Advisor</td>
<td>☑ ☑ — — — — — —</td>
</tr>
<tr>
<td>15 Apr 09</td>
<td>The Interface Signals Do Not Behave As Expected</td>
<td>☑ ☑ ☑ — — — —</td>
</tr>
<tr>
<td>15 Mar 09</td>
<td>Transmitter Line Number (LN) Insertion</td>
<td>☑ ☑ ☑ ☑ — — — —</td>
</tr>
<tr>
<td></td>
<td>Cyclical Redundancy Check (CRC) Error When Receiving 3G-SDI 425MB-A Input</td>
<td>— — Fixed ☑ —</td>
</tr>
</tbody>
</table>
### Incorrect User Guide on ACDS

The user guide that is on the Altera Complete Design Suite (ACDS) is an out-of-date version.

**Affected Configurations**

This issue affects no configurations.

**Design Impact**

There is no design impact.

**Workaround**

Download the latest *SDI MegaCore Function User Guide* from the Altera website.

**Solution Status**

This issue is fixed in version 9.0 SP2 of the SDI MegaCore function.

### No Support for IP Advisor

The *SDI MegaCore Function User Guide* incorrectly states that the SDI MegaCore function supports IP Advisor.

**Affected Configurations**

This issue affects no configurations.

**Design Impact**

There is no design impact.

**Workaround**

None.

**Solution Status**

This issue will be fixed in version 9.1 of the *SDI MegaCore Function User Guide*. 
The Interface Signals Do Not Behave As Expected

The interface signals, \textit{rx\_xyz}, \textit{xyz\_valid}, and \textit{rx\_eav}, are asserted at the next word after the actual XYZ word. These interface signals should be asserted to accompany the actual XYZ word.

**Affected Configurations**
This issue affects the receiver and duplex SDI MegaCore functions.

**Design Impact**

You cannot rely on these signals to detect the current XYZ word.

**Workaround**

To detect the current XYZ word, create a counter and count. Three word counts after \textit{rx\_trs} is asserted indicates that the current word is XYZ word. Decode \textit{rxdata} for its validity and to indicate that the current TRS is EAV.

**Solution Status**

This issue will be fixed in a future version of the SDI MegaCore function.

Transmitter Line Number (LN) Insertion

The LN insertion feature on the SDI MegaCore transmitter function does not perform correctly. The line information appears on the chroma channel but not on the luma channel.

**Affected Configurations**

This issue affects the transmitter and duplex MegaCore functions.

**Design Impact**

The Tektronix WFM700 equipment does not recognize the HD-SDI signal transmitted by the SDI MegaCore transmitter.

**Workaround**

Connect the LN word to the upper 11 bits of \textit{tx\_ln} signal.

For example:

\textit{tx\_ln} [21:0] Input  HD-SDI: bits 21:11 LN; bits 10:0 LN

- Dual link: bits 21:11 LN link B; bits 10:0 LN link A
- 3G-SDI Level A: bits 21:11 LN; bits 10:0 LN
- 3G-SDI Level B: bits 21:11 LN link B; bits 10:0 LN link A

**Solution Status**

This issue will be fixed in a future version of the SDI MegaCore function.
Cyclical Redundancy Check (CRC) Error When Receiving 3G-SDI 425M-A Input

The SDI MegaCore function reports CRC error when receiving 3G-SDI 425M-A input. The SDI MegaCore function intermittently outputs corrupted data on the \texttt{rxdata} port, and the \texttt{rx_status[3]}, \texttt{rx_status[4]}, and \texttt{rx_in} bits go to zero.

**Affected Configurations**
This issue affects all SDI MegaCore triple-rate and 3G-SDI receiver functions.

**Design Impact**
The \texttt{rxdata} port is intermittently corrupted causing CRC error.

**Workaround**
None.

**Solution Status**
This issue is fixed in version 9.0 of the SDI MegaCore function.

SDI Receiver Misdetects Data Rate

The SDI MegaCore receiver function intermittently misdetects data rate.

**Affected Configurations**
This issue affects all SDI MegaCore triple-rate receiver functions.

**Design Impact**
Your design intermittently fails to detect the correct data rate in the hardware.

- During fast unplug/plug HD-SDI, it occasionally misdetects as 3G-SDI.
- During fast unplug/plug 3G-SDI, it occasionally misdetects as HD-SDI or SD-SDI.

**Workaround**
Apply the patch provided in the Quartus II version 8.0 SP1 patch 1.18, regenerate the SDI MegaCore function, and recompile in the Quartus II software.

**Solution Status**
This issue is fixed in version 8.1 of the SDI MegaCore function.

SDI Receiver Fails to Align

The SDI MegaCore receiver function fails to align with partial complete frame.

**Affected Configurations**
This issue affects all SDI MegaCore triple-rate receiver functions.

**Design Impact**
Your design fails in hardware.
Workaround
Apply the patch provided in the Quartus II version 8.1 patch 0.12, regenerate the SDI MegaCore function, and recompile in the Quartus II software.

Solution Status
This issue is fixed in version 8.1 of the SDI MegaCore function.

Example Designs Are Out of Date
The example designs and testbenches included in the simulation directory were generated with v7.2 of the SDI MegaCore function. They must be updated before they can be used correctly with v8.0 of the SDI MegaCore function.

Affected Configurations
This issue affects HD-SDI, HD-SDI 3G and HD-SDI dual-link examples in the simulation directory.

Design Impact
The example designs do not successfully simulate. There is no impact on your design.

Workaround
The three examples require different steps to upgrade them to work with v8.0 of the SDI MegaCore function.

- To simulate the HD-SDI example, which is stored in the simulation/hdsdi directory, you must regenerate the SDI instance by opening it in the version 8.0 of the MegaWizard and clicking Finish. You must also update the testbench by connecting the upper 11 bits of the 22 bit transmit line number signal to zero as shown in the following codes:

```vhdl
hd_duplex hd_duplex_inst
(
    ...
    .tx_ln   ( {11'b0, gen_ln} ), // connect the upper 11 bits to zero
);
```

- To simulate the HD-SDI 3G example, which is stored in the simulation/hdsdi_3g directory, you must regenerate the SDI instance by opening it in the version 8.0 of the MegaWizard and clicking Finish. You must also update the testbench by adding the connections to SDI instance and connecting the upper 11 bits of the 22 bit transmit line number signal to zero as shown in the following codes:

```vhdl
hd_3g_duplex hd_3g_duplex_inst
(
    ...
    .gxb2_cal_clk              (sdi_ref), // required for hard serdes designs
    .tx_data_valid_a_bn     (1'b1),
    .tx_data_type_a_bn     (1'b1),
    .tx_ln   ( {11'b0, gen_ln} ), // connect the upper 11 bits to zero
);
```

- To simulate the HD-SDI dual-link example, which is stored in the simulation/hdsdi_dual_link directory, you must regenerate the SDI instance by opening it in the version 8.0 of the MegaWizard and clicking Finish. No changes are required to the testbench.
Solution Status
This issue is fixed in version 8.1 of the SDI MegaCore function.

Quartus II Fitter Reports Error When PLL-Generated Clock of 67.5 MHz Is Used in Stratix GX Devices
The Quartus II Fitter reports an error when you use PLL-generated clock inputs of 67.5 MHz frequency in SDI-SD MegaCore targeting Stratix GX devices.

Affected Configurations
This issue affects all Stratix GX SDI-SD MegaCore functions with PLL-generated clock inputs of 67.5 MHz frequency.

Design Impact
The design cannot be fitted in the device.

Workaround
Set the input clock to 29.7 MHz frequency so that the PLL generates the frequency of the output clock to 74.25 MHz.

Solution Status
This issue will be fixed in a future version of the SDI MegaCore function.

NativeLink Fails With ModelSim Simulator
When using NativeLink to run simulations with the ModelSim simulator, the testbench fails.

Affected Configurations
This issue affects all configurations.

Design Impact
The design does not simulate and the testbench reports a failure.

Workaround
Use the ModelSim simulation scripts provided by Altera or carry out the following steps:
1. Edit the NativeLink generated script to command “vsim -t 100fs”.
2. Reexecute the script in ModelSim.

Solution Status
This issue will be fixed in a future version of the SDI MegaCore function.
Timing Not Met in C5 Speed Grade Stratix II GX Devices

The 3-Gbps and triple rate variants of the SDI MegaCore function may not meet the timing requirements in the C5 speed grade device of the Stratix II GX device family.

Affected Configurations
This issue affects the 3-Gbps and triple-rate SDI MegaCore functions.

Design Impact
Your design does not meet timing requirements.

Workaround
Use either a C4 or C3 speed grade device.

Solution Status
This issue will be fixed in a future version of the SDI MegaCore function.
Revision History

Table 22–1 shows the revision history for the SerialLite II MegaCore function.

For more information about the new features, refer to the SerialLite II MegaCore Function User Guide.

Table 22–1. SerialLite II MegaCore Function Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.0 SP2</td>
<td>July 2009</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>9.0 SP1</td>
<td>May 2009</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>9.0</td>
<td>March 2009</td>
<td>Preliminary support for Arria II GX devices.</td>
</tr>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>8.0 SP1</td>
<td>July 2008</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>Preliminary support for Stratix IV devices.</td>
</tr>
</tbody>
</table>

Errata

Table 22–2 shows the issues that affect the SerialLite II MegaCore v9.0 SP2, 9.0 SP1, 9.0, 8.1, and 8.0.

Not all issues affect all versions of the SerialLite II MegaCore.

Table 22–2. SerialLite II MegaCore Function Errata (Part 1 of 2)

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Jul 09</td>
<td>Incorrect User Guide on ACDS</td>
<td>9.0 SP2 9.0 SP1 9.0 8.1 8.0 SP1 8.0</td>
</tr>
<tr>
<td>15 Apr 09</td>
<td>Simulating Streaming Mode Design with a Non-Default Reference Clock Frequency Selected</td>
<td>✓ ✓ ✓ ✓ ✓ ✓</td>
</tr>
<tr>
<td>15 Mar 09</td>
<td>Selecting Non-Default Input Clock Frequency Value for Stratix IV GX Devices</td>
<td>✓ ✓ ✓ — — —</td>
</tr>
<tr>
<td>01 Nov 08</td>
<td>Demo Testbench Cannot Be Simulated With Arria GX Variants</td>
<td>— — — Fixed ✓ ✓</td>
</tr>
<tr>
<td></td>
<td>Timing Analyzer Reports “Critical Warning: Timing Requirements Not Met”</td>
<td>— — — Fixed ✓ —</td>
</tr>
<tr>
<td></td>
<td>Stratix IV Internal Core Clocking Is Incorrect for a Design Using TSIZE = 2 and Data Rate &gt; 3,125 Mbps</td>
<td>— — — Fixed ✓ ✓</td>
</tr>
</tbody>
</table>
Incorrect User Guide on ACDS

The user guide that is on the Altera Complete Design Suite (ACDS) is an out-of-date version.

Affected Configurations
This issue affects no configurations.

Design Impact
There is no design impact.

Workaround
Download the latest SerialLite II MegaCore Function User Guide from the Altera website.

Solution Status
This issue is fixed in version 9.0 SP2 of the SerialLite MegaCore function.

Simulating Streaming Mode Design with a Non-Default Reference Clock Frequency Selected

If you have selected a streaming mode design together with a non-default reference clock frequency, the IP Functional Simulation model fails to simulate. The default reference clock frequency is defined as (data rate / (transfer size *10)). Any frequency that is not equal to the formula is non-default.

Affected Configurations
This issue affects all designs that have enabled the Streaming data type option with non-default reference clock frequency.

Design Impact
None.

Table 22–2. SerialLite II MegaCore Function Errata (Part 2 of 2)

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 May 08</td>
<td>Link Management FIFO May Overflow When Small Packets Are Sent Continuously Over a Long Period of Time.</td>
<td>9.0 SP2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>8.0 SP1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>8.0</td>
</tr>
<tr>
<td>01 Dec 06</td>
<td>Rx Only Mode With Clock Compensation Does Not Support All Reference Clock Selections</td>
<td>9.0 SP1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>8.0</td>
</tr>
<tr>
<td>01 Dec 06</td>
<td>Generation Fails or Corrupt Variation Generated if Asymmetric Broadcast Mode Used</td>
<td>9.0 SP1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>8.0</td>
</tr>
</tbody>
</table>
Workaround
To enable the IP Functional Simulation model to simulate successfully, perform the following steps:
1. Open the <design_name>_tb.v file.
2. In the following strings, change the value of N to equate
   \[ N = \left(\frac{1}{(\text{data rate} \div (\text{transfer size} \times 10)}) \right) \times 1000000. \]
   
   \[ \text{parameter arclk_period = N; } \]
   \[ \text{parameter atclk_period = N; } \]

Solution Status
This issue will be fixed in a future version of the SerialLite II MegaCore function

Selecting Non-Default Input Clock Frequency Value for Stratix IV GX Devices

The Quartus II reports an error and fails to compile your design, if you choose the 3,125-Mbps data rate and specify 97.6562-Mhz for input clock frequency.

Affected Configurations
This issue affects all configurations targeting Stratix IV with 3,125-Mbps data rate and 97.6562-Mhz input clock frequency.

Design Impact
The Quartus II software fails to compile your design.

Workaround
To compile your design successfully, perform the following steps:
1. Open the <variation name>_slite2_xcvr.v file.
2. Locate the string 97.6562, and replace the string with 97.65625.
3. Recompile your design with the Quartus II software.

Solution Status
This issue will be fixed in version 9.1 of the SerialLite II MegaCore function

Demo Testbench Cannot Be Simulated With Arria GX Variants

When the SerialLite II MegaCore version 8.0 is generated using the Quartus II software version 8.1, the demonstration testbench simulation script targets Stratix II GX libraries, instead of the required Arria GX libraries. A syntax error occurs indicating a required library is missing.

Affected Configurations
This issue affects all variations of the SerialLite II version 8.0 designs compiled in the Quartus II software version 8.1 targeting the Arria GX devices.
Design Impact
The demonstration testbench simulation is unable to run.

Workaround
Upgrade the IP to version 8.1, and regenerate your configuration.
If you are unable to upgrade the IP, follow these steps:
1. Open the <variation name>_run_modelsim.tcl script.
2. Locate the Quartus II Libraries section of the file, and add the following commands:
   append libraries {arriagx arriagx_hssi }
   append lib_files {{arriagx_atoms.v} {arriagx_hssi_atoms.v} }

Solution Status
This issue is fixed in version 8.1 of the SerialLite II MegaCore function.

Timing Analyzer Reports “Critical Warning: Timing Requirements Not Met”
The Quartus II TimeQuest Timing Analyzer reports that certain SerialLite II designs fail to meet timing requirements on one of the following clocks:
slite2_top_inst|xcvr_inst|alt4gxb_component|auto_generated|transmit_pcs0|clkout
slite2_top_inst|xcvr_inst|alt4gxb_component|auto_generated|receive_pcs0|clkout
The failure is a negative hold slack, normally a very small figure (less than 0.05ns).

Affected Configurations
This issue affects selected SerialLite II designs targeting the Stratix IV family.

Design Impact
The design may fail to function properly on hardware if the TimeQuest timing analyzer reports that timing requirements are not met.

Workaround
Add this command into the <quartus project name>.qsf file:
set_global_assignment -name OPTIMIZE_HOLD_TIMING "ALL PATHS"
or
Follow these steps:
1. Open the Quartus II software.
2. On the Assignments menu, click Settings and select Fitter Settings.
3. Enable the Optimize hold timing: option and select All paths from the drop-down menu.
4. Click OK to save your settings.
**Solution Status**
This issue is fixed in version 8.1 of the SerialLite II MegaCore function.

**Stratix IV Internal Core Clocking Is Incorrect for a Design Using TSIZE = 2 and Data Rate > 3,125 Mbps**

Due to an error in the transceiver parameters, a variation using Stratix IV, TSIZE = 2 and a data rate greater than 3,125 Mbps, fails to use the proper transceiver clocking.

**Affected Configurations**
This issue affects all SerialLite-II variations using Stratix IV, transfer size of 2, and a data rate greater than 3,125 Mbps.

**Design Impact**
While simulation works fine, the design does not meet the timing requirements on the transceiver output clocks. If the design is implemented in hardware, data errors may occur.

**Workaround**
Open the generated transceiver wrapper file (<variation name>_slite2_xcvr.v) in a text editor. Make the following changes to the alt4gxb component defparam section:

```vhdl
// Change:
alt4gxb_component.rx_rate_match_fifo_mode = "normal", // Change (Was None)
alt4gxb_component.rx_use_clkout="false", // Change (Was True)
// Add:
alt4gxb_component.rx_rate_match_pattern1 = "00110000111010000011", // Add
alt4gxb_component.rx_rate_match_pattern2 = "11001111000101111100", // Add
alt4gxb_component.rx_rate_match_pattern_size = 20, // Add
alt4gxb_component.rx_use_rate_match_pattern1_only = "false", // Add
```

**Solution Status**
This issue is fixed in version 8.1 of the SerialLite II MegaCore function.

**Link Management FIFO May Overflow When Small Packets Are Sent Continuously Over a Long Period of Time.**

For configurations that have the Enable flow control option turned on and small packets are sent continuously for a significant amount of time (more than 50 clock cycles), the processing of the link management packets will be delayed indefinitely. This causes the Link Management FIFO to overflow. Small packet means packet with sizes equal to or less than (TSIZE * TX_NUM_LANES) bytes.

**Affected Configurations**
This issue affects all configurations that have the Enable flow control option turned on, and when small packets are sent continuously over the link for a long period of time.
**Design Impact**  
The link management FIFO will overflow, and flow control gets delayed indefinitely, resulting in loss of data.

**Workaround**  
Do not send small packets continuously for a long period of time. Allow a few idle clock cycles in between the small packets every 20 clock cycles.

**Solution Status**  
This issue is fixed in version 8.0 SP1 of the SerialLite II MegaCore function.

---

**Rx Only Mode With Clock Compensation Does Not Support All Reference Clock Selections**

For a Non-Stratix GX receiver only configuration with Clock Compensation turned on, the GUI currently allows multiple reference clock selections. Choosing a reference clock frequency in mode less than $\text{RefFreq} = \text{DRATE} / (\text{TSIZE} \times 10)$, causes the rate match FIFO to overflow.

**Affected Configurations**  
This issue affects all receiver only SerialLite-II variations in a non-Stratix GX family when Clock Compensation is turned on, with the reference clock set to a frequency less than $\text{DRATE} / (\text{TSIZE} \times 10)$.

**Design Impact**  
The internal rate match FIFO will overflow, causing data loss.

**Workaround**  
Do not use a lower frequency reference clock.

or

Turn off Clock Compensation in this configuration. The data is transmitted out of the Rx core on the $rrefclk$ domain instead of the $trefclk$ domain.

**Solution Status**  
Configurations that cause this error can no longer be generated.

---

**Generation Fails or Corrupt Variation Generated if Asymmetric Broadcast Mode Used**

The SerialLite II MegaCore function fails to generate or generates corrupted variations that use the broadcast mode in an asymmetric configuration.

If the state machine is not self-synchronized, the syntax error shown in Figure 22–1 appears and the generation fails. If the state machine is self-synchronized, an invalid configuration is generated, data is corrupted, and the testbench fails.
Chapter 22: SerialLite II  
Errata

Affected Configurations
This issue affects configurations that use the broadcast mode and for which the transmitter number of lanes does not equal the receiver number of lanes (asymmetric).

Design Impact
If the state machine is not self-synchronized, the syntax error shown in Figure 22–1 appears and the generation fails. If the state machine is self-synchronized, an invalid configuration is generated, data is corrupted, and the testbench fails.

Workaround
If the self-synchronized state machine is required, use the MegaWizard interface to generate a transmitter-only broadcast variation. Use the MegaWizard interface again to generate a single lane receiver-only self-synchronized variation. Then instantiate as many of these receiver variations as required to match the number of lanes needed.

You cannot select options such as retry-on-error and flow control for your workaround variation.

If self-synchronized state machine is not required, there is no workaround other than to use a self-synchronized state machine and configure the system as previously described.

Solution Status
Configurations that cause this error can no longer be generated.
Revision History

Table 23–1 shows the revision history for the Triple Speed Ethernet MegaCore function.

For more information about the new features, refer to the *Triple Speed Ethernet MegaCore Function User Guide*.

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.0 SP2</td>
<td>July 2009</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>9.0 SP1</td>
<td>May 2009</td>
<td>Preliminary support for HardCopy III and HardCopy IV E devices.</td>
</tr>
<tr>
<td>9.0</td>
<td>March 2009</td>
<td>■ Preliminary support for Arria II GX device family.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Support for different speeds in multi-port MACs.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Option to extend the width of selected statistics counters to 64 bits.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Support for 64 Kbyte frame length.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Implemented 125-MHz clock enable signals in the physical coding sublayer (PCS) function to</td>
</tr>
<tr>
<td></td>
<td></td>
<td>replace the internal SGMII clock generator blocks.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Added a new field, <code>disable_rd_timeout</code> (bit 27), in the <code>command_config</code> register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Added a new parameter in the top-level file that specifies the depth of the synchronizer chain.</td>
</tr>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>Support for dynamic reconfiguration.</td>
</tr>
<tr>
<td>8.0 SP1</td>
<td>July 2008</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>■ Preliminary support for Stratix IV device family.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Support for multi-port MAC.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Option to exclude internal FIFO buffers during synthesis.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Support for Reduced Gigabit Media Independent Interface (RGMII) in fast Ethernet (10/100 Mbps).</td>
</tr>
</tbody>
</table>

Errata

Table 23–2 shows the issues that affect the Triple Speed Ethernet MegaCore function v9.0 SP2, 9.0 SP1, 9.0, 8.1, 8.0 SP1, and 8.0.

Not all issues affect all versions of the Triple Speed Ethernet MegaCore function.
Half-Duplex Late Collision in MACs Corrupts Next Packets

Half-duplex late collisions in media access control (MAC) functions cause the following errors:

- Late collision that happens 17 bytes before the end of packet (EOP) corrupts the next outgoing packet, and may cause the subsequent packets to underflow.
- MAC continues transmitting packets even when the user logic stops providing packets to the Avalon-ST transmit interface.
**Affected Configurations**
This issue affects all configurations that contain MACs operating in half-duplex mode.

**Workaround**
None.

**Solution Status**
This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

**MACs in Half-Duplex Mode Continue Transmitting Packets**
MACs with internal 8-bit FIFO buffers in half-duplex mode continue transmitting packets even when the user logic stops providing packets to the Avalon-ST transmit interface.

**Affected Configurations**
This issue affects all configurations that contain MACs with internal 8-bit FIFO buffers operating in half-duplex mode.

**Workaround**
None.

**Solution Status**
This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

**Incorrect User Guide on ACDS**
The user guide that is on the Altera Complete Design Suite (ACDS) is an out-of-date version.

**Affected Configurations**
This issue affects no configurations.

**Design Impact**
There is no design impact.

**Workaround**
Download the latest *Triple Speed Ethernet MegaCore Function User Guide* from the Altera website.

**Solution Status**
This issue is fixed in version 9.0 SP2 of the Triple Speed Ethernet MegaCore function.
Reconfig_clk Frequency Violates Device Specification

A single clock source drives both the reconfig_clk input port of the reconfiguration block and an internal clock, fixedclk_fast. Because the internal clock accepts only a frequency of 125 MHz, the clock source is set to the same frequency. This frequency, however, violates the frequency range of the reconfig_clk input port specified for the device, which is between 37.5 and 50 MHz.

Affected Configurations

All configurations that use GXB transceivers.

Workaround

Change the internal clock speed to accept a value between 37.5 and 50 MHz by setting fixedclk_fast to 0 in altera_tse_gxb_gige_inst.v, and set the frequency of the clock source that drives both reconfig_clk and fixedclk_fast to a value within the same range.

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Timing Not Met When System Clock is Set to High Frequency

Configurations that contain 10/100/1000 Mbps Ethernet MAC only variations do not meet timing when the system clock is set to a frequency higher than 75 MHz.

Affected Configurations

All configurations that contain 10/100/1000 Mbps Ethernet MAC only variations.

Workaround

Add the system clock to the following command in the .sdc file, as shown:

```
set_clock_groups -exclusive -group
{rx_clk_to_the_triple_speed_ethernet_0} -group
{tx_clk_to_the_triple_speed_ethernet_0} -group {clk}
```

Solution Status

This issue is fixed in version 9.0 of the Triple Speed Ethernet MegaCore function.

Half-Duplex Collision in MACs Without Internal FIFO Buffers

Half-duplex collisions in MAC functions without internal FIFO buffers cause the following errors:

- Retransmission fails if collision happens during the transmission of the preamble, start frame delimiter, and source address.
- Collision that happens after the transmission of 64 bytes of the packet corrupts the next outgoing packet.
Collision remains undetected if it happens during the reception of the final six bytes of the packet.

**Affected Configurations**
This issue affects all configurations that contain MACs without internal FIFO buffers operating in half-duplex mode.

**Workaround**
None.

**Solution Status**
This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

**Half-Duplex Collision in MACs With Internal FIFO Buffers**
Half-duplex collisions that occur during the reception of the final six bytes of the packet remain undetected in MACs with internal FIFO buffers.

**Affected Configuration**
This issue affects all configurations that contain MACs with internal FIFO buffers operating in half-duplex mode.

**Workaround**
None.

**Solution Status**
This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

**Timing Not Met in Stratix III, Stratix IV, and Arria II GX Devices**
Designs that use the default clock resource assignments may not meet timing.

**Affected Configuration**
This issue may affect Stratix III, Stratix IV, or Arria II GX designs that contain the multi-port 10/100/1000 Mbps Ethernet MAC with 1000BASE-X/SGMII PCS variation.

**Workaround**
Assign each instance of tbi_tx_clk to the periphery clock by adding the following assignment for each port in the Quartus II settings file (.qsf):

```quartus
set_instance_assignment -name GLOBAL_SIGNAL "PERIPHERY CLOCK" -to tbi_tx_clk_0
```

**Solution Status**
This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.
Timing Not Met in Cyclone III Devices

Designs targeted to Cyclone III devices may not meet timing when the skew optimization option is turned on by default.

Affected Configuration
This issue may affect variations in designs targeted to Cyclone III devices.

Workaround
Turn off the skew optimization option by adding the following assignment in the Quartus II settings file (.qsf):

```
set_global_assignment -name ENABLE_BENEFICIAL_SKEW OPTIMIZATION OFF
```

Solution Status
This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Connection Point Validation Fails in SOPC Builder

The connection point validation fails for SOPC Builder systems that contain the MAC block without internal FIFO buffers and the physical coding sublayer (PCS) block with embedded gigabit transceiver block. This variation of the Triple Speed Ethernet MegaCore function contains two unassociated clocks, `rx_afull_clk` and `cal_blk_clk`, but SOPC Builder only allows for one unassociated clock.

Affected Configuration
This issue affects all SOPC Builder systems that contain the 10/100/1000 Ethernet MAC with 1000BASE-X/SMII PCS variation with the following options:

- Use internal FIFO is turned off.
- Use transceiver block and GXB are selected.

Workaround
None.

Solution Status
This issue is fixed in version 9.0 of the Triple Speed Ethernet MegaCore function.

Intermittent Payload Corruption When 32-Bit Byte Alignment is On

The payload is occasionally corrupted when 32-bit byte alignment is turned on in MACs without internal FIFO buffers.

Affected Configuration
This issue affects all configurations that contain the core variations 10/100/1000 Mbps Ethernet MAC only or 10/100/1000 Mbps Ethernet MAC with 1000BASE-X/SMII PCS with the following options:

- Use internal FIFO is turned off
Align packet headers to 32-bit boundaries is turned on

Workaround
None.

Solution Status
This issue is fixed in version 9.0 of the Triple Speed Ethernet MegaCore function.

Testbench Compilation Fails When Using Nativelink with ModelSim

The following error occurs during the testbench compilation when Nativelink is used with ModelSim:

```
# ** Error: (vlog-7) Failed to open design unit file
"D:/altera/81/ip/altera/triple_speed_ethernet/lib/altera_tse_alt2gxb_gige.vo" in read mode.
# No such file or directory. (errno = ENOENT)
# Error in macro ./tse_run_msim_rtl_verilog.do line 9
```

This error is caused by a wrong extension in the Nativelink Tcl script.

Affected Configuration
This issue affects any configuration with the following characteristics:
- Targets Stratix II GX or Arria GX.
- Contains the 10/100/1000 Ethernet MAC with 1000BASE-X/SGMII PCS or 1000BASE-X/SGMII PCS variation.
- Turns on the Use transceiver block option.

Workaround
Edit the script `tse_run_msim_rtl_<verilog>hdle>.do` and change the extension of `altera_tse_alt2gxb_gige.vo` to `.v`.

Solution Status
This issue is fixed in version 9.0 of the Triple Speed Ethernet MegaCore function.

Timing Not Met in 12-Port Configurations Targetting Stratix IV Devices

Twelve-port configurations that target the Stratix IV device family and implement LVDS I/O do not meet timing.

Affected Configuration
This issue affects only 12-port configurations that target the Stratix IV device family and implement LVDS I/O.

Workaround
None.

Solution Status
This issue is fixed in version 9.0 of the Triple Speed Ethernet MegaCore function.
**Limited Multi-Port Support in Cyclone III and Arria GX Device Families**

Full multi-port support is not available in configurations targeting Cyclone III and Arria GX device families due to device limitations. In these device families, the number of ports supported are 1, 4, 8, and 12.

**Affected Configuration**
This issue affects all configurations.

**Workaround**
None.

**Solution Status**
This information will be added in a future version of the *Triple Speed Ethernet MegaCore Function User Guide*.

**Incorrect Number of Packets Received During Simulation**

At the end of a simulation, the number of packets received by the MAC function in affected configurations is one packet less than expected. The MAC function is expected to receive the same number of packets generated by the frame generator and sent to the MAC function. This discrepancy is caused by the simulation model incorrectly initializing the memory block in the PCS receive FIFO converter.

**Affected Configuration**
This issue affects all configurations that contain the *10/100/1000 Mbps Ethernet MAC with 1000BASE-X/SGMII PCS* variation with the following options:

- Generated in Verilog HDL.
- Use internal FIFO is turned off.
- Use transceiver block is turned on.
- Enable SGMII bridge logic is turned on.

**Workaround**
None.

**Solution Status**
This issue is fixed in version 8.1 of the Triple Speed Ethernet MegaCore function.

**Simulation Fails in NC Sim When Using VHDL Testbench**

The signal `preamble_len` ranges from 0 to 15 in the VHDL testbench files (`*_tb.vhd`) but from 0 to 40 in the frame generator files (`ethgen2.vhd` and `ethgen.vhd`). This discrepancy causes simulation to fail in NC Sim simulator.

**Affected Configurations**
This issue affects all configurations in VHDL simulated in the NC Sim simulator.
Workaround
Before running the simulation, change the upper range 15 to 40 in the following line in the VHDL testbench files (*.tb.vhd):

```vhdl
prmble_len : in integer range 0 to 15; -- length of preamble
```

Solution Status
This issue is fixed in version 8.1 of the Triple Speed Ethernet MegaCore function.

Bit SW_RESET is Not Cleared After Software Reset

When a software reset is triggered by setting the SW_RESET bit in the command_config register to 1, the bit is not cleared at the end of the software reset.

Affected Configurations
This issue affects all configurations that contain the multi-port MAC function with the options Use internal FIFO and Implement statistics counter turned off.

Workaround
Set the bits SW_RESET and CNT_RESET in the command_config register to trigger a software reset.

Solution Status
This issue is fixed in version 8.1 of the Triple Speed Ethernet MegaCore function.

Simulation Fails in ModelSim

Simulating the MegaCore function in ModelSim fails when the MegaCore function is generated in Verilog HDL with RGMII selected. The core includes unnecessary media independent interface (MII) signals in the top-level file which conflict with the signal definitions in the loopback module.

Affected Configuration
This issue affects all configurations that are instantiated in SOPC Builder with RGMII and Verilog HDL selected.

Workaround
Remove the MII signals from the top-level file generated by the SOPC Builder.

Solution Status
This issue is fixed in version 8.1 of the Triple Speed Ethernet MegaCore function.

Incorrect Detection of Physical Layer Component
The software driver of the Triple Speed Ethernet MegaCore function detects the Marvell 88E1145 Ethernet transceiver as a Marvell 88E1111 transceiver and the National DP83848C Ethernet transceiver as a National DP83865 transceiver. In the latter, the software driver does not configure the MAC operating speed and duplex mode correctly.
Affected Configuration
This issue affects all configurations.

Workaround
Replace line 1206 in `altera_avalon_tse.c` with the following line:

```c
if((phy_profiles[i]->oui == oui) && (phy_profiles[i]->model_number == model_number))
```

Solution Status
This issue is fixed in version 8.1 of the Triple Speed Ethernet MegaCore function.

Non-Compliant Implementation of Bit PAGE_RECEIVE in PCS Register
The Triple Speed Ethernet MegaCore function sets the PAGE_RECEIVE bit in the PCS register `an_expansion` to 1 when a /C/ ordered set is received. This behavior does not comply with the IEEE 802.3 Standard clause 37.

Affected Configuration
This issue affects all configurations that include the PCS function.

Workaround
None.

Solution Status
This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Non-Compliant Implementation of aAlignmentError Statistics Counter
The Triple Speed Ethernet MegaCore function increments the aAlignmentError statistics counter when an SFD error is encountered. This behavior does not comply with the IEEE 802.3 Standard clause 5.2.2.1.7.

Affected Configuration
This issue affects all configurations.

Workaround
None.

Solution Status
This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Software Driver Realigns Data Unnecessarily
The software driver aligns all data including already aligned data. This behavior results in unnecessary processing time.
Affected Configuration
This issue affects all configurations.

Design Impact
The performance drops when the payload is sent in small packets.

Workaround
Replace the condition in line 540 in the source file ins_tse_mac.c with the following condition:

```c
if((unsigned int)data & 0x03) == 0)
```

Solution Status
This issue is fixed in version 8.0 SP1 of the Triple Speed Ethernet MegaCore function.

Software Driver Does Not Update Bit ENA_10 When Operating Speed Changes to 10 Mbps

The ENA_10 bit in the command_config register, which is directly wired to the signal ena_10, is not updated by the software driver when the operating speed of the MAC changes to 10Mbps.

Affected Configuration
This issue affects configurations in RGMII mode that use the provided software driver and rely on the signal ena_10 to determine the speed of the MAC.

Design Impact
The design stops working when the operating speed changes to 10 Mbps.

Workaround
Edit the source files as shown in Table 23–3.

<table>
<thead>
<tr>
<th>Source File</th>
<th>Type of Edit</th>
<th>New Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>altera_avalon_tse.c</td>
<td>Replace line 750 with the new code.</td>
<td>result = ((is100 &amp; 0x01) &lt;&lt; 2)</td>
</tr>
<tr>
<td>Ins_tse_mac.c</td>
<td>Insert the new code before line 740.</td>
<td>is100 = alt_tse_phy_rd_mdio_reg(pphy, pphy-&gt;pphy_profile-&gt;status_reg_location, pphy-&gt;pphy_profile-&gt;speed_lsb_location, 1);</td>
</tr>
<tr>
<td>Ins_tse_mac.c</td>
<td>Insert the new code before line 594.</td>
<td>alt_u8 is100 = 0;</td>
</tr>
<tr>
<td>Ins_tse_mac.c</td>
<td>Insert the new code before line 424.</td>
<td>if((is100 == 0) &amp; (is1000 == 0)) { dat</td>
</tr>
<tr>
<td>Ins_tse_mac.c</td>
<td>Insert the new code before line 284.</td>
<td>is100 = (result &gt;&gt; 2) &amp; 0x01;</td>
</tr>
<tr>
<td>Ins_tse_mac.c</td>
<td>Insert the new code before line 201.</td>
<td>int is100 = 0;</td>
</tr>
</tbody>
</table>
Solution Status

This issue is fixed in version 8.1 of the Triple Speed Ethernet MegaCore function.
Revision History

Table 24–1 shows the revision history for the UTOPIA Level 2 Master MegaCore function.

For more information about the new features, refer to the UTOPIA Level 2 Master MegaCore Function User Guide.

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.0</td>
<td>March 2009</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>Full support for Stratix III devices.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>■ Full support for Cyclone III devices</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Preliminary support for Stratix IV devices</td>
</tr>
</tbody>
</table>

Errata

There are no issues that affect the UTOPIA Level 2 Master MegaCore function v9.0, 8.1, and 8.0.
Revision History

Table 25–1 shows the revision history for the UTOPIA Level 2 Slave MegaCore function.

For more information about the new features, refer to the UTOPIA Level 2 Slave MegaCore Function User Guide.

Table 25–1. UTOPIA Level 2 Slave MegaCore Function Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.0</td>
<td>March 2009</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>Full support for Stratix III devices.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>■ Full support for Cyclone III devices</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Preliminary support for Stratix IV devices</td>
</tr>
</tbody>
</table>

Errata

There are no issues that affect the UTOPIA Level 2 Slave MegaCore function v9.0, 8.1, and 8.0.
# 26. Video and Image Processing Suite

## Revision History

Table 26–1 shows the revision history of the Video and Image Processing Suite MegaCore functions.

For information about the new features, refer to the Video and Image Processing Suite User Guide.

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.0 SP1</td>
<td>May 2009</td>
<td>Preliminary support for HardCopy III and HardCopy IV E.</td>
</tr>
</tbody>
</table>
| 9.0     | March 2009     | ■ The Deinterlacer MegaCore function supports controlled frame dropping or repeating to keep the input and output frame rates locked together.  
■ The Test Pattern Generator MegaCore function can generate a user-specified constant color that can be used as a uniform background.  
■ Preliminary support for Arria II GX devices. |
| 8.1     | November 2008  | ■ Added new Test Pattern Generator.  
■ The Deinterlacer supports pass-through mode and run-time algorithm switching.  
■ The Deinterlacer and Frame Buffer support clock crossing for improved external memory access efficiency.  
■ The Clocked Video Input and Clocked Video Output support run-time switching between standard definition (SD) and high definition (HD) video streams.  
■ The Color Space Converter supports run-time changing of coefficients.  
■ The Gamma Corrector supports parallel data processing for three channels.  
■ The 2D FIR Filter supports run-time changing of coefficients.  
■ Full support for Stratix III devices.  
■ Withdrawn support for UNIX. |
| 8.0 SP1 | July 2008      | Fixed several errata issues (see Table 26–2). |
| 8.0     | May 2008       | ■ Added new Clipper, Clocked Video Input, Clocked Video Output, Frame Buffer, and Color Plane Sequencer MegaCore functions.  
■ All MegaCore functions now support 2,600 pixels height and width.  
■ Alpha Blending Mixer and Deinterlacer support parallel processing for 1080p60.  
■ Full support for Cyclone III devices.  
■ Preliminary support for Stratix IV devices. |
Errata

Table 26–2 shows the issues that affect the Video and Image Processing Suite MegaCore functions v9.0, v8.1, v8.0 SP1, and v8.0.

Not all issues affect all versions of the Video and Image Processing Suite MegaCore function.

Table 26–2. Video and Image Processing Suite Errata

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Jul 09</td>
<td>Deinterlacer and Frame Buffer Connected to DDR3 May Not Work Properly</td>
<td>v9.0,v8.1,v8.0SP1,v8.0</td>
</tr>
<tr>
<td>15 Mar 09</td>
<td>RTL Simulation Reports Errors When Using Verilog HDL</td>
<td>v9.0,v8.1,v8.0SP1,v8.0</td>
</tr>
<tr>
<td></td>
<td>Incorrect Simulation Models Created for Deinterlacer and Frame Buffer</td>
<td>v9.0,v8.1,v8.0SP1,v8.0</td>
</tr>
<tr>
<td></td>
<td>Deinterlacer and Test Pattern Generator May Not Upgrade</td>
<td>v9.0,v8.1,v8.0SP1,v8.0</td>
</tr>
<tr>
<td></td>
<td>The 2D Median Filter Does Not Support 7×7 Filter Size</td>
<td>v9.0,v8.1,v8.0SP1,v8.0</td>
</tr>
<tr>
<td></td>
<td>Misleading Error Message Issued by Color Plane Sequencer</td>
<td>Fixed</td>
</tr>
<tr>
<td></td>
<td>Changing Target Device After Quartus II Compilation Causes Error</td>
<td>Fixed</td>
</tr>
<tr>
<td></td>
<td>Active Picture Line Selection Should be Available for Separate Sync Mode</td>
<td>Fixed</td>
</tr>
<tr>
<td></td>
<td>v7.2 MegaCore Functions are Not Compatible with v8.x Quartus II</td>
<td>v9.0,v8.1,v8.0SP1,v8.0</td>
</tr>
<tr>
<td></td>
<td>Packets Sent to VIP Cores Must Have Non-Empty Payload</td>
<td>v9.0,v8.1,v8.0SP1,v8.0</td>
</tr>
<tr>
<td>01 Nov 08</td>
<td>Control Port Behavior Unpredictable for Scaler and Clipper</td>
<td>Fixed</td>
</tr>
<tr>
<td></td>
<td>Error in Clocked Video Output Constraint File</td>
<td>Fixed</td>
</tr>
<tr>
<td></td>
<td>Simulation Models Not Created For Clocked Video Functions</td>
<td>Fixed</td>
</tr>
<tr>
<td></td>
<td>Cannot Connect Adapter in SOPC Builder For Multiple Parallel Planes</td>
<td>Fixed</td>
</tr>
<tr>
<td></td>
<td>Line Buffer Compiler Does Not Generate for Arria GX</td>
<td>Fixed</td>
</tr>
<tr>
<td></td>
<td>Misleading Warning Message for Color Plane Sequencer</td>
<td>Fixed</td>
</tr>
<tr>
<td></td>
<td>Color Plane Sequencer Does Not Report GUI Messages</td>
<td>Fixed</td>
</tr>
<tr>
<td></td>
<td>The .hex Files for Simulation in SOPC Builder Systems Must be Moved</td>
<td>Fixed</td>
</tr>
<tr>
<td>15 Jul 08</td>
<td>Deinterlacer Fails to Generate in Some Configurations</td>
<td>Fixed</td>
</tr>
<tr>
<td></td>
<td>Color Plane Sequencer Shows Parallel Bit Ranges in Reverse Order</td>
<td>Fixed</td>
</tr>
<tr>
<td></td>
<td>Clipper Fails to Send EOP When Active Region is Bottom Right</td>
<td>Fixed</td>
</tr>
<tr>
<td>15 Jul 08</td>
<td>File Name Clash for Files Generated by Clocked Video Functions</td>
<td>Fixed</td>
</tr>
<tr>
<td></td>
<td>The F Falling Edge Line Clocked Video Output Parameter Not Loaded</td>
<td>Fixed</td>
</tr>
<tr>
<td></td>
<td>Layers Supported by Alpha Blending Mixer Incorrect in User Guide</td>
<td>Fixed</td>
</tr>
<tr>
<td></td>
<td>Addendum to the Alpha Blending Mixer Functional Description</td>
<td>Fixed</td>
</tr>
<tr>
<td></td>
<td>Control Register Map for the Clipper Missing From User Guide</td>
<td>Fixed</td>
</tr>
<tr>
<td>15 May 08</td>
<td>SOPC Builder Avalon-ST Adapter Does Not Support Avalon-ST Video</td>
<td>Fixed</td>
</tr>
<tr>
<td>01 Oct 07</td>
<td>Scalar Coefficients Preview Window Cannot be Closed</td>
<td>Fixed</td>
</tr>
<tr>
<td>01 May 07</td>
<td>Precision Must be Set When Using Lanczos Coefficients in Scaler</td>
<td>Fixed</td>
</tr>
<tr>
<td>01 Dec 06</td>
<td>Cyclone II M4K Fails in Alpha Blending Mixer and Gamma Corrector</td>
<td>Fixed</td>
</tr>
</tbody>
</table>
Deinterlacer and Frame Buffer Connected to DDR3 May Not Work Properly

The Deinterlacer and Frame Buffer MegaCore functions may not work properly when connected to a DDR3 High Performance Memory Controller MegaCore function.

In some configurations and/or with specific input resolutions, the Deinterlacer and Frame Buffer MegaCore functions may issue write and read bursts starting at odd addresses. The DDR3 controller uses wrapping bursts for read accesses and, as a consequence, the wrong data may be read back from memory.

Affected Configurations

Systems connecting the Video and Image Processing MegaCore functions to DDR3 SDRAM memory.

Design Impact

This issue may have unpredictable effects. Typically, the output video will be distorted.

Workaround

There is no workaround. However, increasing the number of samples reserved for non-image data packets in memory may solve the issue and realign the starting addresses of the bursts in specific cases.

To realign the starting addresses, the number of words reserved in memory for a non-image packet should be equal to the full wrapping burst, or a multiple of this value. The number of memory words reserved for a non-image packet in memory can be calculated as follows:

1. Determine the number of beats necessary to stream the longest allowed non-image packet through the Avalon Streaming (Avalon-ST) interface. For example, the number of beats to stream an Avalon-ST Video packet of length 10, is 4 when the number of color samples in parallel is 3, 6 when the number of symbols per beat is 2, and 10 when the number of symbols per beat is 1.

   \[
   \text{number_beats} = \text{roundUp}\left(\frac{(\text{max_length} + \text{symbols_per_beat} - 1)}{\text{symbols_per_beat}}\right)
   \]

2. Determine the number of words necessary to store the longest allowed non-image packet:

   \[
   \text{number_words} = \text{roundUp}((\text{number_beats} \times \text{symbols_per_beat} \times \text{bits_per_symbol}) / \text{memory_word_bits})
   \]

By reversing these expressions, you can deduce an adequate value for the maximum number of samples:

\[
\text{max_length} = (\text{wrapping_burst_size} \times \text{roundDown}(\text{memory_word_bits} / (\text{symbols_per_beat} \times \text{bits_per_symbol})) \times \text{symbols_per_beat}) - \text{symbols_per_beat} + 1
\]

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.
**RTL Simulation Reports Errors When Using Verilog HDL**

EDA RTL simulation started from the Quartus II software reports errors in ModelSim® for designs containing Video and Image Processing Suite MegaCore functions when the output files are in Verilog HDL.

**Affected Configurations**
Configurations using Native Link to run a ModelSim simulation from Verilog HDL.

**Design Impact**
An error message reports that the altera library cannot be found.

**Workaround**
Compile the file `db/alt_cusp90_package.vhd` to the altera library. This compilation can be performed by modifying the top-level `.do` script in the `simulation/modelsim` directory.

**Solution Status**
This issue will be fixed in a future version of the Video and Image Processing Suite.

**Incorrect Simulation Models Created for Deinterlacer and Frame Buffer**

Incorrect functional simulation models may be created for the Deinterlacer and Frame Buffer MegaCore functions.

**Affected Configurations**
Configurations that use a different clock domain for the Avalon Memory-Mapped (Avalon-MM) master interfaces.

**Design Impact**
The IP functional simulation models generated using the MegaWizard™ Plug-in Manager may reset in an incorrect state. This issue may also affect simulation models generated with SOPC Builder.

**Workaround**
If possible, release the reset signals for the Avalon-MM interface ports before the reset signal for the MegaCore function. Alternatively, repeat the generation until a valid `.vo` or `.vho` file is produced.

**Solution Status**
This issue will be fixed in a future version of the Video and Image Processing Suite.

**Deinterlacer and Test Pattern Generator May Not Upgrade**

The Deinterlacer and Test Pattern Generator MegaCore functions may not directly upgrade to v9.0 in SOPC Builder.
**Affected Configurations**
Quartus II v8.1 designs containing Deinterlacer or Test Pattern Generator MegaCore functions that were originally created in the Quartus II v8.0 software.

**Design Impact**
SOPC Builder reports an error when it tries to upgrade the MegaCore function if the parameterization has not changed.

**Workaround**
Open the v8.1 version of your design, make a change to the parameterization of any Deinterlacer or Test Pattern Generator MegaCore functions and apply your change. Change back to the original parameterization, then save the SOPC Builder system.

**Solution Status**
This issue will be fixed in a future version of the Video and Image Processing Suite.

**The 2D Median Filter Does Not Support 7×7 Filter Size**
The 2D Median Filter MegaCore function does not support the 7×7 filter size.

**Affected Configurations**
Configurations including the 2D Median Filter MegaCore function.

**Design Impact**
You can select a 7×7 filter size in pre-9.0 versions of the 2D Median Filter MegaCore function but an error message is issued when generating the simulation model.

**Workaround**
There is no workaround. Do not select the 7×7 filter size.

**Solution Status**
The 7×7 filter size is not available in version 9.0 or later of the Video and Image Processing Suite. The documentation will be updated in the next version.

**Misleading Error Message Issued by Color Plane Sequencer**
If you try to enable both ports din1 and dout1 in the MegaWizard interface for the Color Plane Sequencer MegaCore function a misleading error message is issued stating that "dout0 and dout1 cannot both be enabled". The message should state "din1 and dout1 cannot both be enabled".

**Affected Configurations**
Pre-9.0 configurations including the Color Plane Sequencer MegaCore function.

**Design Impact**
None.
Workaround
None needed.

Solution Status
The error message has been updated in v9.0 of the Video and Image Processing Suite.

Changing Target Device After Quartus II Compilation Causes Error
Changing the target device in a family after compilation in the Quartus II software can cause an error with subsequent Quartus II compilations.

Affected Configurations
Any Video and Image Processing Suite MegaCore function when the target device is changed within the same device family.

Design Impact
The generation flow does not correctly recognize the change to the target device. The HDL generation is skipped for subsequent Quartus II compilations, and the following error message is issued when you re-compile:

```
Error (10481): VHDL Use Clause error at *_GN.vhd: design library "altera" does not contain primary unit "alt_cusp81_package"
```

Workaround
Remove the `db` directory from the project directory and re-compile in the Quartus II software.

Solution Status
This issue is fixed in v9.0 of the Video and Image Processing Suite.

Active Picture Line Selection Should be Available for Separate Sync Mode
The Active picture line selection box should be available when On separate wires is selected for Sync signals.

Affected Configurations
This issue affects the Clocked Video Output MegaCore function when sync signals on separate wires are selected.

Design Impact
An incorrect active picture line is selected.

Workaround
Select Embedded in video to enable the selection box, then switch back to On separate wires after specifying the required active picture line. The specified value is used although it is shown dimmed in the selection box.

Solution Status
This issue is fixed in v9.0 of the Video and Image Processing Suite.
v7.2 MegaCore Functions are Not Compatible with v8.x Quartus II

The v7.2 Video and Image Processing Suite MegaCore functions are not compatible with v8.0 or v8.1 of the Quartus II software, SOPC Builder or DSP Builder.

Affected Configurations
All designs including v7.2 Video and Image Processing Suite MegaCore functions.

Design Impact
Errors are issued when you attempt to compile the design.

Workaround
Upgrade the MegaCore functions to v8.0 or v8.1.

Solution Status
This issue will not be fixed. However v8.x MegaCore functions can be used in v9.0 of the Quartus II software.

Packets Sent to VIP Cores Must Have Non-Empty Payload

The packets sent to the Color Space Converter and 2D Median Filter MegaCore functions must have non-empty payload. If a packet is sent with a type but without any further information, the packet processing logic may enter an inconsistent state.

Affected Configurations
Configurations including the Color Space Converter or 2D Median Filter MegaCore functions.

Design Impact
If a packet with an empty payload is received, the MegaCore function may not output correct data until a few non-empty packets have been received.

Workaround
If an empty packet is intended, send one symbol of data with it.

Solution Status
This issue is unlikely to be fixed as there is a simple workaround.

Control Port Behavior Unpredictable for Scaler and Clipper

The run-time control port has unpredictable behavior for the Scaler and Clipper MegaCore functions.

Affected Configurations
Instantiations of the Scaler or Clipper MegaCore functions where the run-time control port is enabled.
Design Impact
Values on the Avalon-MM bus are captured correctly and re-captured after a few cycles. However, the second capture does not respect the chipselect and write signals. This issue may have unpredictable results: for example, write data being corrupted, or writes to one control register affecting other addresses within the slave.

Workaround
A patch is available from Altera customer support.

Solution Status
This issue is fixed in v8.1 of the Video and Image Processing Suite.

Error in Clocked Video Output Constraint File
There is an error in the .sdc file for the Clocked Video Output MegaCore function.

Affected Configurations
Configurations using the Clocked Video Output MegaCore function.

Design Impact
An error message is issued by the TimeQuest Timing Analyzer:
Warning: Ignored assignment: set_false_path -to [get_keepers {*alt_vip_IS2Vid:*|is_line_count_f0[*][*]}]

Workaround
Edit the <install path>\ip\clocked_video_output\lib\alt_vip_cvo.sdc file and change line 71 from:
set_false_path -to [get_keepers {*alt_vip_IS2Vid:*|is_line_count_f0[*][*]}]
to:
set_false_path -to [get_keepers {*alt_vip_IS2Vid:*|is_line_count_f0[*][*]}]

Solution Status
This issue is fixed in v8.1 of the Video and Image Processing Suite.

Simulation Models Not Created For Clocked Video Functions
The simulation check box in SOPC Builder is not triggering generation of the simulation models for the clocked video MegaCore functions.

Affected Configurations
SOPC Builder configurations including the Clocked Video Input or Clocked Video Output MegaCore functions.

Design Impact
No simulation model is available.
**Workaround**

Use the MegaWizard Plug-In Manager to generate the simulation models by performing the following steps:

1. In the Quartus II software, open the MegaWizard Plug-In Manager (from the Tools menu).
2. Click **Edit an existing custom megafunction variation**.
3. Select the `.vhd` file that matches the name of the MegaCore function (as shown in SOPC Builder) and select the **Megafunction name** that corresponds to the MegaCore function (Clocked Video Input v8.0 or Clocked Video Output v8.0).
4. Click **Ok** to display the MegaWizard interface and verify that the parameterization of the user interface is as expected.
5. Click on the **EDA** tab. Select **Generate simulation model**, then click **Finish**.

The simulation model is generated.

**Solution Status**

This issue is fixed in v8.1 of the Video and Image Processing Suite.

**Cannot Connect Adapter in SOPC Builder For Multiple Parallel Planes**

In SOPC Builder, any Video and Image Processing Suite MegaCore function that supports the Avalon-ST Video protocol can connect to any other Video and Image Processing Suite MegaCore function without error.

However, connecting any v8.0 Video and Image Processing Suite component, with more than one color plane in parallel, to an Avalon-ST adapter or user IP component which supports Avalon-ST Video, may cause SOPC Builder to display an error message.

The message states that there is an empty signal associated with the adapter but there is no empty signal associated with the Video and Image Processing Suite MegaCore function:

**Error:** my_alt_vip_<vip core>.dout/<Avalon-ST Adapter>.in: The sink has a empty signal of <n> bits, but the source does not.

**Affected Configurations**

SOPC Builder configurations that connect an Avalon-ST adapter to a Video and Image Processing MegaCore function that is parameterized for more than one color plane in parallel.

**Design Impact**

There are currently no SOPC Builder adapters that support connection between packet-based Avalon-ST components with greater than one symbol per beat and the Video and Image Processing Suite MegaCore functions that support the Avalon-ST Video protocol. Error messages are displayed in the SOPC Builder message window.

However, the Video and Image Processing Suite MegaCore functions do not require the empty signal and the resulting system is valid if the connecting component supports the Avalon-ST Video protocol.
Workaround
Ignore the error message, and generate the system by holding down the Ctrl key while clicking Generate.

Solution Status
This issue is fixed in v8.1 of SOPC Builder and the Video and Image Processing Suite.

Line Buffer Compiler Does Not Generate for Arria GX
The Line Buffer Compiler MegaCore function does not generate for Arria GX devices.

Affected Configurations
Line Buffer Compiler MegaCore function in any parameterization targeting Arria GX devices.

Design Impact
The MegaCore function cannot be generated.

Workaround
None.

Solution Status
This issue is fixed in v8.1 of the Video and Image Processing Suite.

Misleading Warning Message for Color Plane Sequencer
The MegaWizard interface for the Color Plane Sequencer shows the warning message "Data rates of channels on din0 and dout0 are not equal, inefficient use of the pipeline will result" at all times and for all parameterizations. This warning should not be shown for parameterizations that use the processing pipeline at full efficiency.

Affected Configurations
All configuration using the Color Plane Sequencer MegaCore function.

Design Impact
None.

Workaround
The message can be ignored. However, note that when converting from channels in parallel to channels in sequence or vice versa, the data rate of the streaming connection will be slowed to the data rate of the slowest input or output.

Solution Status
This issue is fixed in v8.1 of the Video and Image Processing Suite.
Color Plane Sequencer Does Not Report GUI Messages

The Color Plane Sequencer MegaCore function does not report information messages regarding the GUI behavior.

Affected Configurations

Configurations including the Color Plane Sequencer MegaCore function.

Design Impact

The MegaWizard interface has some controls which cannot enter an invalid state. When a value is entered that would specify an invalid state, the GUI reverts to the previous parameter setting without issuing an information message explaining why it has reverted its settings.

Workaround

Take extra care to ensure that your parameter values are valid and have been accepted.

Solution Status

This issue is fixed in v8.1 of the Video and Image Processing Suite.

The .hex Files for Simulation in SOPC Builder Systems Must be Moved

When simulation files are generated in SOPC Builder, the .hex files are generated in a different location to the .vho/.vo files. These files must be moved to the same directory as the .vho/.vo files.

Affected Configurations

This issue affects all Video and Image Processing Suite MegaCore functions that generate .hex files when the simulation models are generated through SOPC Builder.

Design Impact

If the .hex files are not in the same directory as the .vho/.vo file which uses them, the simulator tool will not be able to find the .hex files when a simulation is run and issues an error. For example, ModelSim reports an error of the form:

```
# ** Error: (vsim-7) Failed to open VHDL file
"alt_vip_scl_gny7hwrxns_v_coeffs0_reg_file_contents.hex" in r mode.
# No such file or directory.
```

Workaround

After SOPC Builder has reported that system generation is complete, the .hex files contained in `<project directory>\db\sopc_sim\db` should be copied to the project directory.

Solution Status

This issue is fixed in v8.1 of the Video and Image Processing Suite.
Deinterlacer Fails to Generate in Some Configurations

Some configurations of the Deinterlacer MegaCore function may fail to compile in the Quartus II software or fail to generate simulation models.

Affected Configurations

This issue affects a very limited number of configurations using double or triple buffering when buffering more than one non-image data packet per field.

Design Impact

The following error messages are issued during analysis and synthesis:

Error: IP Generator Error: Can't synthesise function ker_reader (Can't synthesise operation ASSIGN(current_packet_id, VCALL(ALT_FIFO::read; FIELD(this, packets_write_to_read))))

Error: IP Generator Error: Errors occurred converting parse tree to CDFG

Workaround

A patch is available from Altera customer support.

Solution Status

This issue is fixed in v8.0 SP1 of the Video and Image Processing Suite.

Color Plane Sequencer Shows Parallel Bit Ranges in Reverse Order

The MegaWizard interface for the Color Plane Sequencer MegaCore function uses tables to represent the color pattern used by video data packets. The tables label the bit ranges used for color planes in parallel. This labeling is incorrect; the bit range label for the most significant bits should be at the bottom of the tables, and the bit range label for the least significant bits should be at the top of the tables.

Affected Configurations

Configurations including the Color Plane Sequencer MegaCore function.

Design Impact

The bit ranges may be entered in the wrong order.

Workaround

Ignore the bit range labels. The color planes which use the most significant bits of the interface are on the bottom of the tables, and the color planes that use the least significant bits are on the top of the tables.

Solution Status

This issue is fixed in v8.0 SP1 of the Video and Image Processing Suite.
Clipper Fails to Send EOP When Active Region is Bottom Right

The Clipper MegaCore function fails to send an endofpacket signal when the active region touches the bottom-right corner.

Affected Configurations
Clipper MegaCore function in Offsets mode where the bottom offset and right offset are 0, or in Rectangle mode where top offset + height = input height and left offset + width = input width.

Design Impact
The control packet from the next frame is included at the end of the image data in the current frame, then endofpacket is sent late.

Workaround
None.

Solution Status
This issue is fixed in v8.0 SP1 of the Video and Image Processing Suite.

File Name Clash for Files Generated by Clocked Video Functions

The Clocked Video Input and Clocked Video Output MegaCore functions generate database files sync.v and fifo.v when Verilog HDL is selected. There may be file name clashes if there are user files with the same names.

Affected Configurations
Verilog HDL configurations including the Clocked Video Input or Clocked Video Output MegaCore functions.

Design Impact
Compilation errors when the design is compiled in the Quartus II software.

Workaround
Avoid using sync.v or fifo.v for user-specified filenames in a design that includes the Clocked Video Input and Clocked Video Output MegaCore functions.

Solution Status
This issue is fixed in v8.0 SP1 of the Video and Image Processing Suite.

The F Falling Edge Line Clocked Video Output Parameter Not Loaded

The F falling edge line parameter for the Clocked Video Output MegaCore function is not used for preset loading.

Affected Configurations
Any configuration including the Clocked Video Output MegaCore function.
**Design Impact**
The preset interlaced parameter sets for 1080i60, NTSC and PAL are incorrect.

**Workaround**
Set a value for the F falling edge line parameter, save the variation and reload. The parameters are then loaded correctly.

**Solution Status**
This issue is fixed in v8.0 SP1 of the Video and Image Processing Suite.

**Layers Supported by Alpha Blending Mixer Incorrect in User Guide**
The Alpha Blending Mixer is restricted to a maximum of 12 layers not 16 as specified in the v8.0 user guide.

**Solution Status**
This issue is fixed in the *Video and Image Processing Suite User Guide* for v8.0 SP1.

**Addendum to the Alpha Blending Mixer Functional Description**
The following text was missing from the functional description of the Alpha Blending Mixer in the v8.0 user guide:

When *Alpha blending* is turned on, the Avalon-ST input ports for the alpha channels expect a video stream compliant with the Avalon-ST Video protocol. Alpha frames contain a single color plane and are transmitted in video data packets. The first value in each packet, transmitted while the startofpacket signal is high, contains the packet type identifier 0. This condition holds true even when the width of the alpha channels data ports is less than 4 bits wide. The last alpha value for the bottom-right pixel is transmitted while the endofpacket signal is high.

It is not necessary to send control packets to the ports of the alpha channels. The width and height of each alpha layer are assumed to match with the dimensions of the corresponding foreground layer although the Alpha Blending Mixer MegaCore function recovers gracefully in case of a mismatch. All non-image data packets (control packets included) are ignored and discarded just before the processing of a frame starts.

**Solution Status**
This issue is fixed in the *Video and Image Processing Suite User Guide* for v8.0 SP1.

**Control Register Map for the Clipper Missing From User Guide**
The control register map for the Clipper MegaCore function was omitted from the v8.0 user guide.

Table 26–3 on page 26–15 describes the Clipper control register map.

The control data is read once at the start of each frame and is buffered inside the MegaCore function, so the registers may be safely updated during the processing of a frame.
Chapter 26: Video and Image Processing Suite 26–15

Errata

© 1 July 2009 Altera Corporation Library Version 9.0 MegaCore IP Library Release Notes and Errata

Table 26–3. Clipper Control Register Map

<table>
<thead>
<tr>
<th>Address</th>
<th>Register</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Control</td>
<td>The zeroth bit of this register is the Go bit, all other bits are unused. Setting this bit to 0 causes the Clipper MegaCore function to stop the next time control information is read. Refer to “Avalon-MM Slave Interfaces” on page 4–17 of the Video and Image Processing Suite User Guide for full details.</td>
</tr>
<tr>
<td>1</td>
<td>Status</td>
<td>The zeroth bit of this register is the Status bit, all other bits are unused. The Clipper MegaCore function sets this address to 0 between frames. It is set to 1 while the MegaCore function is processing data and cannot be stopped. Refer to “Avalon-MM Slave Interfaces” on page 4–17 of the Video and Image Processing Suite User Guide for full details.</td>
</tr>
<tr>
<td>2</td>
<td>Left Offset</td>
<td>The left offset, in pixels, of the clipping window/rectangle. (Note 1)</td>
</tr>
<tr>
<td>3</td>
<td>Right Offset</td>
<td>In clipping window mode, the right offset of the window. In clipping rectangle mode, the width of the rectangle. (Note 1)</td>
</tr>
<tr>
<td>4</td>
<td>Top Offset</td>
<td>The top offset, in pixels, of the clipping window/rectangle. (Note 2)</td>
</tr>
<tr>
<td>5</td>
<td>Bottom Offset</td>
<td>In clipping window mode, the bottom offset of the window. In clipping rectangle mode, the height of the rectangle. (Note 2)</td>
</tr>
</tbody>
</table>

Notes to Table 26–3:
(1) The left and right offset values must be less than or equal to the input image width.
(2) The top and bottom offset values must be less than or equal to the input image height.

Solution Status
This issue is fixed in the Video and Image Processing Suite User Guide for v8.0 SP1.

SOPC Builder Avalon-ST Adapter Does Not Support Avalon-ST Video
In SOPC Builder, the Avalon-ST data adapter does not support the Avalon-ST Video protocol. No error message is currently displayed when connecting the components.

Affected Configurations
SOPC Builder configurations that connect an Avalon-ST adapter to a Video and Image Processing MegaCore function.

Design Impact
Connecting any of the Video and Image Processing Suite MegaCore functions to an Avalon-ST data adapter results in a generated system in which the Avalon-ST video protocol is corrupted.

Workaround
To connect Video and Image Processing MegaCore functions which have a different number of planes in parallel, use the Color Plane Sequencer. For example: to convert between 3 colors in parallel (3 symbols per beat) and 3 colors in sequence (1 symbol per beat).

Solution Status
It will not be possible to connect unsupported Avalon-ST adapters in a future version of SOPC Builder and the Video and Image Processing Suite.
Scalar Coefficients Preview Window Cannot be Closed

The Scalar Coefficients Preview window cannot be closed when it is used in SOPC Builder.

Affected Configurations
This issue affects the Scaler MegaCore Function when it is parameterized in the SOPC Builder flow.

Design Impact
This issue does not prevent you from parameterizing the Scalar and therefore has no design impact.

Workaround
The Coefficient Preview window will close when you close the main Scalar parameterization interface.

Solution Status
This issue will be fixed in a future version of the Video and Image Processing Suite.

Precision Must be Set When Using Lanczos Coefficients in Scaler

When configuring the Scaler MegaCore function, you must choose the correct coefficient precision when using Lanczos coefficients.

Affected Configurations
This issue affects configurations of the Scaler MegaCore function using the polyphase algorithm with Lanczos coefficients.

Design Impact
The MegaCore function fails to generate.

Workaround
If you select polyphase mode with Lanczos coefficients, you must set the coefficient precision to be signed with one integer bit. Fraction bits can be set within the full range available in the MegaWizard interface.

Solution Status
The coefficient precision restriction will be enforced in future versions of the Video and Image Processing Suite.

Cyclone II M4K Fails in Alpha Blending Mixer and Gamma Corrector

M4K block write operations may fail for Cyclone II devices with the Alpha Blending Mixer and Gamma Corrector MegaCore functions.

Affected Configurations
This issue affects configurations using Cyclone II devices and the Alpha Blending Mixer or Gamma Corrector MegaCore function.
Design Impact

The following error message is issued:

Error: M4K memory block WYSIWYG primitive
"vhdl_gam:vhdl_gam_inst|TTA_X_smem_av:gamma_lut|altsyncram:\ds1:altsyncram_component|altsyncram_rvh1:auto_generated|ram_block1a0" utilizes the dual-port dual-clock mode. However, this mode is not supported in Cyclone II device family in this version of Quartus II software. Please refer to the Cyclone II FPGA Family Errata Sheet for more information on this feature.

Workaround

If you are targeting any affected revision (Rev a or b of the 2c35 or Rev a of any other Cyclone II part), set the CYCLONEII_SAFE_WRITE variable to RESTRUCTURE. This setting causes the Quartus II software to fix the issue at a cost in M4Ks and F\textsubscript{max}. If you are using a newer revision device, set the CYCLONEII_SAFE_WRITE variable to VERIFIED_SAFE which turns off the error message.

Solution Status

This issue has been fixed for the latest silicon devices but remains an issue if you are using the earlier silicon.

Refer to the Cyclone II FPGA Family Errata Sheet for more information about this issue.
Revision History

Table 27–1 shows the revision history for the Viterbi Compiler.

For more information about the new features, refer to the Viterbi Compiler User Guide.

Table 27–1. Viterbi Compiler Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.0 SP1</td>
<td>May 2009</td>
<td>Preliminary support for HardCopy III and HardCopy IV E devices.</td>
</tr>
<tr>
<td>9.0</td>
<td>March 2009</td>
<td>Preliminary support for Arria® II GX devices.</td>
</tr>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>Full support for Stratix III devices.</td>
</tr>
</tbody>
</table>
| 8.0     | May 2008 | • Full support for Cyclone III devices  
|         |            | • Preliminary support for Stratix IV devices                  |

Errata

Table 27–2 shows the issues that affect the Viterbi Compiler v9.0, 8.1, and 8.0.

Not all issues affect all versions of the Viterbi Compiler.

Table 27–2. Viterbi Compiler Errata

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Jul 09</td>
<td>Trellis Mode Fails</td>
<td>—</td>
</tr>
<tr>
<td>15 Mar 09</td>
<td>Testbench ber_clear Signal is Not Connected</td>
<td>✔ — — Fixed</td>
</tr>
<tr>
<td></td>
<td>Gate-Level Simulation Fails</td>
<td>✔ — —</td>
</tr>
<tr>
<td>01 Nov 08</td>
<td>Display Symbol Button in IP Toolbench is Missing</td>
<td>✔ ✔ —</td>
</tr>
<tr>
<td>15 May 08</td>
<td>IP Functional Simulation Model Fails</td>
<td>✔ ✔ ✔</td>
</tr>
<tr>
<td>01 Oct 07</td>
<td>File Summary Does Not List All Generated Files</td>
<td>✔ ✔ ✔</td>
</tr>
</tbody>
</table>

Trellis Mode Fails

The trellis mode does not work correctly in the parallel continuous architecture.

Affected Configurations

This issue affects the parallel architecture, continuous optimization.

Design Impact

You cannot use the trellis mode.
Workaround
There is no workaround. Contact Altera, if you need this issue fixed.

Solution Status
This issue is fixed in version 8.0 of the Viterbi Compiler.

Testbench ber_clear Signal is Not Connected
The ber_clear signal in the generated testbench is not connected correctly.

Affected Configurations
This issue affects all designs.

Design Impact
There is no design impact.

Workaround
This issue has no workaround.

Solution Status
This issue will be fixed in a future version of the Viterbi Compiler.

Gate-Level Simulation Fails
The Viterbi Compiler does not support gate-level simulations.

Affected Configurations
This issue affects all designs.

Design Impact
There is no design impact.

Workaround
This issue has no workaround.

Solution Status
This issue will be fixed in a future version of the Viterbi Compiler.

Display Symbol Button in IP Toolbench is Missing
The Display Symbol button in IP Toolbench does not appear, even though the screenshot in the user guide implies it should appear.

Affected Configurations
This issue affects all designs.
Design Impact
There is no design impact.

Workaround
This issue has no workaround.

Solution Status
This issue will be fixed in a future version of the Viterbi Compiler.

IP Functional Simulation Model Fails
The IP functional simulation model for your Verilog HDL design may fail.

Affected Configurations
This issue affects all Verilog HDL designs.

Design Impact
There is no design impact.

Workaround
Create a VHDL variation and use the VHDL IP functional simulation model.

Solution Status
This issue will be fixed in a future version of the Viterbi Compiler.

File Summary Does Not List All Generated Files
The file summary on the IP Toolbench Generate window does not always list all the generated files.

Affected Configurations
This issue affects all configurations.

Design Impact
There is no design impact.

Workaround
In the Parameterize window, when you finish parameterizing your variation, do not click Finish, just go to IP Toolbench and click Generate.

Solution Status
This issue will be fixed in a future version of the Viterbi Compiler.
How to Contact Altera

For the most up-to-date information about Altera® products, see the following table.

<table>
<thead>
<tr>
<th>Contact</th>
<th>Contact Method</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technical support</td>
<td>Website</td>
<td><a href="http://www.altera.com/support">www.altera.com/support</a></td>
</tr>
<tr>
<td>Technical training</td>
<td>Website</td>
<td><a href="http://www.altera.com/training">www.altera.com/training</a></td>
</tr>
<tr>
<td>Altera literature services</td>
<td>Email</td>
<td><a href="mailto:custrain@altera.com">custrain@altera.com</a></td>
</tr>
<tr>
<td>Non-technical support (General)</td>
<td>Email</td>
<td><a href="mailto:literature@altera.com">literature@altera.com</a></td>
</tr>
<tr>
<td>(Software Licensing)</td>
<td>Email</td>
<td><a href="mailto:nacomp@altera.com">nacomp@altera.com</a></td>
</tr>
<tr>
<td></td>
<td>Email</td>
<td><a href="mailto:authorization@altera.com">authorization@altera.com</a></td>
</tr>
</tbody>
</table>

**Note:**
(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions that this document uses.

<table>
<thead>
<tr>
<th>Visual Cue</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Bold Type with Initial Capital Letters</strong></td>
<td>Indicates command names, dialog box titles, dialog box options, and other GUI labels. For example, <em>Save As</em> dialog box. For GUI elements, capitalization matches the GUI.</td>
</tr>
<tr>
<td><strong>bold type</strong></td>
<td>Indicates directory names, project names, disk drive names, file names, file name extensions, dialog box options, software utility names, and other GUI labels. For example, \qdesigns\ directory, d: drive, and chiptrip.gdf file.</td>
</tr>
<tr>
<td><strong>Italic Type with Initial Capital Letters</strong></td>
<td>Indicates document titles. For example, <em>AN 519: Stratix IV Design Guidelines.</em></td>
</tr>
<tr>
<td><strong>Italic type</strong></td>
<td>Indicates variables. For example, n + 1.</td>
</tr>
<tr>
<td></td>
<td>Variable names are enclosed in angle brackets (&lt; &gt;). For example, &lt;file name&gt; and &lt;project name&gt;.pof file.</td>
</tr>
<tr>
<td><strong>Initial Capital Letters</strong></td>
<td>Indicates keyboard keys and menu names. For example, Delete key and the Options menu.</td>
</tr>
<tr>
<td><strong>“Subheading Title”</strong></td>
<td>Quotation marks indicate references to sections within a document and titles of Quartus II Help topics. For example, “Typographic Conventions.”</td>
</tr>
<tr>
<td><strong>Courier type</strong></td>
<td>Indicates signal, port, register, bit, block, and primitive names. For example, data1, tdi, and input. Active-low signals are denoted by suffix n. For example, resetn.</td>
</tr>
<tr>
<td></td>
<td>Indicates command line commands and anything that must be typed exactly as it appears. For example, c:\qdesigns\tutorial\chiptrip.gdf.</td>
</tr>
<tr>
<td></td>
<td>Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword SUBDESIGN), and logic function names (for example, TRI).</td>
</tr>
<tr>
<td>Visual Cue</td>
<td>Meaning</td>
</tr>
<tr>
<td>-----------------------------------</td>
<td>-------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>1., 2., 3., and a., b., c., and so on.</td>
<td>Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.</td>
</tr>
<tr>
<td>■ ■</td>
<td>Bullets indicate a list of items when the sequence of the items is not important.</td>
</tr>
<tr>
<td>1.</td>
<td>The hand points to information that requires special attention.</td>
</tr>
<tr>
<td><img src="caution.png" alt="Caution" /></td>
<td>A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.</td>
</tr>
<tr>
<td><img src="warning.png" alt="Warning" /></td>
<td>A warning calls attention to a condition or possible situation that can cause you injury.</td>
</tr>
<tr>
<td>→</td>
<td>The angled arrow instructs you to press Enter.</td>
</tr>
<tr>
<td><img src="feet.png" alt="Feet" /></td>
<td>The feet direct you to more information about a particular topic.</td>
</tr>
</tbody>
</table>