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About These Release Notes

These release notes cover versions 7.2 through 8.1 of the Altera® MegaCore® IP Library. Each chapter in these release notes describes the revision history and errata for each product in the MegaCore IP Library.

From v7.2 onwards, this document replaces all individual IP product release notes and errata sheets that Altera previously published.

Errata are functional defects or errors, which may cause the product to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

The product errata tables use the following indicators:
- A checkmark “✓” indicates an issue is applicable to that version
- “Fixed” indicates the issue was fixed in that version
- A dash “—” indicates the issue is not applicable to that version

For the most up-to-date errata for this release, refer to the latest version of the MegaCore IP Library Release Notes on the Altera website.

For more information on Quartus® II issues, refer to the Quartus II Software Release Notes.

System Requirements

The MegaCore IP Library is distributed with the Quartus® II software and downloadable from the Altera® website, www.altera.com.

For system requirements and installation instructions, refer to Quartus II Installation & Licensing for Windows or Quartus II Installation & Licensing for Linux Workstations.

Update Status

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<td>1 November 2008</td>
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<td>3. CIC</td>
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<td>8. FFT</td>
<td>1 November 2008</td>
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<td>9. FIR Compiler</td>
<td>1 November 2008</td>
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<td>13. PCI Compiler</td>
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<td>15. POS-PHY Level 2 and 3 Compiler</td>
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<td>27. Viterbi Compiler</td>
<td>1 November 2008</td>
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</tbody>
</table>
Revision History

Table 1–1 shows the revision history for the 8B10B Encoder/Decoder MegaCore® function.

For more information on the new features, refer to the 8B10B Encoder/Decoder MegaCore Function User Guide.

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
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<tbody>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>Preliminary support for Stratix® IV device family.</td>
</tr>
<tr>
<td>7.2</td>
<td>October 2007</td>
<td>Maintenance release.</td>
</tr>
</tbody>
</table>

Errata

No known issues in v8.1, 8.0, and 7.2.
Revision History

Table 2–1 shows the revision history for the ASI MegaCore® function.

For more information on the new features, refer to the ASI MegaCore Function User Guide.

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>■ Maintenance release.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>■ Preliminary support for Stratix® IV devices.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Added GX transceiver based core for Arria® GX devices.</td>
</tr>
<tr>
<td>7.2</td>
<td>October 2007</td>
<td>■ Support for Arria GX devices.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Support for SOPC Builder.</td>
</tr>
</tbody>
</table>

Errata

Table 2–2 shows the issues that affect the ASI MegaCore function v8.1, 8.0, and 7.2.

Not all issues affect all versions of the ASI MegaCore function.

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 May 08</td>
<td>NativeLink Simulation Fails</td>
<td>8.1 Fixed</td>
</tr>
<tr>
<td></td>
<td>VCS Simulator</td>
<td>8.0 Fixed</td>
</tr>
<tr>
<td>01 Dec 06</td>
<td>NativeLink Does Not Support Gate-Level Simulation</td>
<td>7.2 Fixed</td>
</tr>
</tbody>
</table>

NativeLink Simulation Fails

The NativeLink example simulation fails because it cannot find the memory initialization files (.mif).

Affected Configurations
This issue only affects example simulations.

Design Impact
There is no design impact.

Workaround
Regenerate both the ASI receiver and ASI transmitter MegaCore functions.
1. Double click on the `asi_rx` instance in the project navigator pane. This action opens up the `asi_rx` instance MegaWizard® Plug-In Manager.
2. Click Finish, then Exit.
3. On the Tools menu click MegaWizard Plug In Manager.
4. Select Edit an existing megafunction.
5. Browse to `\72\ip\asi\testbench\asi_mc_build` and select `asi_tx_sim.v` and click Next.
6. In the MegaWizard Plug In Manager, click the Finish button, then Exit.
   The .vo files for both cores have now regenerated.
   You can now proceed with NativeLink simulation as described in the user guide.

**Solution Status**
This issue is fixed in version 8.0 of the ASI MegaCore Function.

**VCS Simulator**

The ASI MegaCore function may not work with the VCS simulator.

**Affected Configurations**
This issue affects all configurations.

**Design Impact**
If you simulate your design in the VCS simulator, it may not work.

**Workaround**
Use a different simulator.

**Solution Status**
This issue is fixed in version 8.0 of the ASI MegaCore function.

**NativeLink Does Not Support Gate-Level Simulation**

When using the NativeLink simulation example, the gate-level simulation design fails.

**Affected Configurations**
This issue affects all simulators supported by NativeLink.

**Design Impact**
This issue only affects simulation and does not affect the design compilation.

**Workaround**
Perform an RTL simulation of the NativeLink simulation example.
Solution Status

This issue will be fixed in a future version of the ASI MegaCore function.
3. CIC

Revision History

Table 3–1 shows the revision history for the CIC MegaCore® function.

For information on the new features, refer to the CIC MegaCore Function User Guide.

Table 3–1. CIC MegaCore Function Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>■ Full support for Stratix® III.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Withdrawn support for UNIX.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>■ Full support for Cyclone® III.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Preliminary support for Stratix IV.</td>
</tr>
<tr>
<td>7.2</td>
<td>October 2007</td>
<td>■ Full support for Arria® GX devices.</td>
</tr>
</tbody>
</table>

Errata

Table 3–2 shows the issues that affect the CIC MegaCore function v8.1, v8.0, and v7.2.

Not all issues affect all versions of the CIC MegaCore function.

Table 3–2. CIC MegaCore Function Errata

<table>
<thead>
<tr>
<th>Added or Updated</th>
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<tbody>
<tr>
<td>01 Jul 07</td>
<td>Synthesis Error When Number of Stages is Greater than 10</td>
<td>8.1 8.0 7.2</td>
</tr>
</tbody>
</table>

Synthesis Error When Number of Stages is Greater than 10

If the number of stages is more than 10, a signal name used in the MISO architecture can conflict.

Affected Configurations

MISO architectures with 10 stages or more.

Design Impact

An incorrect variation file is generated which cannot be synthesized.

The following error message is issued:

VHDL error at xxx_cic.vhd(115): name "D_fsR10" cannot be used because it is already used for a previously declared item

Workaround

A patch is available from Altera customer support.
Solution Status
This issue is fixed in version 7.2 of the CIC MegaCore function.
Revision History

Table 4–1 shows the revision history for the CRC Compiler.

For more information on the new features, refer to the CRC Compiler User Guide.

Table 4–1. CRC Compiler Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>Preliminary support for Stratix® IV device family.</td>
</tr>
</tbody>
</table>
| 7.2     | October 2007    | • Preliminary support for Stratix III device family.  
|         |                 | • Multi-channel support; up to 100 CRC channels.   |
|         |                 | • Enhanced control of input bits and symbols swapping.  |
|         |                 | • Support for partial first word.                 |

Errata

Table 4–2 shows the issues that affect the CRC Compiler v8.1, 8.0, and 7.2.

Not all issues affect all versions of the CRC Compiler.

Table 4–2. CRC Compiler Errata

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Oct 07</td>
<td>Incorrect crcchannel Value in Multi-Channel Mode</td>
<td>8.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>8.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>7.2</td>
</tr>
<tr>
<td>01 Dec 06</td>
<td>Testbench Directory Generated When You Create a Simulation Model</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>✔</td>
</tr>
<tr>
<td></td>
<td></td>
<td>✔</td>
</tr>
<tr>
<td></td>
<td></td>
<td>✔</td>
</tr>
</tbody>
</table>

Incorrect crcchannel Value in Multi-Channel Mode

When CRC channels are switched continuously at random points within a packet transmission, the signal crcchannel doesn’t reflect the correct channel for the output signals checksum and crcbad.

Affected Configuration

Configurations with multi-channel CRCs.

Workaround

You have the following options to avoid this issue:

• Limit each packet transmission to only a single channel.
Keep track of the channels in your design, if you need to switch channels within a packet transmission.

**Solution Status**
This issue is fixed in version 8.0 of the CRC Compiler.

**Testbench Directory Generated When You Create a Simulation Model**
When you create a simulation model, the CRC compiler automatically creates a testbench directory in the project directory for you. If you follow the Running the Testbench Example steps in the CRC Compiler User Guide to create the generator and checker files, another testbench directory is created as a subdirectory of the initial testbench directory resulting in the following directory structure:

```
c:\altera\projects\crc_project\testbench\testbench
```
when the initial directory is
```
c:\altera\projects\crc_project\testbench
```

**Affected Configuration**
All CRC MegaCore function variations are affected.

**Design Impact**
There is no design impact for this issue.

**Workaround**
The testbench subdirectory (testbench\testbench) of the initial
c:\altera\projects\crc_project\testbench directory may be deleted.

**Solution Status**
Currently, there are no plans to change this behavior.
Revision History

Table 5–1 shows the revision history for the DDR and DDR2 SDRAM Controller Compiler.

For more information on the new features, refer to the DDR and DDR2 SDRAM Controller Compiler User Guide.

Table 5–1. DDR and DDR2 SDRAM Controller Compiler Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>8.0 SP1</td>
<td>July 2008</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>7.2</td>
<td>October 2007</td>
<td>Maintenance release.</td>
</tr>
</tbody>
</table>

Errata

Table 5–2 shows the issues that affect the DDR and DDR2 SDRAM Controller Compiler v8.1, 8.0 and 7.2.

Not all issues affect all versions of the DDR and DDR2 SDRAM Controller Compiler.

Table 5–2. DDR and DDR2 SDRAM Controller Compiler Errata

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Nov 08</td>
<td>VHDL Package Declaration Error When Upgrading the MegaCore Function</td>
<td>Fixed</td>
</tr>
<tr>
<td>15 Jul 08</td>
<td>Read Requests Are Sometimes Discarded</td>
<td>—</td>
</tr>
<tr>
<td>15 May 08</td>
<td>“Cannot Find Source Node” Error During Post-Compile Timing Analysis</td>
<td>—</td>
</tr>
<tr>
<td>15 Oct 07</td>
<td>Error: Can’t Find the Clock Output Pins. Stop.</td>
<td>—</td>
</tr>
<tr>
<td>01 Jul 07</td>
<td>ODT Launches Off System Clock</td>
<td>—</td>
</tr>
<tr>
<td>01 Jun 06</td>
<td>Simulating with the NCSim Software</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>Simulating with the VCS Simulator</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>Error Message When Recompiling a Project</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>Pin Planner HDL Syntax Error</td>
<td>—</td>
</tr>
</tbody>
</table>

**VHDL Package Declaration Error When Upgrading the MegaCore Function**

If you upgrade an existing custom variation of the MegaCore® function, the following error may occur:
Error (10624): VHDL Package Declaration error at auk_ddr_tb_functions.vhd(23): package "auk_ddr_tb_functions" already exists in the work library

IP Toolbench adds files to your Quartus® II project when you generate your custom variation. When you upgrade your MegaCore function, the same files from the previous and current versions are present in the same Quartus II project, which causes a VHDL error.

**Affected Configurations**
This issue affects all designs that were created in a previous version of the MegaCore function.

**Workaround**
From your Quartus II project, remove the Device Design Files that were added by the earlier version of the MegaCore function. These files can be identified by the files’ directory names.

**Design Impact**
You cannot compile your Quartus II project until you remove the duplicate files.

**Solution Status**
This issue is fixed in v8.1 of the DDR and DDR2 SDRAM Controller Compiler.

**Read Requests Are Sometimes Discarded**
Some read requests on the local interface may be discarded and not sent to the memory, particularly the first read to a bank that has not yet been activated.

**Affected Configurations**
All configurations are affected.

**Design Impact**
Your design may fail to operate correctly.

**Workaround**
Regenerate your controller instance in the latest version of the DDR and DDR2 SDRAM Controller Compiler.

**Solution Status**
This issue is fixed in v8.0 SP1 of the DDR and DDR2 SDRAM Controller Compiler.

**“Cannot Find Source Node” Error During Post-Compile Timing Analysis**
The post-compile timing script may report the following error:

```
Cannot find source node
'<<variation>:_ddr_sdram[/.../<<variation>_auk_ddr_datapath:ddr_io<<variation>_auk_ddr_dqs_group\g_datapath:0:g_ddr_io|dq_enable_reset[0]'``
**Affected Configurations**

Some Stratix® II and Stratix II GX designs.

**Design Impact**

You cannot successfully complete the post compile timing analysis.

**Workaround**

Add an "Auto Shift Register Replacement" constraint to the following node in your Quartus II project using the Assignment editor, and set the value to Off.

<variation>:<variation>_ddr_sdram|<variation>_auk_ddr_sdram:<variation>_auk_ddr_sdram_inst|<variation>_auk_ddr_datapath:ddr_io

**Solution Status**

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controller Compiler.

---

**Error: Can't Find the Clock Output Pins. Stop.**

The postcompile timing script reports the following error:

'Couldn't find the clock output pins. Stop.'

**Affected Configurations**

This issue affects designs using the DDR SDRAM controller, when the PLL counters have been reordered or the clocks for the DDR SDRAM interface are not on global clocks. This issue may occur automatically in the fitter if there is pressure on global clock resources.

**Design Impact**

The design fails.

**Workaround**

Make the following two assignments:

```
ddr_pll_stratixii:g_stratixpll_ddr_pll_inst Preserve PLL Counter Order
ddr_pll_stratixii:g_stratixpll_ddr_pll_inst|altpll:altpll_component|_clk3* Global Signal Global Clock
```

Replace the file names of the PLL with those in your DDR SDRAM controller design.

**Solution Status**

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controller Compiler.

---

**ODT Launches Off System Clock**

In designs with a separate address and command clock, the ODT output launches from the system clock not from this address and command clock.
**Affected Configurations**
This issue affects the following configurations:

- DDR2 SDRAM controller (not DDR SDRAM)
- ODT is turned on
- CAS latency is set to three
- The design uses a separate address and command clock and not the default system clock

**Design Impact**
There is no design impact.

**Workaround**
Use a CAS latency of four, which means one extra cycle of read latency, or use the DDR2 SDRAM High-Performance controller, which uses the ALTMEMPHY megafunction to transfer all the address and command outputs to the correct clock.

**Solution Status**
This issue will never be fixed.

**Simulating with the NCSim Software**
The DDR or DDR2 SDRAM Controller MegaCore functions do not fully support the NCSim software.

**Affected Configurations**
This issue affects all configurations.

**Design Impact**
The design does not simulate.

**Workaround**
Set the `-relax` switch for all calls to the VHDL analyzer.

**Solution Status**
This issue will never be fixed.

**Simulating with the VCS Simulator**
The DDR or DDR2 SDRAM Controller MegaCore functions do not fully support the VCS simulator.

**Affected Configurations**
This issue affects all configurations.

**Design Impact**
The design does not simulate.
Workaround

The following workarounds exist.

VHDL

Change the following code.
- In file `<variation name>_example_driver.vhd`, change all `when` statements between lines 333 and 503 from `when std_logic_vector’("<bit_pattern>")` to `when "<bit_pattern>"`.
- In file `testbench\<example name>_tb`, change line 191 from `signal zero_one(gMEM_BANK_BITS -1 downto 0) := (0 => '1', others => '0')` to `signal zero_one(gMEM_BANK_BITS -1 downto 0) := ('1', others=> '0')`.

Verilog HDL

No changes are necessary. Calls to the Verilog analyzer sets the +v2k switch to enable Verilog 2000 constructs.

Solution Status

This issue will never be fixed.

Error Message When Recompiling a Project

If you move the directory containing your Quartus II project, or rename your Quartus II project and recompile it without regenerating the DDR or DDR2 SDRAM Controller, you may receive the following error:

Error: DDR timing cannot be verified until project has been successfully compiled.

This error indicates that some of the settings files contain references to the previous location or project name and the verify timing script is unable to find the current project.

Affected Configurations

This issue affects all configurations.

Design Impact

The timing script does not verify your design.

Workaround

Regenerate your controller in IP Toolbench and recompile the project. The timing analysis script now completes correctly.

Solution Status

This issue will never be fixed.
Pin Planner HDL Syntax Error

There is an HDL syntax error in Pin Planner-generated top-level design files that contain a DDR or DDR2 SDRAM Controller variation.

Affected Configurations

Pin Planner-generated top-level design files that use a design that contains a DDR or DDR2 SDRAM Controller variation.

Design Impact

If you import the DDR or DDR2 SDRAM Controller Pin Planner file into Pin Planner and then generate a top-level design file for your design, it contains an HDL syntax error and does not compile in the Quartus II software. You cannot use this top-level design file for IO Assignment Analysis.

Workaround

Use the IP Toolbench top-level example design and automatically assigned constraints to verify your pin and IO assignments.

Solution Status

This issue will never be fixed.
6. DDR and DDR2 SDRAM High-Performance Controller

Revision History

Table 6–1 shows the revision history for the DDR and DDR2 SDRAM High-Performance Controller MegaCore® function.

For more information on the new features, refer to the DDR and DDR2 SDRAM High-Performance Controller MegaCore Function User Guide.

Table 6–1. DDR and DDR2 SDRAM High-Performance Controller MegaCore Function Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>■ Reduced controller latency and improved efficiency.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Improved example top-level design.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Support for multiple synchronous controllers in an SOPC Builder-generated design.</td>
</tr>
<tr>
<td>8.0 SP1</td>
<td>July 2008</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>■ Preliminary support Stratix® IV devices.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Optional support for self-refresh and power-down commands.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Optional support for auto-precharge read and auto-precharge write commands.</td>
</tr>
</tbody>
</table>

Errata

Table 6–2 shows the issues that affect the DDR and DDR2 SDRAM Controller High-Performance Controllers v8.1 and 8.0.

Not all issues affect all versions of the DDR and DDR2 SDRAM Controller High-Performance Controller.

Table 6–2. DDR and DDR2 SDRAM High-Performance Controller MegaCore Function Errata (Part 1 of 2)

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Feb 09</td>
<td>Intermittent Read Failure After Calibration</td>
<td>✓    ✓    ✓</td>
</tr>
<tr>
<td>01 Feb 09</td>
<td>Incorrect Controller Latency Information in User Guide</td>
<td>✓    —    —</td>
</tr>
<tr>
<td>01 Dec 08</td>
<td>DDR and DDR2 High-Performance Controllers Verilog HDL Design Doesn't Work</td>
<td>✓    —    —</td>
</tr>
<tr>
<td></td>
<td>SOPC Builder Does Not Recognize Decimal Points</td>
<td>✓    —    —</td>
</tr>
<tr>
<td>01 Nov 08</td>
<td>Inefficient Write Request to An Open Bank</td>
<td>Fixed ✓    —</td>
</tr>
<tr>
<td></td>
<td>Unnecessary Warning During Generation</td>
<td>Fixed ✓    ✓</td>
</tr>
<tr>
<td></td>
<td>Memory Timing Parameter tWR Is Set Incorrectly</td>
<td>Fixed ✓    ✓</td>
</tr>
<tr>
<td></td>
<td>Unable to Deliberately Corrupt the ECC Data When Using the Native Interface</td>
<td>Fixed ✓    ✓</td>
</tr>
<tr>
<td></td>
<td>DDR or DDR2 SDRAM High-Performance Controllers May Not Appear in SOPC Builder</td>
<td>Fixed ✓    ✓</td>
</tr>
</tbody>
</table>
Intermittent Read Failure After Calibration

The ALTMEMPHY megafuction leads to intermittent read failure after calibration.

Affected Configurations

This issue affects all designs that use DDR and DDR2 SDRAM High-Performance Controllers (versions 8.1 and previous) in full-rate mode and DQS-based capture.

Design Impact

Your design may fail in hardware at low frequency.

Workaround

Apply the patch provided at http://www.altera.com/support/kdb/solutions/rd12182008_673.html, and recompile your design.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controllers.

Incorrect Controller Latency Information in User Guide

The controller latency information in Tables C1 to C9 in the DDR and DDR2 SDRAM High-Performance Controllers User Guide 8.1 is incorrect.

The correct controller latency for DDR and DDR2 SDRAM high-performance controllers is 5 for half-rate controller and 4 for full-rate controller.

Solution Status

This issue will be fixed in v9.0 of the DDR and DDR2 SDRAM High-Performance Controllers User Guide.

---

Table 6–2. DDR and DDR2 SDRAM High-Performance Controller MegaCore Function Errata (Part 2 of 2)

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 Jul 08</td>
<td>Possibility of Calibration Failure</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>Precharge-all Command Not Always Issued Before Auto-Refresh Command</td>
<td>—</td>
</tr>
<tr>
<td>15 May 08</td>
<td>RTL Simulation May Fail When Dedicated Memory Clock Outputs Are Selected</td>
<td>✔</td>
</tr>
<tr>
<td></td>
<td>Gate Level Simulation Fails</td>
<td>✔</td>
</tr>
<tr>
<td></td>
<td>VHDL Simulation Fails When DDR CAS Latency 2.0 or 2.5 Is Selected</td>
<td>✔</td>
</tr>
<tr>
<td></td>
<td>Memory Presets Contain Some Incorrect Memory Timing Parameters</td>
<td>✔</td>
</tr>
<tr>
<td>15 Oct 07</td>
<td>Mimic Path Incorrectly Placed</td>
<td>✔</td>
</tr>
<tr>
<td>01 Dec 06</td>
<td>Simulating with the NCSim Software</td>
<td>✔</td>
</tr>
<tr>
<td></td>
<td>Simulating with the VCS Simulator</td>
<td>✔</td>
</tr>
</tbody>
</table>
DDR and DDR2 High-Performance Controllers Verilog HDL Design Doesn’t Work

If you generate a Verilog HDL instance of the DDR or DDR2 High-Performance Controller version 8.1, the design will not work in hardware or simulation.

Affected Configurations

This issue affects all Verilog HDL instances of the Insert extra pipeline registers in datapath option enabled. The VHDL designs are not affected.

Design Impact

Your design will not work in hardware or simulation.

Workaround

If you require a Verilog HDL instance of the DDR or DDR2 SDRAM High-Performance Controller, you can use one of the following workarounds:

- Continue to use your existing version 8.0 instance. There are no functional changes between versions 8.0 and 8.1 of the DDR or DDR2 SDRAM High-Performance Controller, so you are not required to upgrade.

- If you choose to upgrade to version 8.1 or if you do not have a version 8.0 instance, edit the <variation name>_auk_ddr_sdram.v file to change all instances of the line:

```
else if (0)
```

- to

```
else if (1)
```

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controllers.

SOPC Builder Does Not Recognize Decimal Points

If you assign the PLL clock with a value with decimals, SOPC Builder takes only the whole number and does not recognize the value after the decimal point. When you generate the system, the “The PLL reference clock of <value> does not match the clock frequency input to refclk” error message appears.

Affected Configurations

This issue affects all designs that have a PLL clock value with decimals.

Design Impact

Your system cannot be generated.

Workaround

Ignore the error message, and generate the system by holding down the Ctrl key on the keyboard while clicking Generate in SOPC Builder.
Solution Status
This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controllers.

Inefficient Write Request to An Open Bank
If your design requests consecutive write commands to the same open row, the controller will stall every eight clock cycles. It should be able to accept consecutive write accesses to the same open row until the next auto-refresh command is scheduled.

Affected Configurations
This issue only affects DDR2 SDRAM controllers configured for CAS latency of five or greater.

Design Impact
Your design will not be as efficient as it should be.

Workaround
Reduce the CAS latency setting to four.

Solution Status
This issue is fixed in v8.1 of the DDR and DDR2 SDRAM High-Performance Controllers.

Unnecessary Warning During Generation
If you have not enabled the Generate simulation model option, you will see the following warning when generating your controller variation.

Warning: <your design directory>/<variation>_auk_ddr_hp_controller_wrapper.vho doesn't exist but should have been created by IPToolbench.

Affected Configurations
This issue affects designs that have the Generate simulation model option turned off.

Design Impact
None. You can ignore this warning.

Workaround
None required.

Solution Status
This issue is fixed in v8.1 of the DDR and DDR2 SDRAM High-Performance Controllers.
Memory Timing Parameter tWR Is Set Incorrectly

The tWR memory timing parameter is set to twice the number of clock cycles that it should be if the Local interface clock frequency setting is set to Half.

Affected Configurations

This issue affects designs that have the Native interface option turned on.

Design Impact

You design may suffer from lower efficiency than expected.

Workaround

Edit the `<variation_name>_auk_ddr_hp_controller_wrapper.v` file (for both Verilog HDL or VHDL) and change the value assigned to the `mem_twr` signal to half of the original value, rounding up to the nearest integer. For example, if the Megawizard® applied a value of 3 cycles to the tWR parameter, change the assignment from

```verilog
assign mem_twr = 3'b011;
```

to

```verilog
assign mem_twr = 3'b010;
```

This change will only affect the design in hardware. The simulation model will still use the value set by the Megawizard.

Solution Status

This issue is fixed in v8.1 of the DDR and DDR2 SDRAM High-Performance Controllers.

Unable to Deliberately Corrupt the ECC Data When Using the Native Interface

When the Native interface option is turned on, you cannot enable the deliberate corruption of ECC data, which is used to test the functionality of the ECC logic. You must choose the Avalon Memory-Mapped interface option to be able to generate corrupted ECC data.

Affected Configurations

This issue affects designs that have the Native interface option turned on.

Design Impact

You cannot fully test the ECC functionality in the selected configuration.

Workaround

Change the local interface protocol to Avalon Memory-Mapped interface.

Solution Status

This issue is fixed in v8.1 of the DDR and DDR2 SDRAM High-Performance Controllers.
DDR or DDR2 SDRAM High-Performance Controllers May Not Appear in SOPC Builder

Under some circumstances, it is possible that the DDR or DDR2 SDRAM High-Performance Controllers do not appear in SOPC Builder. This is due to an indexing issue.

Affected Configurations
This issue affects SOPC Builder designs that use DDR or DDR2 SDRAM High-Performance Controllers.

Design Impact
The DDR or DDR2 SDRAM High-Performance Controllers may not appear in SOPC Builder when it is first launched.

Workaround
To make the DDR or DDR2 SDRAM High-Performance Controllers appear, follow these steps:
1. Close the SOPC Builder and the Quartus® II software.
2. Delete the C:\Documents and Settings\<username>\altera.quartus\ip_cache directory if you are using Windows or $HOME/altera.quartus/ip_cache if you are using Linux or Solaris.
3. Restart the SOPC Builder and the Quartus II software.
This causes the index to be regenerated and the DDR and DDR2 High-Performance Controllers to appear.

Solution Status
This issue is fixed in v8.1 of the DDR and DDR2 SDRAM High-Performance Controllers.

Possibility of Calibration Failure

Designs with the DDR or DDR2 SDRAM High Performance Controller IP created in the Quartus II software version 8.0 that target DDR or DDR2 SDRAM could fail to calibrate correctly in hardware under certain conditions.

Affected Configurations
This issue affects all variations and device families.

Design Impact
Your design may fail to operate correctly in hardware.

Workaround
Regenerate the memory controller with the Quartus II software version 8.0 SP1.

Solution Status
This issue is fixed in v8.0 SP1 of the DDR and DDR2 SDRAM High Performance Controllers.
Precharge-all Command Not Always Issued Before Auto-Refresh Command

If your design has eight chip selects and no reads or writes have happened to the lower four chip selects since the last auto-refresh command, the controller will issue an auto-refresh command without first issuing a precharge all command.

Affected Configurations
This issue only affects controllers with eight chip selects.

Design Impact
Your design may fail to operate correctly.

Workaround
Regenerate your controller instance in the latest version of the DDR and DDR2 SDRAM High Performance Controller.

Solution Status
This issue is fixed in v8.0 SP1 of the DDR and DDR2 SDRAM High Performance Controllers.

RTL Simulation May Fail When Dedicated Memory Clock Outputs Are Selected

The example testbench RTL simulation may not simulate correctly when a dedicated memory clock phase is selected because clock net delay between the PLL and the clock output pins is not modelled in the RTL.

Affected Configurations
This issue affects designs that enable the Use dedicated PLL outputs to drive memory clocks option and set a value for Dedicated memory clock phase parameter.

Design Impact
The design does not simulate correctly.

Workaround
Add MEM_CLK_DELAY to clk_to_ram signal at example top-level testbench, to compensate for the on-chip clock net delay to mem_dqs which is not present in the RTL simulation.

```vhdl
parameter DED_MEM_CLK = 1;
parameter real DED_MEM_CLK_PHASE = <value for dedicated memory clock phase>
parameter real mem_clk_ratio = ((360.0*DED_MEM_CLK_PHASE)/360.0);
parameter MEM_CLK_DELAY = mem_clk_ratio*CLOCK_TICK_IN_PS * (DED_MEM_CLK ? 1 : 0);
wire clk_to_ram0, clk_to_ram1, clk_to_ram2;
assign #(MEM_CLK_DELAY/4.0) clk_to_ram2 = clk_to_sdram[0];
assign #(MEM_CLK_DELAY/4.0) clk_to_ram1 = clk_to_ram2;
assign #(MEM_CLK_DELAY/4.0) clk_to_ram0 = clk_to_ram1;
assign #(MEM_CLK_DELAY/4.0)) clk_to_ram = clk_to_ram0;
//Replace testbench clk_to_ram assignment by adding MEM_CLK_DELAY
//assign clk_to_ram = clk_to_sdram[0];
```
Solution Status
This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controllers.

Gate Level Simulation Fails
Gate level simulation of the example design and example testbench fails when Use differential DQS is enabled in DDR2 High-Performance Controller.

Affected Configurations
This issue affects DDR2 SDRAM High Performance Controller designs in Stratix III and Stratix IV devices that have the Use differential DQS option enabled.

Design Impact
Gate level simulation of the example design does not behave correctly.

Workaround
You can use the following options:
1. To connect dqs_n example top-level design:
   - .mem_dqsn(mem_dqsn)
2. To connect dqs_n in memory model
   - DQSN mem_dqsn[index])

Solution Status
This issue will be fixed in a future version of the DDR2 SDRAM High-Performance Controller.

VHDL Simulation Fails When DDR CAS Latency 2.0 or 2.5 Is Selected
VHDL generated sequencer block for CAS latency 2.0 and 2.5 designs using DDR SDRAM High-Performance Controller results in simulation failure. The issue is due to delta cycle delays on a clock net.

Affected Configurations
This issue affects DDR SDRAM High-Performance Controller CAS latency 2.0 and 2.5 designs.

Design Impact
This issue only affects simulation on VHDL and does not affect the functionality of the design.

Workaround
To workaround this issue, follow these steps:
1. Open the <variation_name>_phy_vho file in the project directory.
2. Search for the altsyncram instantiation for the postamble block (this can be done by searching for " altsyncram" - note the white space). This should be the altsyncram component with a label which includes the word "postamble".

3. Search for the signal which is attached to the clock1 port to find the point in the design where this signal is assigned to (in a test case, this is on line 4043).

```verilog
wire_<variation_name>_phy_<variation_name>_phy_alt_mem Phy_sii_<variation_name>_phy_alt_mem_phy_sii Inst_<variation_name>_phy_alt_mem_phy_postamble_sii_poa_altsyncram_half_rate_ram_gen_altsyncram_inst_19557_clock1
```

4. Change the assignment as shown below. The signal inside not(..) should be the same as the signal on clock0 port of a second instance of the altsyncram component which is associated to the read datapath (with "read_dp" in the label).

```verilog
wire_<variation_name>_phy_<variation_name>_phy_alt_mem Phy_sii_<variation_name>_phy_alt_mem_phy_sii Inst_<variation_name>_phy_alt_mem_phy_postamble_sii_poa_altsyncram_half_rate_ram_gen_altsyncram_inst_19557_clock1 <= not (wire_<variation_name>_phy_<variation_name>_phy_alt_mem Phy_sii_<variation_name>_phy_alt_mem_phy_sii Inst_<variation_name>_phy_alt_mem_phy_clk_reset_sii_clk_<variation_name>_phy_alt_mem_phy_pll_sii_pll_19462_c4);
```

This step removes a delta delay for simulation but leaves the code unchanged. The right hand side of the assignment above is taken as the right hand side of the assignment to the signal which is previously assigned to the "wire_<variation_name>_phy_<variation_name>_phy_alt_mem Phy_sii_<variation_name>_phy_alt_mem_phy_sii Inst_<variation_name>_phy_alt_mem_phy_postamble_sii_poa_altsyncram_half_rate_ram_gen_altsyncram_inst_19557_clock1" signal.

5. If the <variation_name>_phy component is recompiled in your simulator, the design should now pass.

**Solution Status**

This issue will be fixed in a future version of the DDR SDRAM High-Performance Controller.

**Memory Presets Contain Some Incorrect Memory Timing Parameters**

The memory presets contain incorrect data for the tDSa and tDHa memory timing parameters.

**Affected Configurations**

This issue affects all configurations.

**Design Impact**

Timing analysis results for write and address/command paths may be incorrect.
**Workaround**

Make sure that the memory timing parameters in the MegaWizard Plug-In Manager match the datasheet of the target memory device. The output edge rate and the use of single-ended versus differential DQS, may affect certain memory parameters.

**Solution Status**

This issue will be fixed in a future version of the DDR2 SDRAM High-Performance Controller.

**Mimic Path Incorrectly Placed**

The Quartus II software may fail to place the mimic path correctly. The report timing script then indicates a timing setup failure on the mimic path.

**Affected Configurations**

This issue affects all designs.

**Design Impact**

Your design may fail.

**Workaround**

Manually edit the following parameter in the autogenerated Synopsis design constraint (.sdc) script to correct the timing analysis:

```
mimic_shift
```

Add a value of at least the worst case failed slack to the value already stated in the Synopsis design constraint file.

**Solution Status**

This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controllers.

**Simulating with the NCSim Software**

The DDR and DDR2 SDRAM High-Performance Controller MegaCore functions do not fully support the NCSim software.

**Affected Configurations**

This issue affects all configurations.

**Design Impact**

The design does not simulate.

**Workaround**

Set the `–relax` switch for all calls to the VHDL analyzer.
**Solution Status**

This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controllers.

**Simulating with the VCS Simulator**

The DDR and DDR2 SDRAM High-Performance Controller MegaCore functions do not fully support the VCS simulator.

**Affected Configurations**

This issue affects all configurations.

**Design Impact**

The design does not simulate.

**Workaround**

The following workarounds exist.

**VHDL**

Change the following code.

- In file `<variation name>_example_driver.vhd`, change all when statements between lines 333 and 503 from `when std_logic_vector'(<bit_pattern>)` to `when "<bit_pattern>".`

- In file `testbench\<example name>_tb`, change line 191 from `signal zero_one(gMEM_BANK_BITS -1 downto 0) := (0 => '1', others => '0')` to `signal zero_one(gMEM_BANK_BITS -1 downto 0) := ('1', others=> '0').`

**Verilog HDL**

No changes are necessary. Calls to the Verilog analyzer sets the +v2k switch to enable Verilog 2000 constructs.

**Solution Status**

This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controllers.
7. DDR3 SDRAM High-Performance Controller

Revision History

Table 7–1 shows the revision history for the DDR3 SDRAM High-Performance Controller MegaCore® function.

For more information on the new features, refer to the DDR3 SDRAM High-Performance Controller MegaCore Function User Guide.

Table 7–1. DDR3 SDRAM High-Performance Controller MegaCore Function Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>■ Reduced controller latency and improved efficiency.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Improved example top-level design.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Support for multiple synchronous controllers in an SOPC Builder-generated design.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>■ Preliminary support Stratix® IV devices.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Optional support for self-refresh and power-down commands.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Optional support for auto-precharge read and auto-precharge write commands.</td>
</tr>
<tr>
<td>7.2</td>
<td>October 2007</td>
<td>First release.</td>
</tr>
</tbody>
</table>

Errata

Table 7–2 shows the issues that affect the DDR3 SDRAM Controller High-Performance Controller v8.1, 8.0 and 7.2.

Table 7–2. DDR3 SDRAM High-Performance Controller MegaCore Function Errata

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Feb 09</td>
<td>Incorrect Controller Latency Information in User Guide</td>
<td>8.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>8.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>7.2</td>
</tr>
<tr>
<td>01 Nov 08</td>
<td>Unable to Deliberately Corrupt the ECC Data When Using the Native Interface</td>
<td>Fixed</td>
</tr>
<tr>
<td></td>
<td>DDR3 SDRAM High-Performance Controllers May Not Appear in SOPC Builder</td>
<td>Fixed</td>
</tr>
<tr>
<td>15 Oct 07</td>
<td>Generate Netlist Option Does Not Work</td>
<td>Fixed</td>
</tr>
</tbody>
</table>

Incorrect Controller Latency Information in User Guide

The controller latency information in Tables B2 and B3 in the DDR3 SDRAM High-Performance Controller User Guide 8.1 is incorrect.

The correct controller latency for DDR3 SDRAM high-performance controller is 5.

Solution Status

This issue will be fixed in v9.0 of the DDR3 SDRAM High-Performance Controller User Guide.
Unable to Deliberately Corrupt the ECC Data When Using the Native Interface

When the Native interface option is turned on, you cannot enable the deliberate corruption of ECC data, which is used to test the functionality of the ECC logic. You must choose the Avalon Memory-Mapped interface option to be able to generate corrupted ECC data.

Affected Configurations
This issue affects designs that have the Native interface option turned on.

Design Impact
You cannot fully test the ECC functionality in the selected configuration.

Workaround
Change the local interface protocol to Avalon Memory-Mapped interface.

Solution Status
This issue is fixed in v8.1 of the DDR3 SDRAM High-Performance Controller.

DDR3 SDRAM High-Performance Controllers May Not Appear in SOPC Builder

Under some circumstances, it is possible that the DDR3 SDRAM High-Performance Controllers do not appear in SOPC Builder. This is due to an indexing issue.

Affected Configurations
This issue affects SOPC Builder designs that use DDR3 SDRAM High-Performance Controllers.

Design Impact
The DDR3 SDRAM High-Performance Controllers may not appear in SOPC Builder when it is first launched.

Workaround
To make the DDR3 SDRAM High-Performance Controllers appear, follow these steps:
1. Close the SOPC Builder and the Quartus® II software.
2. Delete the C:\Documents and Settings\<username>\altera.quartus\ip_cache directory if you are using Windows or $HOME/altera.quartus/ip_cache if you are using Linux or Solaris.
3. Restart the SOPC Builder and the Quartus II software.

This causes the index to be regenerated and the DDR3 High-Performance Controller to appear.

Solution Status
This issue is fixed in v8.1 of the DDR3 SDRAM High-Performance Controller.
Generate Netlist Option Does Not Work

If you turn on the Generate netlist option, the wizard does not generate a timing and resource estimation netlist.

Affected Configurations
This issue affects designs that have Generate Netlist turned on.

Design Impact
You cannot generate a timing and resource estimation netlist to use with a third-party synthesis tool to estimate timing and resource usage. There is no functional impact.

Workaround
None.

Solution Status
This issue is fixed in v8.0 of the DDR3 SDRAM High-Performance Controller.
8. FFT

Revision History

Table 8–1 shows the revision history for the FFT MegaCore® function.

For more information on the new features, refer to the FFT MegaCore Function User Guide.

Table 8–1. FFT MegaCore Function Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>Full support for Stratix® III devices.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>■ Full support for Cyclone® III devices</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Preliminary support for Stratix IV devices</td>
</tr>
<tr>
<td>7.2</td>
<td>October 2007</td>
<td>■ Enhanced variable streaming FFT with single precision floating point or fixed point representation</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Corrected many timing diagrams</td>
</tr>
</tbody>
</table>

Errata

Table 8–2 shows the issues that affect the FFT MegaCore function v8.1, 8.0, and 7.2.

Not all issues affect all versions of the FFT MegaCore function.

Table 8–2. FFT MegaCore Function Errata

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Nov 08</td>
<td>Display Symbol Button in IP Toolbench is Missing</td>
<td>✓</td>
</tr>
<tr>
<td>01 Oct 07</td>
<td>Cannot Find Memory Initialization File if Not in Project Directory</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>Floating-Point FFT Produces Non-Zero Output</td>
<td>✓</td>
</tr>
<tr>
<td>01 Dec 06</td>
<td>Simulation Errors—Synopsys VCS</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>Simulation Errors—Incorrect Results</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>Simulation Errors—MATLAB Model Mismatch</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>Gate-Level Simulations</td>
<td>✓</td>
</tr>
</tbody>
</table>

Display Symbol Button in IP Toolbench is Missing

The Display Symbol button in IP Toolbench does not appear, even though the screenshot in the user guide implies it should appear.

Affected Configurations

This issue affects all designs.
Design Impact
There is no design impact.

Workaround
This issue has no workaround.

Solution Status
This issue will be fixed in a future version of the FFT MegaCore function.

Cannot Find Memory Initialization File if Not in Project Directory

The Quartus® II software cannot find the memory initialization files (HEX files) required by the design and issues a critical warning of the form:

Critical Warning: Can't find Memory Initialization File or Hexadecimal (Intel-Format) File C:/temp/mlab_test/fir_test0_coef_0.hex -- setting all initial values to 0

Affected Configurations
This issue is observed when the generated IP files are not in the same directory as your project setting files .qsf and .qpf files. For example, if your project involves many submodules and each submodule resides in a separate subdirectory.

Design Impact
The Quartus II software issues critical warnings for the missing files and generates a functionally incorrect netlist because of the missing memory initialization files.

Workaround
Add the path of the folder containing your generated IP files to the user libraries parameter in the .qsf file. For example, if your top-level project directory is c:/myprojects/bigSystem and you have generated the FFT in c:/myprojects/bigSystem/FFTmodule/.

In your project's .qsf file (in c:/myprojects/bigSystem), look for a line that starts set_global_assignment -name USER_LIBRARIES ...

Append the IP directory c:/myprojects/bigSystem/FFTmodule in the following code:

set_global_assignment -name USER_LIBRARIES "C:/altera/72/ip/fft/lib;C:/myprojects/bigSystem/FFTmodule"

After you save your changes, recompile your project and check that the critical warning is no longer displayed.

Solution Status
This issue will be fixed in a future version of the FFT MegaCore function.
Floating-Point FFT Produces Non-Zero Output

When a DC signal is input to a floating-point variable streaming configuration of the FFT, the output is an impulse response, where bin 0 contains the magnitude of the impulse response and the other bins should be 0. The value in bin 0 is correct. However, non-zero values are encountered in the other bins. These values have a magnitude in the range of 10 to 39. More specifically, the exponent is zero, and the mantissa contains a non-zero number. The IEEE754 floating point specification refers to a number with a zero exponent and non-zero mantissa as denormalized. The floating point FFT does not support denormalized numbers, therefore any number with a zero exponent can be considered to have a zero mantissa.

Under these conditions, the MATLAB simulation model also produces output with a zero exponent and non-zero mantissa. However, the value of the mantissa does not match the value in simulation.

Affected Configurations
This issue affects all floating point variable streaming configurations of the FFT.

Design Impact
The design compiles but gives incorrect results under some circumstance. The MATLAB simulation model does not match the simulation results.

Workaround
The mantissa bits should be zeroed if the exponent is zero.

Solution Status
This issue will be fixed in a future version of the FFT MegaCore function.

Simulation Errors—Synopsys VCS

When you use NativeLink to perform an RTL simulation using the generated Verilog HDL testbench in the VCS simulator, you see the following error:

Error: VCS: to support this construct
Error: VCS: operator '***'.

Affected Configurations
This issue affects all Verilog HDL configurations.

Design Impact
There is no design impact; the design compiles correctly.

Workaround
In the Verilog HDL testbench <variation name>_tb.v, replace the power of operator '***' with the calculated value. Alternatively, compile with the +v2k option in the VCS simulator.
Solution Status
This issue will be fixed in a future version of the FFT MegaCore function.

Simulation Errors—Incorrect Results

When the input is defined as $N$ bit wide, the permissible input range is from $-2^{N-1} + 1$ to $2^{N-1} - 1$. If the input contains the value $-2^{N-1}$, the HDL output is incorrect, and does not match the MATLAB simulation result.

Affected Configurations
This issue affects all configurations.

Design Impact
The design compiles but gives incorrect results.

Workaround
If you expect your input signal to contain the value $-2^{N-1}$, you should add a block in front of the FFT, which maps the value $-2^{N-1}$ to $-2^{N-1} + 1$.

Solution Status
This issue will be fixed in a future version of the FFT MegaCore function.

Simulation Errors—MATLAB Model Mismatch

For one particular FFT parameter combination, the HDL output does not match the MATLAB simulation results (for some frames of data).

HDL simulation results are scaled down by a factor of two compared to the MATLAB simulation results. The exponent value produced by the HDL simulation is one less than the output of the MATLAB simulations. When the exponent is taken into account, the MATLAB and the HDL version may differ by one least significant bit (LSB).

Affected Configurations
This issue affects the following parameter combination:

- Transform length: 64
- I/O data flow: burst architecture
- FFT engine architecture: quad output
- Number of parallel engines: 2

Design Impact
There is no design impact, the design compiles and operates correctly.

Workaround
This issue has no workaround.
Solution Status
This issue will be fixed in a future version of the FFT MegaCore function.

Gate-Level Simulations
The testbench provided with the FFT MegaCore function is not suitable for gate-level simulations. The testbench assumes zero delays in post-fitting simulation models. Therefore, running gate-level simulations using the testbench may produce incorrect simulation results.

Affected Configurations
This issue affects all configurations.

Design Impact
There is no design impact; the design compiles correctly.

Workaround
Provide appropriate input and output constraints using the Quartus® II Assignments Editor and create a testbench that matches these requirements.

Solution Status
This issue will be fixed in a future version of the FFT MegaCore function.
9. FIR Compiler

Revision History

Table 9–1 shows the revision history for the FIR Compiler MegaCore® function.

For information on the new features, refer to the FIR Compiler User Guide.

Table 9–1. FIR Compiler Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>■ Full support for Stratix® III.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Withdrawn support for UNIX.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>■ Full support for Cyclone® III devices.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Preliminary support for Stratix IV devices.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Added option to automatically select memory block size for coefficient storage.</td>
</tr>
<tr>
<td>7.2</td>
<td>October 2007</td>
<td>■ Full support for Arria® GX devices.</td>
</tr>
</tbody>
</table>

Errata

Table 9–2 shows the issues that affect the FIR Compiler MegaCore function v8.1, v8.0, and v7.2.

Not all issues affect all versions of the FIR Compiler MegaCore function.

Table 9–2. FIR Compiler Errata (Part 1 of 2)

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Nov 08</td>
<td>Incorrect Screenshot in the User Guide</td>
<td>✔</td>
</tr>
<tr>
<td></td>
<td>Some Gate Level Simulations are Incorrect</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>Cannot Find Memory Initialization File if Not in Project Directory</td>
<td>Fixed</td>
</tr>
<tr>
<td>01 Oct 08</td>
<td>Block Memory Incorrectly Used When Logic Storage Selected</td>
<td>✔</td>
</tr>
<tr>
<td>15 May 08</td>
<td>Bit Serial Filter With 32-Bit Coefficients Does Not Work</td>
<td>✔</td>
</tr>
<tr>
<td>15 Oct 07</td>
<td>Input Signal Incorrectly Shown as Output in User Guide</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>Simulation Incorrect for Reloadable Coefficient Filters</td>
<td>Fixed</td>
</tr>
<tr>
<td></td>
<td>Simulation Result Incorrect Using MCV Interpolation Filters</td>
<td>✔</td>
</tr>
<tr>
<td>01 Oct 07</td>
<td>Reloadable Coefficient Filters Fail for Some MCV Filters</td>
<td>✔</td>
</tr>
<tr>
<td></td>
<td>Error When Preloading Coefficients for HardCopy Devices</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>coef_in Bit Width Incorrect When Using Manual Scaling</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>Half-Band Decimator &amp; Symmetric Interpolator Don’t Support Unsigned Type</td>
<td>✔</td>
</tr>
</tbody>
</table>
### Incorrect Screenshot in the User Guide

The IP Toolbench screenshot in Figure 2-3 of the user guide is out-of-date and shows the Display Symbol option although this feature is no longer supported.

**Solution Status**

This issue will be fixed in the next version of the FIR Compiler User Guide.

### Some Gate Level Simulations are Incorrect

The testbench for testing gate level simulation sometimes stimulates the FIR instantiation incorrectly and as a result the behavior of the testbench is not as expected.

**Affected Configurations**

This issue can potentially affect any gate level simulation using the provided testbench.

**Design Impact**

The test bench behaves incorrectly.

**Workaround**

Apply a delay of a quarter of a clock cycle to the source startofpacket and endofpacket Avalon-ST signals to make the timing consistent with the other data and control signals.

**Solution Status**

This issue is fixed in v8.1 of the FIR Compiler.

### Cannot Find Memory Initialization File if Not in Project Directory

The Quartus® II software cannot find the memory initialization files (HEX files) required by the design and issues a critical warning of the form:

```
Critical Warning: Can't find Memory Initialization File or Hexadecimal (Intel-Format) File C:/temp/mlab_test/fir_test0_coef_0.hex -- setting all initial values to 0
```

---

### Table 9-2. FIR Compiler Errata (Part 2 of 2)

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Dec 06</td>
<td>Signed Binary Fraction Results in Output Bit Width Mismatch</td>
<td>✔    ✔    ✔</td>
</tr>
<tr>
<td></td>
<td>Quartus II Simulation Vector File Not Generated</td>
<td>✔    ✔    ✔</td>
</tr>
<tr>
<td></td>
<td>Incorrect Multicycle Variable Architectures are Generated</td>
<td>—    —    Fixed</td>
</tr>
<tr>
<td></td>
<td>Graphical User Interface Freezes</td>
<td>—    —    Fixed</td>
</tr>
</tbody>
</table>

---

---

---
**Affected Configurations**
This issue is observed when the generated IP files are not in the same directory as your project setting files .qsf and .qpf. For example, if your project involves many sub modules and each sub module resides in a separate sub directory.

**Design Impact**
The Quartus II software issues critical warnings for the missing files and generates a functionally incorrect netlist due to the missing memory initialization files.

**Workaround**
Add the path of the folder containing your generated IP files to the user libraries parameter in the .qsf file. For example, if your top level project directory is C:/myprojects/bigSystem and you have generated the FIR filter in C:/myprojects/bigSystem/FIRmodule/.

In your project's .qsf file (in C:/myprojects/bigSystem), look for a line that starts set_global_assignment -name USER_LIBRARIES ... Append the IP directory C:/myprojects/bigSystem/FIRmodule as shown below:

```
set_global_assignment -name USER_LIBRARIES
"C:/altera/72/ip/fir_compiler/lib;C:/myprojects/bigSystem/FIRmodule"
```

After you save your changes, recompile your project and check that the critical warning is no longer displayed.

**Solution Status**
This issue is fixed in v8.1 of the FIR Compiler.

**Block Memory Incorrectly Used When Logic Storage Selected**
For some instances of the FIR MegaCore function, if you select logic based storage for data and coefficients, it is possible that the results of synthesis may include some block memory.

**Affected Configurations**
Configurations with FIR storage set to logic elements.

**Design Impact**
Unwanted block memory is used.

**Workaround**
Turn off Auto Shift Register Replacement in the Quartus II More Analysis and Synthesis Settings dialog box. This dialog box can be accessed by clicking More Settings in the Analysis & Synthesis Setting page of the Settings dialog box accessed from the Assignments menu in the Quartus II software.

**Solution Status**
This issue will be fixed in a future version of the FIR Compiler.
Bit Serial Filter With 32-Bit Coefficients Does Not Work

The generated netlist may be incorrect if the maximum coefficient width is 32.

Affected Configurations

All distributed arithmetic based architectures (fully serial, multi bit serial, and fully parallel).

Design Impact

The generated netlist is incorrect.

Workaround

Limit the input precision to 31 bits and change the coefficient storage to logic cells. Alternatively, you can use a multicycle variable architecture which gives correct results for 32-bit coefficients.

Solution Status

This issue will be fixed in a future version of the FIR Compiler.

Input Signal Incorrectly Shown as Output in User Guide

The v7.2 user guide shows the ast_sink_error signal as an output in the list of signals (Table 3-3 on page 3-20) but it should be listed as an input.

Solution Status

This issue is fixed in v8.0 of the FIR Compiler User Guide.

Simulation Incorrect for Reloadable Coefficient Filters

Incorrect output from simulation models for reloadable coefficient filters.

Affected Configurations

This issue is observed in some FIR filters with reloadable coefficients. This is due to the simulation model generation mechanism that randomly initializes the registers associated with the coefficient reload mechanism.

Design Impact

The simulation model does not work properly.

Workaround

Use gate level simulation instead.

Solution Status

This issue is fixed in v8.0 of the FIR Compiler.

Simulation Result Incorrect Using MCV Interpolation Filters

Some multicycle variable interpolation filters with high interpolation factors may generate incorrect output.
Affected Configurations
This issue affects MCV interpolation filters with high interpolation factors and forced non-symmetric implementation where the pipelining level is set to greater than 1 for higher \( f_{\text{MAX}} \).

Design Impact
The produced output doesn’t match the expected output.

Workaround
Change the pipelining level to 1. This may result in lower \( f_{\text{MAX}} \) but the filter output will match the expected output.

Solution Status
This issue will be fixed in a future version of the FIR Compiler.

Reloadable Coefficient Filters Fail for Some MCV Filters
Some reloadable coefficient filters with multicycle variable architecture do not produce the right output when a new set of coefficient is reloaded.

Affected Configurations
This error is observed in some of the reloadable coefficient MCV filters.

Design Impact
The produced output does not match the expected output when the new coefficient set is reloaded.

Workaround
There are two separate problems which may cause this failure. If your target device is Cyclone III, change the device to Stratix II or Stratix III in the FIR Compiler GUI and regenerate the filter. (Your device selection in the Quartus II project should stay the same.) If the coefficient storage is set to logic cells, change to a block memory (such as M512, M9K, or Auto).

Solution Status
This issue will be fixed in a future version of the FIR Compiler.

Error When Preloading Coefficients for HardCopy Devices
Some FIR architectures cannot preload coefficient memories in HardCopy devices.

Affected Configurations
This issue affects configurations targeting HardCopy devices.

Design Impact
Some FIR architectures fail during synthesis when targeting hardcopy devices.
Workaround
Avoid using pre-initialized memory by selecting data storage and coefficient storage to be logic elements.

Solution Status
This issue is fixed in v8.0 of the FIR Compiler.

coeff_in Bit Width Incorrect When Using Manual Scaling
For a reloadable coefficient FIR filter when the Coefficients Scaling type is set to Manual, the coefficient bit width calculations are incorrect.

Affected Configurations
This issue affects all reloadable coefficient filters with manual coefficient scaling.

Design Impact
The simulation model generation and Quartus II compilation fails. The incorrect bit width can be observed from the output bit width displayed in the GUI.

Workaround
Avoid selecting manual coefficient scaling for reloadable coefficient filters. If you need to use manual scaling, you can do the following:

- **If you want to load your own set of coefficients:** Scale them before you load them into the FIR Compiler. Then set the Coefficients Scaling to None in the main Parameterize window. You will notice that the output bit width displayed in the GUI has changed. The simulation model will also generate successfully.

- **If you want to generate the filter coefficients using the coefficient generator:** First design a filter with fixed coefficients. Set the manual scaling factor as you require, then generate this filter. The coefficient set is written to a file `<your_fir_filter>_coef_int.txt`.

  Restart the FIR compiler to edit your filter parameters but this time, go to the Edit Coefficient Set page, and instead of generating the coefficients, choose to import the `<your_fir_filter>_coef_int.txt` file. Load this file and change the Coefficients Scaling type to None in the main Parameterize window. You will notice that the output bit width displayed in the GUI has changed. The simulation model will also generate successfully.

Solution Status
This issue is fixed in v7.2 of the FIR Compiler.

Half-Band Decimator & Symmetric Interpolator Don’t Support Unsigned Type
The half-band decimator and symmetric interpolator filters do not support unsigned input data type.

Affected Configurations
This issue affects half-band decimator and symmetric interpolator filter architectures.
Design Impact
The FIR filter produces incorrect results.

Workaround
The half-band decimator and symmetric interpolator filter architectures require signed input data types. To ensure it works with unsigned data, design the filter with input ports 1-bit larger than the original value and connect the MSB bit of the ast_sink_data input port to 0.

Solution Status
This issue will be fixed in a future version of the FIR Compiler.

Signed Binary Fraction Results in Output Bit Width Mismatch
For signed binary fraction data types, some FIR filter variations fail Quartus® II compile and simulation model generation.

Affected Configurations
This issue affects all configurations with signed binary fraction data types.

Design Impact
Compilation fails in the Quartus II software.

Workaround
This issue is related to a user interface issue. In some cases, when you reopen the variation file using IP Toolbench and re-generate the filter the issue is resolved. If it still fails compilation, use one of the other data types (Signed Binary or Unsigned Binary).

Solution Status
This issue will be fixed in a future version of the FIR Compiler.

Quartus II Simulation Vector File Not Generated
FIR Compiler does not create a vector file for Quartus II simulation.

Affected Configurations
This issue affects all configurations.

Design Impact
The design can be compiled, but there is no automatically generated vector file testbench available to simulate the design in the Quartus II software.

Workaround
Use NativeLink to simulate the VHDL testbench instead.
**Solution Status**
This issue will be fixed in a future version of the FIR Compiler.

**Incorrect Multicycle Variable Architectures are Generated**
The FIR Compiler can generate incorrect code if you use all of the following GUI settings:
- The multicycle variable (MCV) architecture
- A high number of coefficients
- A low number of bits per coefficient
- A high number of cycles
- Turn on coefficient reloading

**Affected Configurations**
This issue affects FIR Compiler configurations that use the previously mentioned settings.

**Design Impact**
This issue causes the FIR Compiler GUI to generate incorrect code.

**Workaround**
To avoid this issue, you should instantiate separate filters such that each filter uses only a part of the coefficients. Then, combine the results of these filters.

**Solution Status**
This issue is fixed in v7.2 of the FIR Compiler.

**Graphical User Interface Freezes**
When you choose a Coefficient Width of 2 bits and at the same time set the coefficient scaling to Auto Power of 2, the graphical user interface (GUI) cannot produce the function and the GUI can freeze.

**Affected Configurations**
This issue affects FIR Compiler configurations that use the previously mentioned GUI settings.

**Design Impact**
This issue causes the GUI to freeze.

**Workaround**
To use a Coefficient Width of 2, manually scale the coefficients to the desired range using the manual coefficient scaling option instead of the Auto Power of 2 option. Alternatively, you can perform the scaling externally and import the coefficients as text file. When importing coefficients, set the coefficient scaling option to None.
**Solution Status**

This issue is fixed in v7.2 of the FIR Compiler.
10. HyperTransport

Revision History

Table 10–1 shows the revision history for the HyperTransport MegaCore® function.

For more information about the new features, refer to the *HyperTransport MegaCore Function User Guide*.

Table 10–1. HyperTransport MegaCore Function Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>□ Maintenance release</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>□ Maintenance release</td>
</tr>
<tr>
<td>7.2 SP1</td>
<td>December 2007</td>
<td>□ Fixed link hang or corruption in Shared Rx/Tx Clocks mode</td>
</tr>
<tr>
<td>7.2</td>
<td>October 2007</td>
<td>□ Maintenance release</td>
</tr>
</tbody>
</table>

Errata

Table 10–2 shows the issues that affect the HyperTransport MegaCore function in v8.1, v8.0, v7.2 SP1, and v7.2.

Table 10–2. HyperTransport MegaCore Function Errata

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Dec 07</td>
<td>HyperTransport Link Hang or Corruption in Shared Rx/Tx Clocks Mode</td>
<td>8.1 8.0 7.2 SP1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fixed</td>
</tr>
</tbody>
</table>

**HyperTransport Link Hang or Corruption in Shared Rx/Tx Clocks Mode**

Due to an incorrect Tx Sync FIFO reset circuit, the Tx Sync FIFO control logic can be corrupted at the end of reset. This condition results in incorrect data being transmitted on the HyperTransport link, which typically results in the system’s hanging when the first response to the first configuration read is corrupted.

**Affected Configurations**

This condition affects only variations that use the Shared Rx/Tx Clocks mode.

**Design Impact**

This condition infrequently results in the HyperTransport link’s hanging immediately after reset.

**Workaround**

The following workarounds may be used:

□ If possible, select a different clocking option for your design.
- Reset the system when it hangs.

**Solution Status**

This issue is fixed in version 7.2 SP1 of the HyperTransport MegaCore function.
Revision History

Table 11–1 shows the revision history for the NCO MegaCore® function.

For information on the new features, refer to the NCO MegaCore Function User Guide.

Table 11–1. NCO MegaCore Function Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>• Full support for Stratix® III.  &lt;br&gt; • Withdrawn support for UNIX.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>• Full support for Cyclone® III devices.  &lt;br&gt; • Preliminary support for Stratix® IV devices.</td>
</tr>
<tr>
<td>7.2</td>
<td>October 2007</td>
<td>• Full support for Arria® GX devices.  &lt;br&gt; • Performance improvements for CORDIC architectures.</td>
</tr>
</tbody>
</table>

Errata

Table 11–2 shows the issues that affect the NCO MegaCore function v8.1, v8.0, and v7.2.

Not all issues affect all versions of the NCO MegaCore function.

Table 11–2. NCO MegaCore Function Errata

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
<th>8.1</th>
<th>8.0</th>
<th>7.2</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Oct 07</td>
<td>Mismatches Between Multiplier-Based MATLAB and RTL Models</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>01 Jun 07</td>
<td>Invalid Outputs if Magnitude Precision is Greater than 24</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>01 May 07</td>
<td>Mismatches Between the MATLAB and RTL Models  &lt;br&gt; Crash on Linux if Sum of Precision and Dither Greater than 32  &lt;br&gt; Cannot Generate Large Angular Precision ROM Parameters  &lt;br&gt; MisMatch If Frequency Modulation and Dithering are Both Used</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>01 Dec 06</td>
<td>The MATLAB Simulation File Cannot be Used on UNIX</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Mismatches Between Multiplier-Based MATLAB and RTL Models

For the multiplier-based architecture with throughput = 1 (output every clock cycle), there can be mismatches between the output of the MATLAB model and the RTL output for values of magnitude precision. These mismatches seem to be rounding errors for very large values.
**Affected Configurations**

Multiplier-based architecture with throughput = 1 of the NCO MegaCore function.

**Design Impact**

Comparison of the output values from the MATLAB model and RTL design during testing may show mismatches. However, the error margin is small in both absolute and relative terms. For example, the MATLAB model calculates -536,870,910, whereas the RTL calculates -536,870,911.

**Workaround**

The RTL design works correctly, but comparison between MATLAB model and RTL cannot be done automatically.

**Solution Status**

This issue will be fixed in a future version of the NCO MegaCore function.

**Invalid Outputs if Magnitude Precision is Greater than 24**

Some of the ROM entries used in the small ROM, large ROM, and multiplier-based architectures are incorrect if a magnitude precision greater than 24 bits is selected.

**Affected Configurations**

Small ROM, large ROM, and Multiplier based architectures of the NCO MegaCore function.

**Design Impact**

The sine and cosine outputs from the design are invalid.

**Workaround**

If a magnitude precision of greater than 24 bits is required, a CORDIC architecture should be selected.

**Solution Status**

This issue is fixed in v7.2 of the NCO MegaCore function.

**Mismatches Between the MATLAB and RTL Models**

For the multiplier-based architecture with throughput = ½ (output every 2nd clock cycle), and for the serial CORDIC architecture, there can be mismatches between the output of the MATLAB model and the RTL output for certain parameter combinations. This is because some initial output values are not covered by either the MATLAB model or the RTL design, while the other values match.

**Affected Configurations**

Multiplier-based architecture with halved throughput and serial CORDIC architectures of the NCO MegaCore function.
**Design Impact**
Automatic comparison of the output values from the MATLAB model and RTL design during testing may show mismatches.

**Workaround**
The RTL design works correctly, but comparison between MATLAB model and RTL cannot be done automatically.

**Solution Status**
This issue will be fixed in a future version of the NCO MegaCore function.

**Crash on Linux if Sum of Precision and Dither Greater than 32**
When the multiplier-based architecture is used together with dithering, the MATLAB model crashes on a Linux platform, if the sum of angular precision (maximum 32 bits) and dithering (maximum level 8) is greater than 32.

**Affected Configurations**
Multiplier based architectures of the NCO MegaCore function on a Linux platform.

**Design Impact**
The MATLAB model crashes with a segmentation violation.

**Workaround**
If a large angular precision needs to be used combined with dithering, either a different architecture should be chosen, or the MATLAB model should be run on a Windows platform.

**Solution Status**
This issue is fixed in v7.2 of the NCO MegaCore function.

**Cannot Generate Large Angular Precision ROM Parameters**
IP Toolbench cannot generate NCO designs for large parameters of angular and magnitude precision in the ROM-based architectures.

**Affected Configurations**
Large ROM and Small ROM architectures of the NCO MegaCore function.

**Design Impact**
IP Toolbench does not close the Parameterize Window when the Finish button is pressed unless smaller values for angular and/or magnitude precision are selected.

**Workaround**
Use smaller value precision parameters, a different NCO architecture (multiplier or CORDIC based), or choose a device with more memory.
Solution Status
This issue is fixed in v7.2 of the NCO MegaCore function.

MisMatch If Frequency Modulation and Dithering are Both Used
There are slight mismatches between the MATLAB model and RTL for the serial CORDIC architecture of the NCO if both frequency modulation input and dithering are used. However, both generate sine/cosine waves correctly and the differences between the corresponding values are small.

Affected Configurations
Serial CORDIC architectures of the NCO MegaCore function.

Design Impact
The output values from the RTL design are inaccurate.

Workaround
Use a different architecture if both frequency modulation input and dithering are necessary.

Solution Status
This issue is fixed in v7.2 of the NCO MegaCore function.

The MATLAB Simulation File Cannot be Used on UNIX
The MATLAB simulation file generated by a NCO MegaCore function can only be used on Windows and Linux.

Affected Configurations
UNIX configurations.

Design Impact
You cannot simulate a NCO MegaCore function in MATLAB on UNIX.

Workaround
None.

Solution Status
This issue will be fixed in a future version of the NCO MegaCore function.
12. Nios II Processor

Revision History

Table 12–1 shows the revision history for the Nios® II Processor MegaCore® function.

For more information on the new features, refer to the Nios II Processor Reference Handbook. For information about new features and errata in the Nios II Embedded Design Suite, refer to the Nios II Embedded Design Suite Release Notes and Errata.

Table 12–1. Nios II Processor Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>No changes</td>
</tr>
</tbody>
</table>
| 8.0     | May 2008   | ■ Added memory management unit (MMU). Optionally enabled in Nios II MegaWizard® Plug-In Manager flow. Requires third party operating system support.  
          |            | ■ Added memory protection unit (MPU). Optionally enabled in Nios II MegaWizard Plug-In Manager flow. Supported by the Nios II software build tools.  
          |            | ■ Added support for advanced exceptions to catch illegal instructions, illegal memory access, and division errors. |
| 7.2     | October 2007 | Added the jmpi instruction                                                   |

Errata

Table 12–2 shows the issues that affect the Nios II Processor in versions 7.2 through 8.1.

Not all issues affect all versions of the Nios II Processor.

Table 12–2. Nios II Processor Errata

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Affected Version</th>
<th>Issue</th>
<th>8.1</th>
<th>8.0 SP1</th>
<th>8.0</th>
<th>7.2 SP3</th>
<th>7.2 SP2</th>
<th>7.2 SP1</th>
<th>7.2</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Nov 08</td>
<td></td>
<td>Nios II MMU Micro TLBs Not Flushed</td>
<td>Fixed</td>
<td>✓ ✓ ✓</td>
<td>✓</td>
<td>✓ ✓ ✓ ✓</td>
<td>✓ ✓ ✓ ✓</td>
<td>✓ ✓ ✓ ✓</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Cannot Rename Legacy Custom Instruction</td>
<td>✓ ✓ ✓</td>
<td>✓ ✓ ✓ ✓</td>
<td>✓ ✓ ✓ ✓</td>
<td>✓ ✓ ✓ ✓</td>
<td>✓ ✓ ✓ ✓</td>
<td>✓ ✓ ✓ ✓</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Cannot Add Separate Clock Interface to Custom Instruction</td>
<td>✓ ✓ ✓</td>
<td>✓ ✓ ✓ ✓</td>
<td>✓ ✓ ✓ ✓</td>
<td>✓ ✓ ✓ ✓</td>
<td>✓ ✓ ✓ ✓</td>
<td>✓ ✓ ✓ ✓</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Incorrect Memory Usage Report in Nios II MegaWizard Interface</td>
<td>✓ ✓ ✓</td>
<td>✓ ✓ ✓ ✓</td>
<td>✓ ✓ ✓ ✓</td>
<td>✓ ✓ ✓ ✓</td>
<td>✓ ✓ ✓ ✓</td>
<td>✓ ✓ ✓ ✓</td>
<td></td>
</tr>
<tr>
<td>15 Jul 08</td>
<td></td>
<td>Hardware Breakpoints Not Supported with Nios II MMU and MPU</td>
<td>✓ ✓ ✓</td>
<td>✓ ✓ ✓ ✓</td>
<td>✓ ✓ ✓ ✓</td>
<td>✓ ✓ ✓ ✓</td>
<td>✓ ✓ ✓ ✓</td>
<td>✓ ✓ ✓ ✓</td>
<td></td>
</tr>
<tr>
<td>01 Apr 08</td>
<td></td>
<td>Nios II Ports Created Incorrectly</td>
<td>✓ ✓ ✓</td>
<td>✓ ✓ ✓ ✓</td>
<td>✓ ✓ ✓ ✓</td>
<td>✓ ✓ ✓ ✓</td>
<td>✓ ✓ ✓ ✓</td>
<td>✓ ✓ ✓ ✓</td>
<td></td>
</tr>
<tr>
<td>01 Mar 08</td>
<td></td>
<td>Nios II Processor Consumes Extra M9K RAM</td>
<td>✓ ✓ ✓</td>
<td>✓ ✓ ✓ ✓</td>
<td>✓ ✓ ✓ ✓</td>
<td>✓ ✓ ✓ ✓</td>
<td>✓ ✓ ✓ ✓</td>
<td>✓ ✓ ✓ ✓</td>
<td></td>
</tr>
</tbody>
</table>
Table 12–2. Nios II Processor Errata

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>8.1</td>
</tr>
<tr>
<td>15 Oct 07</td>
<td>New Control Register Names Not Listed</td>
<td>——</td>
</tr>
<tr>
<td></td>
<td>Errors Adding Custom Instruction to the Nios II Processor</td>
<td>✓</td>
</tr>
<tr>
<td>01 Jun 06</td>
<td>Double-Precision Floating-Point Operations With Floating-Point Custom Instructions (1)</td>
<td>✓</td>
</tr>
</tbody>
</table>

Note to Table 12–2:
(1) This issue is documented in Appendix D, Floating Point Custom Instructions in the Nios II Custom Instruction User Guide.

Nios II MMU Micro TLBs Not Flushed

The micro translation lookaside buffer (TLB) entries in the Nios II MMU are not always flushed when required. This leads to unpredictable results with software using the MMU.

Affected Configurations

Nios II systems with the MMU enabled.

Workaround

Upgrade to the Quartus II Complete Design Suite version 8.1 or later.

Solution Status

Fixed in version 8.1.

Cannot Rename Legacy Custom Instruction

If you instantiate a new class.ptf-based custom instruction, or upgrade a design containing such a custom instruction, custom instruction name changes will be lost when you close and reopen SOPC Builder. This also affects the system.h file generated by the Nios II software build tools — the original name will continue to appear in system.h.

Affected Configurations

Nios II systems with legacy custom instructions.

Design Impact

Cannot rename custom instruction

Workaround

Upgrade to the Quartus II Complete Design Suite version 8.0 or later.

Solution Status

Fixed in version 8.0.
Cannot Add Separate Clock Interface to Custom Instruction

When adding a custom instruction to a Nios II processor, you can only use the clock provided by the custom instruction interface to clock your custom instruction logic. You cannot define a separate clock interface to clock the logic.

Affected Configurations

Any Nios II system featuring custom instructions.

Design Impact

No impact on existing designs. On new designs, you cannot define a separate clock interface to clock the logic.

Workaround

If your custom instruction logic is sequential in nature, use the clock provided by the custom instruction interface.

Alternatively, upgrade to the Quartus II Complete Design Suite version 8.0 or later.

Solution Status

Fixed in version 8.0.

Incorrect Memory Usage Report in Nios II MegaWizard Interface

The Nios II Processor MegaWizard interface incorrectly specifies Cyclone III and Stratix III estimated memory usage in terms of M4K memory blocks instead of M9K memory blocks.

Affected Configurations

Nios II designs targeting Cyclone III or Stratix III devices.

Design Impact

When the Nios II MegaWizard interface instantiates the processor core, the memory usage report incorrectly labels the core usage as M4K memory blocks, when it is actually M9K memory blocks. This reporting condition is benign and can be ignored.

Workaround

No workaround required.

For details of Cyclone III M9K memory usage, refer to the Cyclone III Device Handbook. For details of Stratix III M9K memory usage, refer to the Stratix III Device Handbook.

Solution Status

Fixed in version 8.0.
Hardware Breakpoints Not Supported with Nios II MMU and MPU

Enabling the MMU and MPU sets the Nios II instruction and data address to 32 bits. The JTAG debug core, however, leaves the address equal to the size of the Nios II instruction and data master address signals. Because of this address size mismatch, data breakpoints can not be set on a virtual address when using the MMU, or set on an address outside the address space when using the MPU.

Affected Configurations
Nios II systems with the MMU or MPU enabled.

Workaround
There is no workaround available at this time.

Solution Status
This issue will be fixed in a future release of the Nios II processor core.

Nios II Ports Created Incorrectly

A threading issue between SOPC Builder and the Nios II MegaWizard occasionally causes HDL file analysis to fail. This creates all ports as std_logic input with width 1.

Affected Configurations
Nios II processor systems with custom instructions.

Design Impact
Design fails to run under ModelSim.

Workaround
After adding your custom instruction, close and relaunch SOPC Builder.

Solution Status
This issue will be fixed in a future release of the Quartus II Complete Design Suite.

Nios II Processor Consumes Extra M9K RAM

The Quartus® II Complete Design Suite v7.2 allocates two M9K RAMs instead of one for internal processor functions.

Affected Configurations
Nios II systems on Cyclone® III and Stratix® III devices.

Design Impact
An extra M9K RAM is allocated.
For most designs, this issue is not expected to affect timing closure.

Workaround
Upgrade to the Quartus II Complete Design Suite version 7.2 SP1 or later.
**Solution Status**
Fixed in version 7.2 SP1.

**New Control Register Names Not Listed**
New control register names, added to the assembler in v7.2, are not documented in the *Nios II Processor Reference Handbook*.

**Affected Configurations**
All Nios II systems.

**Design Impact**
Documentation issue. No impact on designs.

**Workaround**
The new control register names are shown in Table 12–3.

**Table 12–3. New Control Register Names**

<table>
<thead>
<tr>
<th>Control Register</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>pteaddr</td>
</tr>
<tr>
<td>9</td>
<td>tlbacc</td>
</tr>
<tr>
<td>10</td>
<td>tlbmisc</td>
</tr>
</tbody>
</table>

**Solution Status**
Fixed in version 8.0.

**Errors Adding Custom Instruction to the Nios II Processor**
You might get spurious errors after adding custom instruction slave ports through the Nios II MegaWizard interface.

**Affected Configurations**
Any Nios II system featuring custom instructions.

**Design Impact**
No design impact. The error messages are benign.

**Workaround**
Save your system in SOPC Builder. Close and then relaunch SOPC Builder.
Revision History

Table 13–1 shows the revision history for the PCI Compiler MegaCore® function.

For more information on the new features, refer to the PCI Compiler User Guide.

Table 13–1. PCI Compiler Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>Preliminary support for Stratix® IV device family.</td>
</tr>
<tr>
<td>7.2</td>
<td>October 2007</td>
<td>■ Preliminary support for Stratix III device family.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Support for I/O transactions in non-prefetchable bridge data path.</td>
</tr>
</tbody>
</table>

Errata

Table 13–2 shows the issues that affect the PCI Compiler v8.1, 8.0, and 7.2.

Not all issues affect all versions of the PCI Compiler.

Table 13–2. PCI Compiler MegaCore Function Errata

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Nov 08</td>
<td>Designs With Stratix III Devices Fail to Meet Timing</td>
<td>✔</td>
</tr>
<tr>
<td></td>
<td>Designs With Stratix IV Devices Fail to Meet Timing</td>
<td>✔</td>
</tr>
<tr>
<td></td>
<td>Device Support Incorrect in User Guide</td>
<td>Fixed</td>
</tr>
<tr>
<td></td>
<td>Full Compilation Fails for Some Cyclone III Devices When Using Recommended PCI Pin Assignments</td>
<td>Fixed</td>
</tr>
<tr>
<td></td>
<td>STA Timing Analysis Fails for Stratix III Devices When Using Recommended PCI Constraints at Lower Seed Number</td>
<td>Fixed</td>
</tr>
<tr>
<td></td>
<td>STA Timing Analysis Fails for Hardcopy® II Devices When Using Recommended PCI Constraints</td>
<td>Fixed</td>
</tr>
<tr>
<td></td>
<td>STA Timing Analysis Fails for Some Arria GX and Stratix II Devices When Using Recommended PCI Constraints</td>
<td>Fixed</td>
</tr>
<tr>
<td></td>
<td>STA Timing Analysis Fails for Some Cyclone III Devices When Using Recommended PCI Constraints</td>
<td>Fixed</td>
</tr>
<tr>
<td>15 May 08</td>
<td>PCI Bus Hangs on Write Transactions to the I/O BAR Address Spaces</td>
<td></td>
</tr>
</tbody>
</table>

---

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Library Version 8.1

MegaCore IP Library Release Notes and Errata
Designs With Stratix III Devices Fail to Meet Timing
Timing fails when using Stratix III devices with any core combination at 66 MHz.

Affected Configuration
All PCI Compiler designs targeting the Stratix III EP3SL340 device family with the slowest speed grade, C4.

Design Impact
The PCI Compiler designs with some Stratix III devices may fail to meet timing.

Workaround
None.

Solution Status
This issue will not be fixed.

Designs With Stratix IV Devices Fail to Meet Timing
Timing fails when using Stratix IV devices with any core combination at 66 MHz.

Affected Configuration
All PCI Compiler designs targeting the Stratix IV devices with the slowest speed grade, C4.

Design Impact
The PCI Compiler designs with some Stratix IV devices may fail to meet timing.

Workaround
None.

Solution Status
This issue will not be fixed.

Device Support Incorrect in User Guide
The PCI Compiler User Guide 8.0 states an incorrect level of support for the following devices: Arria® GX and Cyclone® III family devices.
The correct device support level is full support.

Solution Status
This issue is fixed in v8.1 of the PCI Compiler User Guide.
Full Compilation Fails for Some Cyclone III Devices When Using Recommended PCI Pin Assignments

A full compilation in the Quartus® II software fails when using the recommended PCI pin assignments for the following Cyclone III devices: EP3C16Q240C8, EP3C25Q240C8, 3C40F780, 3C40Q240C8, and 3C120F780.

The Quartus II software displays the following error message:

Pin <PCI pinout name> is incompatible with I/O bank 1. It uses I/O standard 3.0-V PCI, which has VCCIO requirement of 3.0V. That requirement is incompatible with bank’s VCCIO setting or other output or bidirectional pins in the bank using VCCIO 3.3V.

Affected Configuration

All designs targeting the following Cyclone III devices: EP3C16Q240C8, EP3C25Q240C8, 3C40F780, 3C40Q240C8, and 3C120F780.

Workaround

Use the pin assignments generated during the fitting stage instead of the recommended PCI pin assignments. When adding the PCI constraints, use the option -no_pinouts to omit the recommended PCI pin assignments.

Design Impact

You cannot compile the design.

Solution Status

This issue is fixed in v8.1 of the PCI Compiler.

STA Timing Analysis Fails for Stratix III Devices When Using Recommended PCI Constraints at Lower Seed Number

The STA timing analysis fails for Stratix III devices when using the recommended PCI constraints at lower seed number, and affects both slow and fast timing models.

Affected Configuration

All PCI Compiler designs with Stratix III devices.

Design Impact

The PCI Compiler designs with Stratix III devices may not meet timing requirements.

Workaround

Add one line of additional assignment to the Quartus settings file (.qsf) according to the PCI Compiler core selection.

For MT64:

```
set_instance_assignment -name AUTO_PACKED_REGISTERS_STRATIXII OFF -to "pci_mt64:pci_mt64_inst|pcimt64_pk:parity_Chk|serr_or_*"
```

For MT32:
set_instance_assignment -name AUTO_PACKED_REGISTERS_STRATIXII OFF -to "pci_mt32:pci_mt32_inst|pcimt32_pk:parity_Check|serr_or_*"

For T64:
set_instance_assignment -name AUTO_PACKED_REGISTERS_STRATIXII OFF -to "pci_t64:pci_t64_inst|pcit64_pk:parity_Check|serr_or_*"

For T32:
set_instance_assignment -name AUTO_PACKED_REGISTERS_STRATIXII OFF -to "pci_t32:pci_t32_inst|pcit32_pk:parity_Check|serr_or_*"

**Solution Status**
This issue is fixed in v8.1 of the PCI Compiler.

### STA Timing Analysis Fails for Hardcopy® II Devices When Using Recommended PCI Constraints

The STA timing analysis fails for Hardcopy II devices when using the recommended PCI constraints.

**Affected Configuration**
All PCI Compiler designs with Hardcopy II devices.

**Design Impact**
The PCI Compiler designs with Hardcopy II devices may not meet timing requirements.

**Workaround**
Remove these two lines from the `<project_name/pci_name>.sdc` file before running the STA timing analysis:

```plaintext
set_input_delay -clock PCI_CLOCK -max 0 <reset_signal_name>
set_input_delay -clock PCI_CLOCK -min 100 < reset_signal_name >
```

**Solution Status**
This issue is fixed in v8.1 of the PCI Compiler.

### STA Timing Analysis Fails for Some Arria GX and Stratix II Devices When Using Recommended PCI Constraints

The STA timing analysis fails when using the recommended PCI constraints for the following Arria GX device: 1AGX90EF1152C6 and Stratix II devices: 2S130F780C5, 2S130F1020C5 and 2S130F1508C5, and affects only the slow timing model.

**Affected Configuration**
All PCI Compiler designs targeting the following Arria GX device: 1AGX90EF1152C6 and Stratix II devices: 2S130F780C5, 2S130F1020C5 and 2S130F1508C5.

**Design Impact**
The PCI Compiler designs with some Arria GX and Stratix II devices may not meet timing requirements.
Workaround
Use the fast timing model for STA timing analysis.

Solution Status
This issue is fixed in v8.1 of the PCI Compiler.

STA Timing Analysis Fails for Some Cyclone III Devices When Using Recommended PCI Constraints

The STA timing analysis fails when using the recommended PCI constraints for the following Cyclone III devices: C4F400C7 and C20F324C8.

Affected Configuration
All PCI Compiler designs targeting the following Cyclone III devices: C4F400C7 and C20F324C8.

Design Impact
The PCI Compiler designs with some Cyclone III devices may not meet timing requirements.

Workaround
None.

Solution Status
This issue is fixed in v8.1 of the PCI Compiler.

PCI Bus Hangs on Write Transactions to the I/O BAR Address Spaces

The STA timing analysis fails when using the recommended PCI constraints for the following Cyclone III devices: C4F400C7 and C20F324C8.

Affected Configuration
PCI Compiler using the I/O BAR settings.

Design Impact
Transactions will go to an infinite retry loop whenever a write transaction is initiated to the I/O BAR address space after a read transaction.

Workaround
Apply the patch provided at www.altera.com/support/kdb/solutions/rd04242008_431.html, regenerate your SOPC Builder system and recompile in the Quartus II software. Alternatively, upgrade to v8.0 of the Quartus II software.

Solution Status
This issue is fixed in v8.0 of the PCI Compiler.
Revision History

Table 14–1 shows the revision history for the PCI Express Compiler.

For complete information on the new features, refer to the PCI Express Compiler User Guide.

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>■ Major release. Introduces full support for root port designs in the Stratix® IV GX devices</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Existing 8.0 PCI Express MegaCore functions targeting Stratix IV GX devices must be</td>
</tr>
<tr>
<td></td>
<td></td>
<td>regenerated with the PCI Express 8.1 Compiler prior to compilation in the Quartus® II software</td>
</tr>
<tr>
<td></td>
<td></td>
<td>8.1 or higher.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ The pinout of the 8.1 variant has changed. When regenerating an 8.0 PCI Express variant</td>
</tr>
<tr>
<td></td>
<td></td>
<td>with version 8.1 of the PCI Express Compiler, there are two differences in the application</td>
</tr>
<tr>
<td></td>
<td></td>
<td>signal interface:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>▪ There is a new input pin, gxb_powerdown. The transceiver calibration module uses gxb_powerdown</td>
</tr>
<tr>
<td></td>
<td></td>
<td>in Stratix II GX, Stratix IV GX, and Arria GX devices. It must be grounded if unused.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>▪ The input pin, aer_msi, which is only used for the root port variants, has been removed from</td>
</tr>
<tr>
<td></td>
<td></td>
<td>the top-level of endpoint designs that use the hard IP implementation.</td>
</tr>
<tr>
<td>8.0 SP1</td>
<td>July 2008</td>
<td>■ Maintenance release.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>■ Major release. Introduces a hard IP implementation of the PCI Express Compiler with an Avalon®</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Streaming (Avalon-ST) interface. Provides support for Gen 2 endpoints.</td>
</tr>
<tr>
<td>7.2 SP3</td>
<td>April 2008</td>
<td>■ Maintenance release.</td>
</tr>
<tr>
<td>7.2 SP2</td>
<td>January 2008</td>
<td>■ Maintenance release.</td>
</tr>
<tr>
<td>7.2 SP1</td>
<td>December 2007</td>
<td>■ Corrected error in SOPC Builder Avalon Memory-Mapped (Avalon-MM) base address assignments</td>
</tr>
<tr>
<td>7.2</td>
<td>October 2007</td>
<td>■ Avalon-ST application interface.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Single clock domain for Avalon Memory-Mapped (Avalon-MM) application interface.</td>
</tr>
</tbody>
</table>

Errata

Table 14–2 shows the issues that affect the PCI Express Compiler in v8.1, v8.0, and v7.2.

Not all issues affect all versions of the PCI Express Compiler.
Table 14–2. PCI Express Compiler Errata  (Part 1 of 2)

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Dec 08</td>
<td>License File for Soft IP Implementation of the PCI Express Compiler Does Not Work</td>
<td>8.1 8.0 7.2</td>
</tr>
<tr>
<td></td>
<td>EDA Netlist Writer Does Not Write Netlist for Hard IP Implementation of PCI Express</td>
<td>8.1 8.0 7.2 7.2</td>
</tr>
<tr>
<td>01 Nov 08</td>
<td>PCI Express Stratix IV Projects with Pin Assignments Specified Using the Pin Planner May Fail Quartus II Compilation</td>
<td>8.1 8.0 7.2</td>
</tr>
<tr>
<td></td>
<td>PCI Express Simulation Fails when Using ModelSim AE for Stratix II GX MegaCore Functions with the Avalon-ST or Descriptor/Data Interfaces</td>
<td>8.1 8.0 7.2 7.2</td>
</tr>
<tr>
<td></td>
<td>The Chaining DMA Design Example May Issue DMA Write Requests that Violate the 4 KByte Boundary Rule in the VHDL Version</td>
<td>8.1 8.0 7.2</td>
</tr>
<tr>
<td></td>
<td>Incorrect Connection of SOPC Builder Interrupt Sources to PCI Express Components</td>
<td>8.1 8.0 7.2</td>
</tr>
<tr>
<td></td>
<td>When operating in hardware, the PCI Express design example might require the RC Slave module to be instantiated</td>
<td>8.1 8.0 7.2</td>
</tr>
<tr>
<td></td>
<td>Root Port BFM in version 8.1 of the PCI Express Testbench is not Backwards Compatible</td>
<td>8.1 8.0 7.2</td>
</tr>
<tr>
<td></td>
<td>PCI Express Avalon-MM Tx Interface Deadlocks on a Read Request</td>
<td>Fixed 8.1 8.0 7.2</td>
</tr>
<tr>
<td></td>
<td>Unable to Compile the Example Design Successfully in Quartus II when using ECRC Forwarding</td>
<td>Fixed 8.1 8.0 7.2</td>
</tr>
<tr>
<td>15 Aug 08</td>
<td>Chaining DMA Design Example Forwards Tx ECRC with Incorrect Alignment</td>
<td>Fixed 8.1 8.0 7.2</td>
</tr>
<tr>
<td>15 Jul 08</td>
<td>PCI Express Compiler User Guide Incorrectly Documents the Number of Address Pages</td>
<td>Fixed 8.1 8.0 7.2</td>
</tr>
<tr>
<td></td>
<td>PCI Express Compiler User Guide Incorrectly Documents rx_st_data and tx_st_data in 128-Bit Mode</td>
<td>Fixed 8.1 8.0 7.2</td>
</tr>
<tr>
<td></td>
<td>Address Translation Update Can Corrupt Outstanding Reads for MegaCore Functions Created in SOPC Builder</td>
<td>8.1 8.0 7.2</td>
</tr>
<tr>
<td></td>
<td>SOPC Builder does not Support Legacy Interrupts for PCI Express</td>
<td>— Fixed 8.1 8.0 7.2</td>
</tr>
<tr>
<td></td>
<td>PCI Express MegaCore Function v7.2 Does Not Work with the SOPC Builder SGDMA v7.2</td>
<td>— Fixed 8.1 8.0 7.2</td>
</tr>
<tr>
<td>15 May 08</td>
<td>The Source Synchronous Output Clock Is Improperly Constrained for an External PHY</td>
<td>Fixed 8.1 8.0 7.2</td>
</tr>
<tr>
<td></td>
<td>PCI Express Compiler Does Not Create a Block Symbol File</td>
<td>Fixed 8.1 8.0 7.2</td>
</tr>
<tr>
<td></td>
<td>PCI Express MegaWizard Interface Displays Incorrect Values</td>
<td>Fixed 8.1 8.0 7.2</td>
</tr>
<tr>
<td></td>
<td>Serial Simulation Is Unsuccessful for PCI Express Variants Targeting Stratix GX with refclk at 156.25 MHz</td>
<td>Fixed 8.1 8.0 7.2</td>
</tr>
<tr>
<td>01 Apr 08</td>
<td>PCI Express 7.2 Avalon Streaming (Avalon-ST) Adaptor is not Recalculating Non-Posted tx_cred</td>
<td>— Fixed 8.1 8.0 7.2</td>
</tr>
</tbody>
</table>
## Table 14–2. PCI Express Compiler Errata  (Part 2 of 2)

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 Jan 08</td>
<td>PCI Express User Guide, Version 7.2 is Missing Descriptions for some Avalon-ST Signals</td>
<td>—— SP 8.0 7.2</td>
</tr>
<tr>
<td></td>
<td>PCI Express User Guide, Version 7.2 Lists the Data Bytes in D0, D1 and D2 of rx_st_data and tx_st_data TLPs in the Wrong Order</td>
<td>—— SP 8.0 7.2</td>
</tr>
<tr>
<td>01 Dec 07</td>
<td>ECRC Check and ECRC Generate Are Incorrectly Implemented If Only One Option is Selected</td>
<td>—— SP 8.0 7.2</td>
</tr>
<tr>
<td></td>
<td>SOPC Builder Avalon-MM Base Addresses Assigned Incorrectly for PCI Express BARs</td>
<td>—— SP 8.0 7.2</td>
</tr>
<tr>
<td>01 Nov 07</td>
<td>When Editing an Existing SOPC Builder System, the Bar3 Parameter of the PCI Express Component is Incorrectly Set</td>
<td>—— SP 8.0 7.2</td>
</tr>
<tr>
<td>01 Oct 07</td>
<td>Chaining DMA Design Has Issues in Hardware when RX_BUFFER Is Set to LOW</td>
<td>—— SP 8.0 7.2</td>
</tr>
<tr>
<td></td>
<td>Generation Error—Stratix GX and Stratix II GX Devices</td>
<td>—— SP 8.0 7.2</td>
</tr>
<tr>
<td></td>
<td>VHDL Chaining DMA Example Design Fails to Compile with VCS-MX Simulator</td>
<td>—— SP 8.0 7.2</td>
</tr>
</tbody>
</table>

### License File for Soft IP Implementation of the PCI Express Compiler Does Not Work

The license file for the soft IP version of the PCI Express Compiler in 8.1 does not work.

**Affected Configurations**

This issue affect soft IP implementations of the PCI Express MegaCore in version 8.1 of the Quartus II software.

**Workaround**

The workaround is to download and install Quartus II 8.1 software patch contained in the following .zip file:


**Solution Status**

This issue will be fixed in a future version of the Quartus II software.

### EDA Netlist Writer Does Not Write Netlist for Hard IP Implementation of PCI Express

The Quartus II EDA Netlist Writer does not write a Stratix IV GX functional simulation netlist for the hard IP implementation of the PCI Express MegaCore function because a license file has not been specified. However, the hard IP implementation does not require a license.

**Affected Configurations**

This issue affects hard IP implementations of the PCI Express MegaCore function that in version 8.1 of the Quartus II software.
Workaround
The workaround is to download and install Quartus II 8.1 software patch contained in the following .zip file:

Solution Status
This issue will be fixed in a future release of the Quartus II software.

PCI Express Stratix IV Projects with Pin Assignments Specified Using the Pin Planner May Fail Quartus II Compilation
If you specify pin assignments using the Pin Planner for Stratix IV projects, Quartus II compilation fails.

Affected Configurations
This issue affects PCI Express MegaCore functions that target the Stratix IV family.

Workaround
Change the definition for the IO standard for the transceivers from 1.2 V PCML (pseudo current mode logic) to 1.4 V PCML.

Solution Status
This issue will be fixed in a future release of the Quartus II software.

PCI Express Simulation Fails when Using ModelSim AE for Stratix II GX MegaCore Functions with the Avalon-ST or Descriptor/Data Interfaces
If you simulate PCI Express MegaCore functions that use the Avalon-ST or descriptor/data interface and target Stratix II GX devices using ModelSim® AE, you get a compilation error.

Affected Configurations
This issue affects PCI Express MegaCore functions written in Verilog HDL that use the Avalon-ST or descriptor/data interface and target a Stratix II GX device.

Workaround
In the <variation_name>_examples/chaining_dma/testbench/sim_filelist file, modify the line specifying <variation_name>_serdes.v to specify <variation_name>_serdes.vo.

Solution Status
This issue will be fixed in a future version of the Quartus II software.
The Chaining DMA Design Example May Issue DMA Write Requests that Violate the 4 KByte Boundary Rule in the VHDL Version

The VHDL version of the chaining DMA design example may issue DMA writes that violate the 4 KByte boundary. If a request crosses the 4 KByte boundary, the DMA data is thrown away. Because there is no data checking in the version 8.1 test driver, the simulation does not fail.

Affected Configurations
This issue affects the VHDL version of the chaining DMA design example for 8.1.

Workaround
You can modify the test driver, altpcietb_bfm_driver_chaining.vhd, so that the write DMA does not transfer data across 4 KByte addresses.

Solution Status
This issue will be fixed in a future version of the PCI Express Compiler design example.

Incorrect Connection of SOPC Builder Interrupt Sources to PCI Express Components

In SOPC Builder systems containing a PCI Express component which masters interrupt senders on the other side of an Avalon-MM pipeline bridge or clock-crossing bridge, interrupt sources are not correctly wired to the PCI express component.

Affected Configurations
This issue affects PCI Express Compiler instances used in SOPC Builder systems containing an Avalon-MM pipeline bridge or clock-crossing bridge.

Workaround
Ensure that there is not an Avalon-MM pipeline bridge or clock-crossing bridge master between the PCI Express Rx master port and its slaves which produce interrupts.

Solution Status
This issue will be fixed in a future version of the PCI Express Compiler.

When operating in hardware, the PCI Express design example might require the RC Slave module to be instantiated

The default configuration of the Altera®-provided design example described in the Testbench chapter of the PCI Express Compiler User Guide does not instantiate the RC Slave module. The RC Slave module acknowledges message TLPs and zero-length memory read TLPs from the root complex. Typically, commercial BIOS’s issue message TLPs; therefore, if you do not instantiate the RC Slave module in this design example, your hardware system may stall indefinitely.
**Affected Configurations**

This issue affects designs that use the PCI Express Development Kit and are recompiling the hardware design example with the 7.2 or 8.0 version of the PCI Express Compiler.

**Workaround**

Enable the RC Slave module when connecting to a commercial PCI Express platform.

**Solution Status**

This issue will be fixed in a future version of the Quartus® II software.

---

**Root Port BFM in version 8.1 of the PCI Express Testbench is not Backwards Compatible**

Testbenches for PCI Express MegaCore® functions generated in version 8.0 or earlier of the Quartus II software fail in version 8.1 of the Quartus II software.

**Affected Configurations**

This issue affects existing PCI Express MegaCore functions generated using version 8.0 or earlier of the PCI Express Compiler if you have upgraded to Quartus II 8.1 and want regenerate the testbench using the Quartus II 8.1 software.

**Workaround**

If your design targets the Stratix IV family, you must regenerate your PCI Express MegaCore function using version 8.1 of the PCI Express Compiler.

If your design targets other device families, a workaround is to modify the `runtb.do` file in the testbench directory. Edit all lines that contain `stratixiv` to point to version 8.0 of the Altera MegaCore IP Library.

- **Example 14–1** shows the original and modified version for VHDL.

  **Example 14–1. Modifications for runtb.do—VHDL**

```vhd
# This is the original line that uses the QUARTUS_ROOTDIR variable
vcom -work stratixiv_pcie_hip $env(QUARTUS_ROOTDIR)/eda/sim_lib/stratixiv_pcie_hip_components.vhd

# This edited version points to version 8.0 of the Altera IP library
vcom -work stratixiv_pcie_hip c:/altera/80/quartus/eda/sim_lib/stratixiv_pcie_hip_components.vhd
```

- **Example Example 14–2** shows the original and edited versions for Verilog HDL.

  **Example 14–2. Modifications for runtb.do—Verilog HDL**

```verilog
# This is the original line that uses the QUARTUS_ROOTDIR variable
vlog -work stratixiv_hssi $env(QUARTUS_ROOTDIR)/eda/sim_lib/stratixiv_hssi_atoms.v

#This edited version points to version 8.0 of the Altera IP Library
vlog -work stratixiv_hssi c:/altera/80/quartus/eda/sim_lib/stratixiv_hssi_atoms.v
```
Solution Status
This issue is the result of incompatibilities between the high-speed serial interface (HSSI) design for version 8.1 of the Quartus II software and earlier versions. These incompatibilities cannot be resolved.

PCI Express Avalon-MM Tx Interface Deadlocks on a Read Request
When the Rx completion buffer is almost fully allocated, a new read might be sent even if there is not enough space in the buffer to store the read data. When this new read is sent, the read credit counter rolls over erroneously indicating that buffer space is available and the buffer overflows. Eventually, the Avalon Tx interface deadlocks on a read request because the waitrequest signal is asserted.

Affected Versions
This issue affects versions 8.0 of the PCI Express Compiler and earlier that use the SOPC Builder design flow.

Workaround
There is no workaround for this issue; however, it is fixed in version 8.1 of the PCI Express Compiler.

Solution Status
This issue is fixed in version 8.1 of the PCI Express Compiler.

Unable to Compile the Example Design Successfully in Quartus II when using ECRC Forwarding
For Stratix IV PCI Express variations that enable ECRC forwarding, compilation of the example design may fail because the included version of the CRC Compiler variation is not enabled for the Stratix IV device family.

Affected Configurations
This issue occurs in version 8.0 of the PCI Express Compiler if you do not have a license for the 8.0 CRC Compiler and you are creating a Stratix IV variant of the PCI Express MegaCore function that uses ECRC forwarding.

Workaround
You can complete the following these steps to edit the CRC Compiler variation created in your design example directory to update it to 8.0:
1. Open the Quartus II project that contains the design example.
2. Launch MegaWizard Plug-In Manager from the Tools menu.
3. Select Edit an existing custom megafunction variation.
4. Click Next.
5. Select atpciedr_rx_ecrc_64.v or .vhd or atpciedr_rx_ecrc_128.v if using Avalon Streaming (Avalon-ST) 128.
6. In the Megafuction name list, select CRC Compiler 8.0.
7. Click Next.
8. Click Next.
9. Click Finish.
10. Repeat steps 5–9 for atpcierd_tx_ecrc_64.v or .vhd or atpcierd_tx_ecrc_128.v if using Avalon-ST 128.

**Solution Status**
This is fixed in version 8.1 of the PCI Express Compiler.

### Chaining DMA Design Example Forwards Tx ECRC with Incorrect Alignment
The chaining DMA design example incorrectly aligns the Tx ECRC, appending the ECRC to the dword immediately following the header regardless of address alignment, when the TLP does not include a payload data. The alignment is incorrect in two cases:

- With four dword headers, non-qword aligned addressing, and no payload data
- With three dword header, qword aligned addressing, and no payload data.

For packets with payload, the ECRC should be appended to the end as an extra dword of payload. For packets without payload, the ECRC field should follow address alignment as if it were a one dword payload.

**Affected Configurations**
This issue effects the chaining DMA design example, not variants of the PCI Express MegaCore function.

**Workaround**
The out-of-the-box simulation example does not cause a simulation failure. If you have modified the simulation to use four dword headers, then you must modify the chaining DMA example code to correct the alignment.

**Solution Status**
This issue is fixed in version 8.1 of the PCI Express Compiler.

### PCI Express Compiler User Guide Incorrectly Documents the Number of Address Pages
Table 3-6 of the *PCI Express Compiler User Guide* incorrectly states the choices for the Number of address pages. The correct number of pages available is $2^n$ from 1–512.

**Affected Configurations**
This is a documentation error only.

**Workaround**
No workaround is required.

**Solution Status**
This issue is fixed in version 8.1 of the *PCI Express Compiler User Guide*. 
PCI Express Compiler User Guide Incorrectly Documents rx_st_data and tx_st_data in 128-Bit Mode

In 128-bit mode, the qwords in the timing diagrams are swapped. The correct order for Rx or Tx data[127:0] is {H3, H2, H1, H0}. The PCI Express Compiler User Guide shows data[127:0] as {H1, H0, H3, H2}. In addition, the rx_st_empty0 and tx_st_empty0 signals indicate that the TLP ends in the lower words of data. The corrected diagrams and text are given here.

**Figure 14–1** shows the mapping of 128-bit Avalon-ST Rx packets to PCI Express TLPs for TLPs with a three dword header and qword aligned addresses.

**Figure 14–2** shows the mapping of 128-bit Avalon-ST Rx packets to PCI Express TLPs for TLPs with a 3 dword header and non-qword aligned addresses.

**Figure 14–3** shows the mapping of 128-bit Avalon-ST Rx packets to PCI Express TLPs for a four dword header with non-qword aligned addresses. In this example, rx_st_empty is low because the data ends in the upper 64 bits of rx_st_data.
Figure 14–4 shows the mapping of 128-bit Avalon-ST Rx packets to PCI Express TLPs for a four dword header with qword aligned addresses.

Figure 14–5 shows the mapping of 128-bit Avalon-ST Tx packets to PCI Express TLPs for a three dword header with qword aligned addresses.

Figure 14–6 shows the mapping of 128-bit Avalon-ST Tx packets to PCI Express TLPs for a 3 dword header with non-qword aligned addresses.
Figure 14–7 shows the mapping of 128-bit Avalon-ST Tx packets to PCI Express TLPs for a four dword header TLP with non-qword aligned addresses. In this example, \texttt{tx\_st\_empty} is low because the data ends in the upper 64 bits of \texttt{tx\_st\_data}.

**Affected Configurations**

This is a documentation error only.

**Workaround**

No workaround is required.

**Solution Status**

This issue is fixed in version 8.1 of the *PCI Express Compiler User Guide*. 
Address Translation Update Can Corrupt Outstanding Reads for MegaCore Functions Created in SOPC Builder

When an Avalon-MM master sends a request larger than the PCI Express Maximum payload size to the Tx slave port, the MegaCore function converts this large request into multiple PCIe requests of smaller size, depending on address boundaries and size. For each smaller payload packet sent, the address translation table is accessed to generate the address field of the packet. This process takes a number of clock cycles, and during that time, if the translation table entry is altered, the subsequent smaller request packets have the wrong address.

For write requests, it is safe to change the entry associated with a DMA after the last data is accepted for write. For read requests, it is safe to change the table entry after the first data for a DMA is returned. You should rotate among multiple entries in the Avalon-MM to PCIe address translation table in order to support more than one outstanding read request.

Affected Configurations

This issue affects PCI Express applications created in SOPC Builder.

Workaround

You must use the address translation tables as described in this errata.

Solution Status

This issue will be documented in a future version of the PCI Express Compiler User Guide.

SOPC Builder does not Support Legacy Interrupts for PCI Express

PCI Express applications created in SOPC Builder that run on top of Windows XP do not support legacy interrupts. Windows XP does not support MSI; consequently, no interrupt mechanism is available for these applications.

Affected Configurations

This issue affects PCI Express applications created in SOPC Builder that run on top of Windows XP.

Workaround

Two possible workarounds are to change to Windows Vista which supports MSI interrupts or use the PCIe Avalon-ST interface which supports legacy interrupts.

Solution Status

This issue is fixed in PCI Express Compiler version 8.0 SP1. The SOPC Builder PCI Express component will now use either MSI or Legacy interrupts automatically based on the standard interrupt controls in the PCI Express configuration space registers. The Interrupt Disable bit, which is bit 10 of the Command register, can be used to disable legacy interrupts. The MSI enable bit, which is bit 0 of the Message Control register in the MSI capability, can be used to enable MSI interrupts. Only one type of interrupt can be enabled at a time.
**PCI Express MegaCore Function v7.2 Does Not Work with the SOPC Builder SGDMA v7.2**

This issue is due to the Avalon-MM burst support capabilities of the Scatter-Gather DMA (SG-DMA).

**Affected Configurations**

This issue occurs when using the PCI Express MegaCore function v7.2 in SOPC Builder with the 7.2 SG-DMA.

**Workaround**

Use PCI Express v8.0 with the 8.0 SG-DMA component.

**Solution Status**

This issue is fixed in PCI Express Compiler version 8.0.


<table>
<thead>
<tr>
<th>Signal</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>cpl_err[5:4]</td>
<td>I</td>
<td>Completion error. This signal reports completion errors to the configuration space.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ cpl_err[5]: Unsupported request error for non-posted TLP. Used in soft IP Avalon-ST interface and the hard IP implementation.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ cpl_err[4]: Unsupported request error for posted TLP. Used in soft IP Avalon-ST interface and the hard IP implementation.</td>
</tr>
</tbody>
</table>

**Affected Configurations**

This is a documentation error only.

**Workaround**

No workaround is required.

**Solution Status**

This error will be fixed in a future version of the PCI Express Compiler User Guide.

**The Source Synchronous Output Clock Is Improperly Constrained for an External PHY**

For an external PHY, the source synchronous output clock is not constrained to be placed in an IO buffer.

**Affected Configurations**

This issue affects all PHYs with an output PIPE clock.

**Workaround**

Add the following constraint to the Quartus II Settings File (.qsf) for your project:

```
set_instance_assignment -name FAST_OUTPUT_REGISTER ON -to pipe_txclk
```
Solution Status
This issue will be fixed in a future version of the PCI Express Compiler.

PCI Express Compiler Does Not Create a Block Symbol File
The PCI Express Compiler does not automatically create a Block Symbol File (.bsf) for the PCI Express MegaCore function.

Affected Configurations
This issue affects all PCI Express MegaCore function variations in 8.0.

Workaround
You can use the Quartus II Block Editor to manually create a .bsf for the variation. Alternatively, you can use the quartus_map API at the command line to create a symbol, by typing the following command:

```
quartus_map --generate_symbol=<variation_name>.<v|vhd> <quartus II project name>
```

Solution Status
This issue will be fixed in a future version of the PCI Express Compiler.

PCI Express MegaWizard Interface Displays Incorrect Values
PCI Express MegaWizard Interface displays incorrect values for the Credit Display Table of Buffer Setup Page when the Hard IP Implementation is Selected. The displayed Rx Buffer Space Allocation (per VC) table displays incorrect values for the hard IP implementation of the PCI Express MegaCore function. Table 14–4 lists the correct values. The Desired performance for received requests setting has no effect. The credit allocations for the hard IP implementation are set to the values indicated in Table 14–4.

<table>
<thead>
<tr>
<th>Credit Type</th>
<th>Number of Credits</th>
<th>Space Used (in Bytes)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Without ECRC Forwarding</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Posted header credit</td>
<td>50</td>
<td>800</td>
</tr>
<tr>
<td>Posted data credit</td>
<td>360</td>
<td>5760</td>
</tr>
<tr>
<td>Non-posted header credit</td>
<td>54</td>
<td>864</td>
</tr>
<tr>
<td>Completion header credit</td>
<td>112</td>
<td>1792</td>
</tr>
<tr>
<td>Completion data credit</td>
<td>448</td>
<td>7168</td>
</tr>
<tr>
<td>Total header credits</td>
<td>216</td>
<td>—</td>
</tr>
<tr>
<td>Rx buffer size</td>
<td>—</td>
<td>16384</td>
</tr>
<tr>
<td><strong>With ECRC Forwarding</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Posted header credit</td>
<td>50</td>
<td>1200</td>
</tr>
<tr>
<td>Posted data credit</td>
<td>336</td>
<td>5375</td>
</tr>
<tr>
<td>Non-posted header credit</td>
<td>54</td>
<td>1296</td>
</tr>
</tbody>
</table>
**Table 14–4. Rx Buffer Space Allocation (per VC) Hard IP Implementation**

<table>
<thead>
<tr>
<th>Credit Type</th>
<th>Number of Credits</th>
<th>Space Used (in Bytes)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Completion header credit</td>
<td>112</td>
<td>1792</td>
</tr>
<tr>
<td>Completion data credit</td>
<td>420</td>
<td>6720</td>
</tr>
<tr>
<td>Total header credits</td>
<td>216</td>
<td>—</td>
</tr>
<tr>
<td>Rx buffer size</td>
<td>—</td>
<td>16384</td>
</tr>
</tbody>
</table>

**Affected Configurations**

The Rx Buffer Space Allocation information is incorrect for the hard IP implementation of the PCI Express MegaCore function which is available in Stratix® IV GX devices.

**Workaround**

Refer to Table 14–4 for the correct values for Rx buffer space allocation.

**Solution Status**

This issue is fixed in version 8.1 of the PCI Express Compiler.

---

**Serial Simulation Is Unsuccessful for PCI Express Variants Targeting Stratix GX with refclk at 156.25 MHz**

Serial simulation fails because the root port bus functional model (BFM) cannot decode the serial data coming from the device under test (DUT).

**Affected Configurations**

All PCI Express MegaCore variants using the Stratix GX PHY of any lane width with refclk at 156.25 MHz. This issue does not affect Stratix GX PHYs that use a refclk at 100 MHz or 125 MHz.

**Workaround**

There is no workaround.

**Solution Status**

This issue will be fixed in a future version of the PCI Express Compiler.

---

**PCI Express 7.2 Avalon Streaming (Avalon-ST) Adaptor is not Recalculating Non-Posted tx_cred**

tx_cred does not account for non-posted credits which are consumed by non-posted requests already in the Tx FIFO. If subsequent non-posted requests are transferred across the Avalon-ST Tx interface based solely on the tx_cred value, they may sit in the Tx FIFO waiting for additional non-posted credits to be received.

**Affected Configurations**

This issue affects PCI Express version 7.2 when using the Avalon-ST interface. PCI Express versions 7.1 and earlier are not affected.
Workaround
If the non-posted credits are being used to reorder packets, then you should check for sufficient credits on `tx_cred` when the Tx FIFO is empty (`tx_fifo_empty` is high) before sending more non-posted requests.

Solution Status
This issue is fixed in PCI Express Compiler version 8.0.

PCI Express User Guide, Version 7.2 is Missing Descriptions for some Avalon-ST Signals
A number of signals that are part of the Avalon-ST interface were omitted from version 7.2 of the PCI Express Compiler User Guide. These signals are included in v8.0 of the PCI Express Compiler User Guide.

Affected Configurations
This is a documentation error only.

Workaround
No workaround is required.

Solution Status
These signals are included in v8.0 of the PCI Express Compiler User Guide.

PCI Express User Guide, Version 7.2 Lists the Data Bytes in D0, D1 and D2 of rx_st_data and tx_st_data TLPs in the Wrong Order
The following tables show incorrect composition of D0 - D2:

- Table 4-30: rx_st Cycle Definition for 3, Doubleword Header Non-Quadword Aligned Packets
- Table 4-31: rx_st_data0 Cycle Definitions for 3 Dataword Header, Quadword Aligned Packets and All 4 Dataword Header Packets
- Table 4-33: tx_st_data Cycle Definition for 3 Doubleword Header, Non-Quadword Aligned Packets

The correct composition of D0 - D2 is as follows:

D0 = {pcie_data_byte3, pcie_data_byte2, pcie_data_byte1, pcie_data_byte0}
D1 = {pcie_data_byte7, pcie_data_byte6, pcie_data_byte5, pcie_data_byte4}
D2 = {pcie_data_byte11, pcie_data_byte10, pcie_data_byte9, pcie_data_byte8}

Affected Configurations
This is a documentation error only.

Workaround
No workaround is required.
Solution Status
This error is fixed in v8.0 of the PCI Express Compiler User Guide.

ECRC Check and ECRC Generate Are Incorrectly Implemented If Only One Option is Selected

When the Implement advanced error reporting is selected on the Capabilities tab, the Implement ECRC check option and Implement ECRC generation option are improperly implemented if only one of the two options is selected.

Affected Configurations
This issue affects all configurations.

Workaround
Either choose either both or neither of the Implement ECRC check and Implement ECRC generation options.

Solution Status
This is fixed in v8.0 of the PCI Express Compiler.

SOPC Builder Avalon-MM Base Addresses Assigned Incorrectly for PCI Express BARs

When using the PCI Express Compiler with the SOPC Builder design flow the Avalon-MM base addresses used in the PCI Express to Avalon-MM address translations are assigned incorrectly. The incorrect assignment results in received PCI Express memory read and write transactions being converted to Avalon-MM read and write transactions with incorrect Avalon-MM addresses.

Affected Configurations
All PCI Express variations used in the SOPC Builder design flow can be affected.

Workaround
There is no workaround for this issue.

Solution Status
This issue is fixed in v7.2 of the PCI Express Compiler.

When Editing an Existing SOPC Builder System, the Bar3 Parameter of the PCI Express Component is Incorrectly Set

SOPC Builder displays the following erroneous warning message when opening an SOPC Builder system that contains a PCI Express component using BAR3:

"Warning: PCIExpress_CORE: bar3_Non_Prefetchable: BAR settings do not allow full access to the mapped Avalon slaves. Avalon size is hardcoded to > 31 bits and Avalon Base Address is 0x00000000 in PCI Express Compiler settings."
Affected Configurations
This issue affects PCI Express versions 7.1 and 7.2 when using the Avalon-MM interface in SOPC Builder and opening an existing SOPC Builder system that contains a PCI Express component using BAR3.

Workaround
In the System Settings tab of the PCI Express Compiler MegaWizard interface, click on the BAR Size column for BAR3 which is set to Auto and then click Finish. These actions cause BAR3 to be set to Auto. After correcting the setting for BAR3, the warning message is eliminated and system generation is successful.

Solution Status
This issue is fixed in PCI Express Compiler version 8.0.

Chaining DMA Design Has Issues in Hardware when RX_BUFFER Is Set to LOW
When using the chaining DMA design example you may experience intermittent DMA read failures in hardware. Received completions may overrun the space allocated in the Rx Buffer causing corruption of completion or write request packets.

Affected Configurations
This failure may occur when the receive buffer’s Desired performance for received completions is set to Low or Medium.

Workaround
To avoid these intermittent failures Altera recommends that you use the following Rx buffer Space Allocation settings:

Desired performance for received completions: High or Maximum

Solution Status
This issue is fixed in PCI Express Compiler version 8.0.

Generation Error—Stratix GX and Stratix II GX Devices
When generating a third-party timing and resource estimation model for a PCI Express configuration that uses the Stratix GX or Stratix II GX PHY, generation fails if the device family is not also set to Stratix GX or Stratix II GX.

The following error is returned:

Error: dsfsd: HDL generation failed
Info: dsfsd: Third-party timing and resource estimation model creation failed. The following error was returned:
Error: Assertion error: Megafunction altgxb is currently not supporting Stratix II logic family File: c:/altera/70/quartus/libraries/megafunctions/altgxb.tdf Line: 605

Affected Configurations
All variations of the PCI Express compiler that use an internal PHY.
Workaround
Select the appropriate device family in the MegaWizard Plug-In Manager before launching the PCI Express MegaWizard.

Solution Status
This issue is fixed in PCI Express Compiler version 8.0.

VHDL Chaining DMA Example Design Fails to Compile with VCS-MX Simulator

The chaining DMA example design fails to compile with the Synopsys VCS-MX simulator when using the VHDL language. Several of the chaining DMA design files produce errors, all referring to the use of the CONV_STD_LOGIC_VECTOR function as a case statement choice. Because the CONV_STD_LOGIC_VECTOR function is not locally static it should not be used as a case statement choice. Other tested VHDL simulators only issue a warning about these constructs but otherwise produce the intended results in simulation. The intended result is also obtained when compiling in the Quartus II software.

Affected Configurations
The Chaining DMA example design in VHDL for all variations have this issue.

Design Impact
None.

Workaround
The Simple DMA example design does not have this issue and can be used to simulate the basic operation of the PCI Express function. The affected lines of the Chaining DMA example design can also be modified by replacing the CONV_STD_LOGIC_VECTOR function calls with a newly defined constant STD_LOGIC_VECTOR of the correct bit width.

For example in the file altpcie_dma_prg_reg.vhd after the definitions of the IDLE, RX_WS_STATE, RX_ACK_STATE, and HEADER_DESCR_UPD constants add the following new constant definitions:

```
class IDLE_VEC : std_logic_vector(2 downto 0) := "000";
class RX_WS_STATE_VEC : std_logic_vector(2 downto 0) := "001";
class RX_ACK_STATE_VEC : std_logic_vector(2 downto 0) := "010";
class HEADER_DESCR_UPD_VEC : std_logic_vector(2 downto 0) := "011";
```

Then, in the CASE cstate IS statement replace all of the WHEN clauses that look like this:

```
WHEN CONV_STD_LOGIC_VECTOR(IDLE, 3) =>
WHEN CONV_STD_LOGIC_VECTOR(RX_WS_STATE, 3) =>
WHEN CONV_STD_LOGIC_VECTOR(RX_ACK_STATE, 3) =>
WHEN CONV_STD_LOGIC_VECTOR(HEADER_DESCR_UPD, 3) =>
```

With new WHEN clauses using the newly defined vector constants:

```
WHEN IDLE_VEC =>
WHEN RX_WS_STATE_VEC =>
WHEN RX_ACK_STATE_VEC =>
WHEN HEADER_DESCR_UPD_VEC =>
```
You must make similar modifications in the other affected files: 
altpcie_dma_descriptor.vhd, altpcie_rc_slave.vhd, 
altpcie_read_dma_requester.vhd, and altpcie_write_dma_requester.vhd.

Solution Status

This issue is fixed in PCI Express Compiler version 8.0.
15. POS-PHY Level 2 and 3 Compiler

Revision History

Table 15–1 shows the revision history for the POS-PHY Level 2 and 3 Compiler.

For more information on the new features, refer to the POS-PHY Level 2 and 3 Compiler User Guide.

Table 15–1. POS-PHY Level 2 and 3 Compiler Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>Full support for Stratix® III devices.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>■ Full support for Cyclone® III devices</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Preliminary support for Stratix IV devices</td>
</tr>
<tr>
<td>7.2</td>
<td>October 2007</td>
<td>Maintenance release.</td>
</tr>
</tbody>
</table>

Errata

Table 15–2 shows the issues that affect the POS-PHY Level 2 and 3 Compiler v8.1, 8.0, and 7.2.

Not all issues affect all versions of the POS-PHY Level 2 and 3 Compiler.

Table 15–2. POS-PHY Level 2 and 3 Compiler Errata

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Oct 07</td>
<td>Missing Timescale Directive in NativeLink Verilog HDL Testbench</td>
<td>✔ ✔ ✔</td>
</tr>
<tr>
<td></td>
<td>Compilation Error in NativeLink VHDL Flow for NCSim</td>
<td>✔ ✔ ✔</td>
</tr>
<tr>
<td>01 Dec 06</td>
<td>IP Toolbench Incorrect Behavior</td>
<td>✔ ✔ ✔</td>
</tr>
<tr>
<td></td>
<td>Errors with Pin Planner Top-Level File</td>
<td>✔ ✔ ✔</td>
</tr>
</tbody>
</table>

Missing Timescale Directive in NativeLink Verilog HDL Testbench

There is a timescale directive missing from the top-level Verilog HDL testbench.

Affected Configurations

This issue affects the example testbench for NativeLink simulation using VCS MX.

Design Impact

The testbench does not compile.
Workaround
Edit the `\sim_lib\testbench\verilog\auk_pac_mtx_ref_tb.v` file and add the following directive:
```
timescale 1ns / 1ns
```

Solution Status
This issue will be fixed in a future version of the POS-PHY Level 2 and 3 Compiler.

Compilation Error in NativeLink VHDL Flow for NCSim
There is a compilation error due an error in the file declaration format.

Affected Configurations
This issue affects NCSim simulation for the VHDL flow.

Design Impact
NCSim simulation does not work for the VHDL flow.

Workaround
The incorrect declaration lines are not required and can be commented out:
- Edit the `\sim_lib\testbench\vhdl\auk_pac_mtx_ref_tb.vhd` file and comment out lines 128 and 461.
- Edit the `\sim_lib\testbench\vhdl\auk_pac_mrx_ref_tb.vhd` file and comment out lines 130 and 474.

Solution Status
This issue will be fixed in a future version of the POS-PHY Level 2 and 3 Compiler.

IP Toolbench Incorrect Behavior
In the IP Toolbench Parameterize window, after you click Finish, if you click Parameterize to review your settings, the options show incorrect behavior.

Affected Configurations
This issue affects all configurations.

Design Impact
There is no design impact.

Workaround
When you click Finish, ensure you close IP Toolbench (which cancels any changes) or click Generate. You can view the parameterize window again by reopening IP Toolbench.

Solution Status
This issue will be fixed in a future version of the POS-PHY Level 2 and 3 Compiler.
Errors with Pin Planner Top-Level File

When you compile a Quartus® II Pin Planner-generated top-level file you receive errors.

Affected Configurations
This issue affects all configurations.

Design Impact
The design does not compile.

Workaround
Do not use Pin Planner with the POS-PHY Level 2 and 3 Compiler.

Solution Status
This issue will be fixed in a future version of the POS-PHY Level 2 and 3 Compiler.
Revision History

Table 16–1 shows the revision history for the POS-PHY Level 4 MegaCore® function.

For more information on the new features, refer to the POS-PHY Level 4 MegaCore Function User Guide.

Table 16–1. POS-PHY Level 4 MegaCore Function Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.1</td>
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<td>8.0</td>
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<td>■ Full support for Cyclone® III devices</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Preliminary support for Stratix IV devices</td>
</tr>
<tr>
<td>7.2</td>
<td>October 2007</td>
<td>■ Improved output files organization</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Improved user guide</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Improved VHDL simulation support</td>
</tr>
</tbody>
</table>

Errata

The following sections address known errata and documentation issues for the POS-PHY Level 4 MegaCore function. Errata are functional defects or errors, which may cause the POS-PHY Level 4 MegaCore function to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

Table 16–2 shows the issues that affect the POS-PHY Level 4 MegaCore function v8.1, 8.0, and 7.2.

Not all issues affect all versions of the POS-PHY Level MegaCore function.

Table 16–2. POS-PHY Level 4 MegaCore Function Errata

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Sep 08</td>
<td>Incorrect Description of DIP-4 Out of Service Indication in User Guide</td>
<td>✅ ✅ ✅</td>
</tr>
<tr>
<td>15 Aug 08</td>
<td>Valid Range of Full Threshold High is Incorrect</td>
<td>✅ ✅ ✅</td>
</tr>
<tr>
<td>15 May 08</td>
<td>Errors when Editing Transmitters v7.2 or Earlier in v8.0</td>
<td>✅ ✅ —</td>
</tr>
<tr>
<td></td>
<td>Transmitter Sends Extra Idles with Burst Limit Enable</td>
<td>✅ ✅ —</td>
</tr>
<tr>
<td></td>
<td>Missing Constraint</td>
<td>✅ ✅ —</td>
</tr>
<tr>
<td></td>
<td>Training Interval is Greater than Specified</td>
<td>✅ ✅ —</td>
</tr>
<tr>
<td></td>
<td>Signal stat_rd_dip4_oos Goes to X in Simulation</td>
<td>— Fixed ✅</td>
</tr>
</tbody>
</table>
Table 16–2. POS-PHY Level 4 MegaCore Function Errata

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 May 07</td>
<td>Irrelevant Signals: <code>err_ry_msop*</code> &amp; <code>err_ry_meop*</code></td>
<td>☑    ☑    ☑</td>
</tr>
<tr>
<td></td>
<td>Warning Message: Pin ‘err_rd_dpa’ Stuck at GND</td>
<td>☑    ☑    ☑</td>
</tr>
<tr>
<td></td>
<td>IP Toolbench Error After Changing the Device Family</td>
<td>☑    ☑    ☑</td>
</tr>
<tr>
<td></td>
<td>IP Toolbench Fails to Generate IP Functional Simulation Models for HardCopy Stratix Devices</td>
<td>☑    ☑    ☑</td>
</tr>
<tr>
<td></td>
<td>IP Toolbench Generation Fails if the Generation Is Cancelled and Restarted</td>
<td>☑    ☑    ☑</td>
</tr>
</tbody>
</table>

Incorrect Description of DIP-4 Out of Service Indication in User Guide

The following paragraph is incorrect in the *DIP-4 Out of Service* section in the *POS-PHY Level 4 MegaCore Function User Guide*:

If the receiver is in service (the `stat_rd_dip4_oos` is low) and one or more DIP-4 errors are detected (up to 8 in 128-bit mode) in the current `rdint_clk` cycle, the bad counter is incremented. If the bad counter reaches the `bad_level` threshold, the receiver goes out of service by asserting the `stat_rd_dip4_oos` signal. If all of the DIP-4s received in the current cycle are good, the bad counter is cleared. If no control words are received, nothing happens.

The following paragraph is correct:

If the receiver is in service (the `stat_rd_dip4_oos` is low) and one or more DIP-4 errors are detected (up to 8 in 128-bit mode) in the current `rdint_clk` cycle, the bad counter is incremented. If the bad counter reaches the `bad_level` threshold, the receiver goes out of service by asserting the `stat_rd_dip4_oos` signal. If any of the DIP-4s received in the current cycle are good, the bad counter is cleared. If no control words are received, nothing happens.

In particular, the following sentence has the incorrect “all” replaced by the correct “any”:

If any of the DIP-4s received in the current cycle are good, the bad counter is cleared.

The following paragraph in the *Receiver Options* section is incorrect in a similar way:

If the `stat_rd_dip4_oos` signal is low, and any of the DIP-4s in the control words received in the current clock cycle (up to 8 in 128-bit mode) are errored, the bad counter is incremented by 1; otherwise it is reset to 0. If the bad counter reaches the `bad_level` threshold, the `stat_rd_dip4_oos` flag is asserted. A `bad_level` of 0 is invalid.

The following paragraph is correct:

If the `stat_rd_dip4_oos` signal is low, and all of the DIP-4s in the control words received in the current clock cycle (up to 8 in 128-bit mode) are errored, the bad counter is incremented by 1; otherwise it is reset to 0. If the bad counter reaches the `bad_level` threshold, the `stat_rd_dip4_oos` flag is asserted. A `bad_level` of 0 is invalid.
**Figure 16–1** shows an example of the DIP-4 counter, where the receiver is in service state and bad threshold is 3.

**Affected Configurations**

This issue affects all receiver configurations.

**Design Impact**

The core may need to receive more control word DIP-4 errors than the **DIP-4 Bad Threshold** parameter set in the wizard for `stat_rd_dip4_oos` to go high.

**Solution Status**

This issue will be fixed in a future version of the **POS-PHY Level 4 MegaCore Function User Guide**.

---

**Valid Range of Full Threshold High is Incorrect**

The valid range of the full threshold high (FTH) is dependent on many parameters such as the width of the internal bus. When changing the width of the bus, the wizard may allow the FTH out of the acceptable range and so you end up with an incorrect or non-existent choice for the FTH.

**Affected Configurations**

This issue affects transmitters.
Design Impact
There is no design impact.

Workaround
To work around the issue, if you change the bus width, for example the Atlantic data width, ensure you modify the FTH value on the Protocol Parameters tab of the wizard.

Solution Status
The incorrect paragraphs will be fixed in a future version of the POS-PHY Level 4 MegaCore Function User Guide.

Errors when Editing Transmitters v7.2 or Earlier in v8.0
If you edit a v7.2 or earlier 64 or 128-bit transmitter MegaCore variation in the v8.0 MegaWizard Plug-In, the PLL input frequency is set to 1 MHz, which is incorrect.

Affected Configurations
This issue affects 64- and 128-bit transmitters.

Design Impact
There is no design impact.

Workaround
To work around the issue, follow these steps:
1. Click in the LVDS Data Rate dialog box.
2. Press Enter.
   The PLL input frequency parameter resets to the correct value—data rate divided by deserialization factor.

Solution Status
This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

Transmitter Sends Extra Idles with Burst Limit Enable
The POS-PHY Level 4 MegaCore function transmitter sends up to four control words between two bursts when you turn on Burst Limit Enable.

Affected Configurations
This issue affects transmitters with a 32-bit data-path width when you turn on Burst Limit Enable.

Design Impact
There design bandwidth is decreased.
Workaround
In the <variation name>tx_core.v file, change the TXLITE parameter from 0 to 1.

    parameter TXLITE = 1;

Solution Status
This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

Missing Constraint
In designs targeting Stratix III and Stratix IV devices, the derive_clock_uncertainty Synopsis design constraint (SDC) for TimeQuest is missing.

Affected Configurations
This issue affects all Stratix III and Stratix IV designs.

Design Impact
There is no design impact.

Workaround
Add the derive_clock_uncertainty SDC for Stratix III and Stratix IV device designs.

Solution Status
This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

Training Interval is Greater than Specified
In corner cases, for example with datapath is 256 and a high number of ports and low burst length (BURSTLEN), the maximum training interval (MaxT) is greater than you specify.

Affected Configurations
This issue affects all designs.

Design Impact
There is no design impact.

Workaround
Add (or substract) another BURSTLEN to calculation, so MaxT is SET_MaxT + 2 × BURSTLEN.

Solution Status
This issue will never be fixed.
Signal stat_rd_dip4_oos Goes to X in Simulation

Some signals go to X (for example, stat_rd_dip4_oos) during simulation.

Affected Configurations
Receiver configurations with DPA enabled, in the following device families:
- Stratix II devices
- HardCopy® II devices
- Stratix III devices
- Stratix IV devices
- Stratix II GX devices
- Arria GX devices

Workaround
After you generate the functional simulation model, manually edit the model (*.vo or *.vho) to add a new parameter to the altlvds megafunction instantiation. To edit a Verilog HDL example, follow these steps:

1. Search for the altlvds_rx instantiation:
   ```
   altlvds_rx <instantiation name>
   ```
   Add the following parameter after the altlvds_rx //defparam list:
   ```
   <instantiation name>. x_on_bitslip = "OFF",
   ```

Design Impact
There is no design impact. However, the demonstration testbench simulation fails, as some signals go to X (for example, stat_rd_dip4_oos).

Solution Status
This issue is fixed in the Quartus II software version 8.0.

Irrelevant Signals: err_ry_msop* & err_ry_meop*

After generation, the MegaCore function may include the following irrelevant output signals, which you can safely ignore:
- err_ry_msop*
- err_ry_meop*

Affected Configurations
This issue affects all designs.

Design Impact
There is no design impact.

Workaround
This issue has no workaround.
Solution Status
This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

Warning Message: Pin "err_rd_dpa" Stuck at GND
During compilation, the Quartus® II software issues the following warning, which you can safely ignore:

Pin "err_rd_dpa" Stuck at GND

Affected Configurations
This issue affects all non-Stratix GX receivers with dynamic phase alignment (DPA) enabled.

Design Impact
There is no design impact.

Workaround
This issue has no workaround.

Solution Status
This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

The Calendar Length Value Cannot Equal 256
If the transmitter’s status interpretation mode is set to pessimistic, the programmable calendar length support parameter must be less than the maximum number of ports (< 256), unless the asymmetric port support parameter is enabled.

Affected Configurations
This issue affects all transmitter variations of the MegaCore function that use the pessimistic mode for status interpretation, and that do not have the asymmetric port support parameter enabled.

Design Impact
The status first-in first-out (FIFO) buffer may lock up. The scheduler in individual buffers variations of the MegaCore function may also lock up.

Workaround
If you turn on the programmable calendar length support in your variation, make sure that you set the calendar length value—via a pin or the Avalon® Memory-Mapped (Avalon-MM) register—to less than the maximum calendar length (that is, 256); unless asymmetric port support is enabled, in which case you select the maximum calendar length in IP Toolbench.
Solution Status
This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

IP Toolbench Error After Changing the Device Family
If you change the device family when editing an existing custom megafuction variation (POS-PHY Level 4 MegaCore function variation) without first changing the device family in the Quartus® II project, an error may occur when generating the MegaCore function. This results in a MegaCore function generation error message.

This issue also applies when creating a new custom megafuction variation, if you use a different device family to that specified in the Quartus II project.

Affected Configurations
This issue can affect all configurations.

Design Impact
You may not be able to generate a MegaCore function.

Workaround
Before using the MegaWizard® Plug-In Manager to create or edit a POS-PHY Level 4 custom megafuction variation, make sure that a Quartus II project exists and that the required device family is set in the project. To set the device family, select Device from the Assignments menu in the Quartus II software.

When using the MegaWizard Plug-In Manager to create or edit the megafuction variation, set the device family to be the same as the device family set in the Quartus II project. You can set the device family in the Basic Parameters tab when parameterizing the MegaCore function.

Solution Status
This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

IP Toolbench Fails to Generate IP Functional Simulation Models for HardCopy Stratix Devices
If you select HardCopy Stratix in the MegaWizard Plug-In Manager and you turn on Generate Simulation Model and generate a MegaCore function variation, IP Toolbench fails with an error.

Affected Configurations
This issue affects all configurations.

Design Impact
You cannot generate an IP functional simulation model.

Workaround
Select the Stratix family in the MegaWizard Plug-In Manager.
Solution Status
This issue will never be fixed.

IP Toolbench Generation Fails if the Generation Is Cancelled and Restarted

By clicking the IP Toolbench Generate button you start generating a POS-PHY Level 4 MegaCore function variation. If, during generation, you click the Cancel button (Generation window) and click the IP Toolbench Generate button again to restart the generation, IP Toolbench fails and produces the following error message:

Affected Configurations
This issue affects all variations of the MegaCore function.

Design Impact
IP Toolbench does not generate any files.

Workaround
To cancel a generation and avoid this error, follow these steps:
1. Click the Cancel button in the Generation window.
2. Close IP Toolbench by clicking the × in the upper right corner.
3. Relaunch IP Toolbench from the MegaWizard Plug-In Manager (Tools menu).

Refer to the Getting Started chapter of the POS-PHY Level 4 MegaCore Function User Guide for instructions on using IP Toolbench.

Solution Status
This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.
Revision History

Table 17–1 shows the revision history for the RapidIO MegaCore® function.

For more information on the new features, refer to the RapidIO MegaCore Function User Guide.

Table 17–1. RapidIO MegaCore Function Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>▪ Full support for Stratix® III devices</td>
</tr>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>▪ Support for incoming multicast transactions</td>
</tr>
<tr>
<td></td>
<td></td>
<td>▪ Support to enable or disable destination ID checking</td>
</tr>
<tr>
<td></td>
<td></td>
<td>▪ Support to set transceiver starting channel number</td>
</tr>
<tr>
<td></td>
<td></td>
<td>▪ Requirement to configure a dynamic reconfiguration block with any Stratix IV transceivers, to enable offset cancellation</td>
</tr>
<tr>
<td>8.0 SP1</td>
<td>July 2008</td>
<td>▪ Maintenance release</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>▪ Support for 1× mode 3.125 GBaud variations in Arria® GX devices</td>
</tr>
<tr>
<td></td>
<td></td>
<td>▪ Preliminary support for Stratix IV devices</td>
</tr>
<tr>
<td></td>
<td></td>
<td>▪ Support to set reference clock frequency for Stratix II GX and Stratix IV GX internal transceivers</td>
</tr>
<tr>
<td></td>
<td></td>
<td>▪ Support to set VCCH for Stratix II GX internal transceivers</td>
</tr>
<tr>
<td>7.2</td>
<td>October 2007</td>
<td>▪ Transport layer pass-through interface support added in SOPC Builder</td>
</tr>
<tr>
<td></td>
<td></td>
<td>▪ Full support for Arria GX devices</td>
</tr>
</tbody>
</table>

Errata

Table 17–2 shows the issues that affect the RapidIO MegaCore function v8.1, v8.0 SP1, v8.0, and v7.2.

Not all issues affect all versions of the RapidIO MegaCore function. Altera recommends upgrading to the latest available version of the MegaCore IP Library.

For SOPC Builder errata, which might affect the RapidIO MegaCore function and other SOPC Builder components, refer to the Quartus II Software Release Notes.
### Table 17–2. RapidIO MegaCore Function Errata (Part 1 of 2)

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Feb 09</td>
<td>The packet_transmitted Output Signal is Not Reliable</td>
<td>8.1 8.0 SP1 8.0 7.2</td>
</tr>
<tr>
<td>01 Dec 08</td>
<td>SourceID Can Be Incorrectly Set to Zero in NWRITE_R Response Packets</td>
<td>8.1 8.0 SP1 8.0 7.2</td>
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<tr>
<td></td>
<td>A Cancelled Packet Can Be Processed As a Normal Packet</td>
<td>8.1 8.0 SP1 8.0 7.2</td>
</tr>
<tr>
<td></td>
<td>Asserting io_m_wr_waitrequest During a Burst Transfer When</td>
<td>8.1 8.0 SP1 8.0 7.2</td>
</tr>
<tr>
<td></td>
<td>io_m_wr_write is Not Asserted Can Cause Deadlock</td>
<td>8.1 8.0 SP1 8.0 7.2</td>
</tr>
<tr>
<td></td>
<td>Four Back-to-Back Short Incoming Packets Can Cause Miscalculation of</td>
<td>8.1 8.0 SP1 8.0 7.2</td>
</tr>
<tr>
<td></td>
<td>the Following Packet Sizes</td>
<td>8.1 8.0 SP1 8.0 7.2</td>
</tr>
<tr>
<td></td>
<td>An Errored Incoming Packet Can Cause Miscalculation of the Following</td>
<td>8.1 8.0 SP1 8.0 7.2</td>
</tr>
<tr>
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<td>Packet Sizes</td>
<td>8.1 8.0 SP1 8.0 7.2</td>
</tr>
<tr>
<td></td>
<td>Timeout Logic Can Incorrectly Extend Doorbell Transaction Timeout</td>
<td>8.1 8.0 SP1 8.0 7.2</td>
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<tr>
<td></td>
<td>Doorbell Transaction Can Be Transmitted With Invalid Transaction ID</td>
<td>8.1 8.0 SP1 8.0 7.2</td>
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<tr>
<td>01 Nov 08</td>
<td>User Guide Description of Default Value of EF_ID Field in PHEAD0</td>
<td>8.1 8.0 SP1 8.0 7.2</td>
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<td></td>
<td>Register is Incorrect</td>
<td>8.1 8.0 SP1 8.0 7.2</td>
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<td>SOPC Builder Systems May Have Incorrectly Clocked Reset or Incorrect</td>
<td>8.1 8.0 SP1 8.0 7.2</td>
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<td>Calibration Clock Driver</td>
<td>8.1 8.0 SP1 8.0 7.2</td>
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<td>Stratix IV Simulations May Fail With Modelsim 6.3g Compiler</td>
<td>8.1 8.0 SP1 8.0 7.2</td>
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<td>Optimizations Enabled</td>
<td>8.1 8.0 SP1 8.0 7.2</td>
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<tr>
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<td>RapidIO MegaCore Function v8.0 Targeting Arria GX Device and</td>
<td>Fixed 8.1 8.0 SP1 8.0 7.2</td>
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<tr>
<td></td>
<td>Generated in Quartus II v8.1 Software Cannot Simulate With the v8.0</td>
<td>Fixed 8.1 8.0 SP1 8.0 7.2</td>
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<td>Demo Testbench</td>
<td>Fixed 8.1 8.0 SP1 8.0 7.2</td>
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<tr>
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<td>SOPC Builder Systems Can Lose Read Data Returned From I/O Avalon-MM</td>
<td>Fixed 8.1 8.0 SP1 8.0 7.2</td>
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<tr>
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<td>Slave Module</td>
<td>Fixed 8.1 8.0 SP1 8.0 7.2</td>
</tr>
<tr>
<td></td>
<td>Tx Port Write Control Register Priority Field Can Be Written to</td>
<td>Fixed 8.1 8.0 SP1 8.0 7.2</td>
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<td>Invalid Value 2'b1</td>
<td>Fixed 8.1 8.0 SP1 8.0 7.2</td>
</tr>
<tr>
<td></td>
<td>Valid NREAD Requests Cause Unexpected Illegal Transaction</td>
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<tr>
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<td>Decode Error to Be Declared</td>
<td>Fixed 8.1 8.0 SP1 8.0 7.2</td>
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<tr>
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<td>sys_mnt_s_waitrequest is Asserted Intermittently When sys_mnt_s</td>
<td>Fixed 8.1 8.0 SP1 8.0 7.2</td>
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<tr>
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<td>chipselect is Asserted</td>
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<td>Simultaneous Read and Write to the Doorbell Rx FIFO May Cause Doorbell</td>
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<td>Interrupt to Reset</td>
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<td>Writing OxFFFF to the Host Base Device ID Lock CSR Locks the Register</td>
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<td>Cancelling a Packet Might Cause the Following Packet to be Lost</td>
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</tr>
<tr>
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<td>Doorbell Interrupt Status Register TX_CPL_OVERFLOW Bit Cannot Be</td>
<td>Fixed 8.1 8.0 SP1 8.0 7.2</td>
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<td>Cleared</td>
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<td>Problems After a Read Transaction Address is Outside the Enabled</td>
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<td>Address Mapping Windows</td>
<td>Fixed 8.1 8.0 SP1 8.0 7.2</td>
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<tr>
<td>15 Jul 08</td>
<td>RapidIO MegaWizard Interface Does Not Set Transceiver VCCH to 1.2 V</td>
<td>Fixed 8.1 8.0 SP1 8.0 7.2</td>
</tr>
</tbody>
</table>
The packet_transmitted Output Signal is Not Reliable

The packet_transmitted output signal might be pulsed twice for each transmitted packet.

Affected Configurations
All 4x RapidIO variations.

Design Impact
The packet_transmitted signal cannot be used to determine the exact count of transmitted packets.

Workaround
None known.

Solution Status
This issue will be fixed in a future version of the RapidIO MegaCore function.

SourceID Can Be Incorrectly Set to Zero in NWRITE_R Response Packets

The SourceID field in an NWRITE_R response packet might be set to 0x0000 instead of being set to the destination ID received in the request packet.
**Affected Configurations**
All RapidIO variations that implement an Input/Output Avalon-MM master Logical layer module.

**Design Impact**
If a link partner sends an NWRITE_R request and detects an erroneous SourceID in the response on the link, it might not recognize the response to the request.

**Workaround**
To avoid this issue, perform one of the following workarounds:

- Generate NWRITE or SWRITE requests instead of NWRITE_R requests.
- Precede each sequence of NWRITE_R requests to the same destination ID with an NREAD request to that destination ID.
- Program the link partner to accept response packets regardless of their SourceID.

**Solution Status**
This issue will be fixed in a future version of the RapidIO MegaCore function.

---

**A Cancelled Packet Can Be Processed As a Normal Packet**

If a packet received over the RapidIO link contains a stomp control symbol, and this packet is immediately followed by a start-of-packet control symbol, the first packet might be processed as if it were not cancelled.

**Affected Configurations**
All 4× RapidIO variations.

**Design Impact**
The final two bytes of the cancelled packet are treated as the CRC of the cancelled packet. In most cases, a CRC error is detected, the packet is dropped, and the error recovery process is initiated. In the rare case that the final two bytes form a valid CRC for the packet, the partial packet is processed as if it were not cancelled.

**Workaround**
None known.

**Solution Status**
This issue will be fixed in a future version of the RapidIO MegaCore function.

---

**Asserting io_m_wr_waitrequest During a Burst Transfer When io_m_wr_write is Not Asserted Can Cause Deadlock**

If a slave driven by an Avalon-MM I/O master asserts the io_m_wr_waitrequest signal during a burst transfer when io_m_wr_write is not asserted, the Avalon-MM I/O master module will not assert the io_m_wr_write signal until io_m_wr_waitrequest is deasserted. In this case, the Avalon-MM interface deadlocks.
**Affected Configurations**
All RapidIO variations that implement an Avalon-MM I/O master write interface in an SOPC Builder system.

**Design Impact**
If the slave waits for the assertion of `io_m_wr_write` before deasserting the `io_m_wr_waitrequest` signal, and the master waits for the deassertion of `io_m_wr_waitrequest` before asserting `io_m_wr_write`, the module deadlocks.

**Workaround**
Do not assert `io_m_wr_waitrequest` indefinitely, or avoid asserting `io_m_wr_waitrequest` after a burst transfer has started.

**Solution Status**
This issue will be fixed in a future version of the RapidIO MegaCore function.

**Four Back-to-Back Short Incoming Packets Can Cause Miscalculation of the Following Packet Sizes**
If four short packets are transferred back-to-back from the Physical layer to the Transport layer, the size of subsequent packets can be miscalculated. This problem occurs only following a complex sequence of events followed by the receipt of four short back-to-back packets on the RapidIO link, and is therefore unlikely to occur.

**Affected Configurations**
All 4x RapidIO variations that implement a Transport layer.

**Design Impact**
If this problem occurs, the resulting erroneous packet sizes can cause Input/Output modules to reject valid packets, or to issue Avalon-MM transactions with incorrect burstcounts, among other possible impacts.

**Workaround**
To reduce the chance of encountering this issue, you can modify your application to reduce the number of back-to-back packet transfers from the Physical layer to the Transport layer, by preventing received packets from accumulating in the Physical layer Receive buffer.

For example, either of the following two modifications helps to avoid the accumulation of packets in the Physical layer Receive buffer:
- Run the system clock at the nominal clock frequency or higher.
- To decrease the back pressure that occurs when the Avalon-MM wait-request signals are asserted, do not assert these signals.

**Solution Status**
This issue will be fixed in a future version of the RapidIO MegaCore function.
An Errored Incoming Packet Can Cause Miscalculation of the Following Packet Sizes

If a packet marked as errored is transferred from the Physical layer to the Transport layer immediately following a valid packet, with no gap between the end of the first packet and the start of the second packet, the size of subsequent packets can be miscalculated.

Affected Configurations

All RapidIO variations that implement a Transport layer.

Design Impact

Erroneous packet sizes can cause Input/Output modules to reject valid packets, or to issue Avalon-MM transactions with incorrect burstcounts, among other possible impacts.

Workaround

You can modify your application to reduce the chance of encountering this issue, and you can perform a workaround that avoids the issue.

To reduce the chance of encountering this issue, you can modify your application in one or both of the following ways:

- Reduce the bit-error rate to reduce the number of errored packets received by the Transport layer.
- Reduce the number of back-to-back packet transfers from the Physical layer to the Transport layer, by preventing received packets from accumulating in the Physical layer Receive buffer. Either of the following two modifications helps to avoid the accumulation of packets in the Physical layer Receive buffer:
  - Run the system clock at the nominal clock frequency or higher.
  - To decrease the back pressure that occurs when the Avalon-MM wait-request signals are asserted, do not assert these signals.

To avoid the issue, perform the following workaround:

1. Create or edit your SOPC Builder project, or specify your RapidIO MegaCore function using the MegaWizard Plug-In Manager.
2. Perform one of the following steps:
   a. In the SOPC Builder, click Generate to generate the SOPC Builder system.
   b. In the MegaWizard Plug-In Manager, click Finish to generate the RapidIO MegaCore function.

   The SOPC Builder or MegaWizard Plug-In Manager generates the Transport layer Verilog HDL file transport.v.
3. Click Exit to close SOPC Builder.
4. Open the newly generated transport.v file for editing.
5. Replace
   
   \_Fstart_waddr = waddr ;

   with
   
   \_Fstart_waddr = waddr + wren;
**Solution Status**

This issue will be fixed in a future version of the RapidIO MegaCore function.

**Timeout Logic Can Incorrectly Extend Doorbell Transaction Timeout Period**

When a **DOORBELL** transaction is transmitted, it is assigned a timeout value based on the Port Response Time-Out Control register (offset 0x124) and a free-running counter. When the counter reaches the timeout value, if the **DOORBELL** transaction has not yet received a response, the transaction times out. In the slowest case, the free-running counter increments every 64 Avalon clock cycles. If **DOORBELL** transactions are transmitted fewer than 64 Avalon clock cycles apart, multiple transactions might be assigned the same timeout value. If processing the timeout for the previous **DOORBELL** transactions with the same timeout value takes too long, a **DOORBELL** transaction’s timeout might not be processed before the counter increments. In this case, the timeout is not recognized until the counter rolls over again to the same value. In addition, the timeout logic processes the pending transactions in FIFO order, and therefore does not examine the remaining pending **DOORBELL** transactions before the counter rolls over again.

**Affected Configurations**

All RapidIO variations that implement a Doorbell module.

**Design Impact**

A **DOORBELL** transaction might not time out when expected, holding up the timeout queue and preventing the Doorbell module from transmitting new transactions in a timely manner.

**Workaround**

To avoid this issue, ensure a wait of at least 64 Avalon clock cycles between transmission of **DOORBELL** transactions.

**Solution Status**

This issue will be fixed in a future version of the RapidIO MegaCore function.

**Doorbell Transaction Can Be Transmitted With Invalid Transaction ID**

A seventeenth pending **DOORBELL** transaction can have an invalid transaction ID. After reset, a counter generates sixteen transaction IDs for the first sixteen **DOORBELL** transactions. When a Doorbell response packet arrives at the Doorbell module, the transaction ID for the originating transaction is recycled through a FIFO and made available for a new pending **DOORBELL** transaction. However, a seventeenth pending **DOORBELL** transaction may use an underflowed TID FIFO output and be assigned a random value for its transaction ID.

**Affected Configurations**

All RapidIO variations that implement a Doorbell module.
**Design Impact**

A DOORBELL transaction can be transmitted with an invalid transaction ID. In this case, its response may not be identified correctly, and the Doorbell module can deadlock.

**Workaround**

To avoid this issue, ensure that 15 or fewer DOORBELL transactions are pending responses before you transmit a new DOORBELL transaction.

**Solution Status**

This issue will be fixed in a future version of the RapidIO MegaCore function.

---

**User Guide Description of Default Value of EF_ID Field in PHEAD0 Register is Incorrect**

The default value of the EF_ID field in the PHEAD0 register (offset 0x100), is listed incorrectly in the RapidIO MegaCore Function User Guide. The correct value is 0x0001.

**Affected Configurations**

All RapidIO variations.

**Design Impact**

Relying on the default value for the EF_ID field in the PHEAD0 register to be the value specified in the RapidIO MegaCore Function User Guide will lead to incorrect results.

**Workaround**

Expect the default value 0x0001 in this register field.

**Solution Status**

This issue will be fixed in a future version of the RapidIO MegaCore Function User Guide.

---

**SOPC Builder Systems May Have Incorrectly Clocked Reset or Incorrect Calibration Clock Driver**

A RapidIO transceiver-based system created in SOPC Builder might generate RTL with the source reset clock in the incorrect clock domain, or might connect the calibration clock port incorrectly.

**Affected Configurations**

All RapidIO variations with high-speed transceivers in SOPC Builder systems with multiple clocks.

**Design Impact**

If the calibration clock is driven by the wrong clock, transceiver calibration can fail, leading to hardware failures.

If the reset is driven by an incorrect clock, intermittent hardware failures may occur.
**Workaround**

If your design allows, you can avoid this issue by using a single clock for all components in your SOPC Builder system. However, cal_blk_clk runs at a maximum frequency of 125 MHz, and all transceiver-based designs in your system must have the same calibration clock. Therefore, not all designs admit this solution.

If you must implement multiple clocks in your design, perform the following alternate workaround to ensure your design is not impacted by this issue.

To determine whether the clock connections in your design are impacted by this issue, and fix them if needed, perform the following steps:

1. Create or edit your SOPC Builder project.
2. In the SOPC Builder, click **Generate** to generate the SOPC Builder system.
   
   The SOPC Builder writes the top-level system file `<SOPC_system_name>.v` or `<SOPC_system_name>.vhd`, depending on the HDL you use.
3. Click **Exit** to close SOPC Builder.
4. Open the newly generated top-level system `.v` or `.vhd` file for editing.
5. Search for the string `the_rapidio` to locate all your RapidIO MegaCore function instances.
6. For each instance, examine the signal connected to the cal_blk_clk port. In Verilog HDL, the relevant code line is similar to the following:
   ```
   .cal_blk_clk (cal_blk_clk),
   ```
7. If the name in parentheses is not that of the calibration clock you want to connect to this port, replace it with your intended calibration clock.
8. For each instance, examine the signal connected to the reset_n port. In Verilog HDL, the relevant code line is similar to the following:
   ```
   .reset_n (clk_0_reset_n),
   ```
9. If the clock name in the signal name in parentheses is not that of the clock connected to the Avalon system clock, replace it with the Avalon system clock. The following code line results:
   ```
   .reset_n (<sysclk_name>_reset_n),
   ```

**Solution Status**

This issue will be fixed in a future version of the RapidIO MegaCore function.

**Stratix IV Simulations May Fail With Modelsim 6.3g Compiler Optimizations Enabled**

Simulation of a RapidIO MegaCore function targeted to a Stratix IV device using Modelsim 6.3g with compiler optimizations enabled, may fail. Compiler optimizations are enabled by default in this version of Modelsim.

**Affected Configurations**

All RapidIO variations that target a Stratix IV device.
\textbf{Design Impact}

The IP functional simulation model of an affected configuration may produce data errors if simulated using Modelsim 6.3g.

\textbf{Workaround}

To avoid this issue, disable the Modelsim compiler optimizations by adding the -novopt switch to the \texttt{vsim} command, in the <\texttt{variant}> \_run_modelsim.tcl script or when you call \texttt{vsim} from the command line.

\textbf{Solution Status}

This issue will be fixed in a future version of the RapidIO MegaCore function.

\textbf{RapidIO MegaCore Function v8.0 Targeting Arria GX Device and Generated in Quartus II v8.1 Software Cannot Simulate With the v8.0 Demo Testbench}

If a RapidIO MegaCore function v8.0 instance that targets an Arria GX device is generated using the Quartus II software v8.1, it cannot simulate with the demonstration testbench. The testbench targets Stratix II GX libraries, but the generated IP functional simulation model requires Arria GX libraries.

\textbf{Affected Configurations}

All RapidIO MegaCore function v8.0 instances that target an Arria GX device and are compiled in the Quartus II software v8.1.

\textbf{Design Impact}

The demonstration testbench simulation does not run correctly with the affected configurations.

\textbf{Workaround}

To avoid this issue, perform one of the following workarounds:

\begin{itemize}
  \item Upgrade to the RapidIO MegaCore function v8.1 and regenerate your configuration.
  \item If you are unable to upgrade to the RapidIO MegaCore function v8.1, perform the following steps:
    \begin{itemize}
      \item In your Quartus II project, open the generated <\texttt{variant}> \_run_modelsim.tcl script in a text editor.
      \item In the Quartus Libraries section of the file, replace
      \begin{verbatim}
      append libraries {stratixiigx_stratixiigx_hssi}
      append lib_files {{stratixiigx_atoms.v} {stratixiigx_hssi_atoms.v}}
      \end{verbatim}
      with
      \begin{verbatim}
      append libraries { stratixiigx stratixiigx_stratixiigx_hssi arriagx\ arriagx_hssi }
      append lib_files {{stratixiigx_atoms.v} {stratixiigx_hssi_atoms.v} \ {arriagx_atoms.v} {arriagx_hssi_atoms.v}}
      \end{verbatim}
    \end{itemize}
\end{itemize}

\textbf{Solution Status}

This issue is fixed in version 8.1 of the RapidIO MegaCore function.
SOPC Builder Systems Can Lose Read Data Returned From I/O Avalon-MM Slave Module

In a system generated using SOPC Builder, when more than eight outstanding reads are issued from the system interconnect fabric to the RapidIO I/O Avalon-MM slave module, the read data for some of the reads can be lost. Although the RapidIO I/O Avalon-MM slave module can accept 14 outstanding reads, the interconnect fabric cannot track more than 8 outstanding read requests to this module.

Affected Configurations
All RapidIO variations that implement an Avalon-MM I/O slave interface in an SOPC Builder system.

Design Impact
In the affected configurations, read data returned from the RapidIO link can be lost.

Workaround
Perform the following workaround:
1. Create or edit your SOPC Builder project.
2. In the SOPC Builder, click Generate to generate the SOPC Builder system.
   The SOPC Builder writes the generation system peripheral template file \(<SOPC_system_name>.ptf\).
3. Click Exit to close SOPC Builder.
4. Open the newly generated .ptf for editing.
5. Under the definition for the io_read_slave, replace
   Maximum_Pending_Read_Transactions = "8";
   with
   Maximum_Pending_Read_Transactions = "14";
6. Close the .ptf.
7. Open the Nios II EDS Command Shell.
8. Navigate to the directory in which your .ptf is located.
9. Type `sopc_builder --classic --generate` to generate the new system.

Solution Status
This issue is fixed in version 8.1 of the RapidIO MegaCore function.

Tx Port Write Control Register Priority Field Can Be Written to Invalid Value 2'b11

A write of the value 2'b11 to the Tx Port Write Control register PRIORITY field is not overwritten to 2'b10 as stated in the RapidIO MegaCore Function User Guide. Instead, the invalid value 2'b11 remains and can cause incorrect scheduling of packets.

Affected Configurations
All RapidIO variations with the Port Write Tx enable option selected.
Design Impact
Incorrect scheduling of packets can occur if the value 2'b11 is written to the Tx Port Write Control register PRIORITY field.

Workaround
Avoid writing the value 2'b11 to the Tx Port Write Control register PRIORITY field.

Solution Status
This issue is fixed in version 8.1 of the RapidIO MegaCore function.

Valid NREAD Requests Cause Unexpected Illegal Transaction Decode Error to Be Declared

When an NREAD is the first received transaction or an NREAD follows a write transfer that has a smaller packet size than the NREAD transaction, the NREAD transaction can incorrectly flag the illegal transaction decode error bit (ILL_TRAN_DECODE) in the Logical/Transport Layer Error Detect CSR.

Affected Configurations
All RapidIO variations that implement an I/O Avalon-MM master module.

Design Impact
The illegal transaction decode error bit (ILL_TRAN_DECODE) in the Logical/transport Layer Error Detect CSR can be set incorrectly.

Workaround
Ignore the illegal transaction decode error bit (ILL_TRAN_DECODE) in the Logical/Transport Layer Error Detect CSR.

Solution Status
This issue is fixed in version 8.1 of the RapidIO MegaCore function.

sys_mnt_s_waitrequest is Asserted Intermittently When sys_mnt_s_chipselect is Asserted

The system maintenance Avalon-MM slave module intermittently asserts the sys_mnt_s_waitrequest signal when sys_mnt_s_chipselect is asserted, even if neither sys_mnt_s_read nor sys_mnt_s_write is asserted. In addition, if sys_mnt_s_read or sys_mnt_s_write is asserted while sys_mnt_s_waitrequest is asserted, the read or write transaction might not complete normally.

Affected Configurations
All RapidIO variations that implement a System Maintenance Avalon-MM slave module.
**Design Impact**

If `sys_mnt_s_read` or `sys_mnt_s_write` is asserted while `sys_mnt_s_waitrequest` is asserted, the read or write transaction might not complete correctly.

**Workaround**

Ensure that you assert the `sys_mnt_s_chipselect` signal only when `sys_mnt_s_read` or `sys_mnt_s_write` is asserted.

**Solution Status**

This issue is fixed in version 8.1 of the RapidIO MegaCore function.

---

**Simultaneous Read and Write to the Doorbell Rx FIFO May Cause Doorbell Interrupt to Reset**

If the Rx FIFO in the Doorbell module contains one outstanding DOORBELL message, a write to this FIFO is in process, and a read of this FIFO occurs at the same time as the write operation or a few clock cycles afterward, the `drbell_s_irq` signal may be inadvertently reset.

**Affected Configurations**

All RapidIO variations that implement a Doorbell module.

**Design Impact**

A DOORBELL message may remain in the Doorbell module Rx FIFO with no outstanding interrupt signal to indicate its presence to the Avalon-MM interface.

**Workaround**

After you detect a Doorbell interrupt on the `drbell_s_irq` line, read the Doorbell module Rx Doorbell Status register `FIFO_LEVEL` field to determine the number of outstanding messages in the Doorbell module Rx FIFO. Ensure that you process this number of messages. After you process all these outstanding messages, read the `FIFO_LEVEL` again to confirm the Doorbell module Rx FIFO is empty.

**Solution Status**

This issue is fixed in version 8.1 of the RapidIO MegaCore function.

---

**Writing 0xFFFF to the Host Base Device ID Lock CSR Locks the Register**

The `HOST_BASE_DEVICE_ID` field of the Host Base Device ID Lock CSR resets to 0xFFFF when the lock is relinquished. However, if the value 0xFFFF is written to this register, the value incorrectly acquires the lock.

**Affected Configurations**

All RapidIO variations that implement a Transport layer.
Design Impact
If the register’s current value is 0xFFFF, write operations to the Host Base Device ID Lock CSR might be unsuccessful.

Workaround
After writing your base device ID to the HOST_BASE_DEVICE_ID field of the Host Base Device ID Lock CSR, check that the value you wrote appears in the register. If the register contains the value 0xFFFF, write 0xFFFF to the register to unlock it, and then write your base device ID to the register again.

Solution Status
This issue is fixed in version 8.1 of the RapidIO MegaCore function.

Cancelling a Packet Might Cause the Following Packet to be Lost
If a Stomp control symbol arrives on the RapidIO link, followed too quickly by a Restart-from-retry control symbol, the first packet that follows the Restart-from-retry symbol can be lost. When this packet is received, a Packet-not-accepted control symbol is incorrectly sent, and the Link-request and Link-response control symbol exchange that ensues incorrectly indicates an incremented AckID for the packet that is rejected.

Affected Configurations
All serial RapidIO variations.

Design Impact
If this issue affects a request packet that does not require a response, the packet is dropped silently. If the issue affects a response packet or a request packet that requires a response, the remote endpoint times out waiting for the response.

Workaround
To avoid this issue or its design impact, perform one of the following workarounds:

■ To avoid the issue, prevent link congestion, so that Stomp and Restart-from-retry control symbols are not issued.
■ To avoid a dropped packet caused by this issue, generate only request packets that require a response, such as NWRITE_R transactions, and ensure that request packets are resubmitted after a timeout occurs.

Solution Status
This issue is fixed in version 8.1 of the RapidIO MegaCore function.

Doorbell Interrupt Status Register TX_CPL_OVERFLOW Bit Cannot Be Cleared
After the TX_CPL_OVERFLOW bit in the Doorbell Interrupt Status register is set, it cannot be reset.

Affected Configurations
All RapidIO variations that implement a Doorbell module.
Design Impact
The TX_CPL_OVERFLOW bit in the Doorbell Interrupt Status register cannot be reset. After it is set, therefore, any subsequent overflow conditions cannot be detected.

Workaround
To mitigate this issue, perform one of the following three workarounds:

- Send fewer than sixteen DOORBELL transactions at a time, and ensure that the Doorbell module Tx Completion buffer is read as soon as each DOORBELL transaction completes. This workaround avoids overflow of the Tx Completion buffer.
- Disable the TX_CPR_OVERFLOW bit in the Doorbell Interrupt Status register by clearing the TX_CPL_OVERFLOW bit in the Doorbell Interrupt Enable register. This workaround avoids notification if the Tx Completion buffer overflows.
- Avoid use of the Tx Completion buffer for successful outbound DOORBELL messages by clearing the COMPLETED bit of the Tx Doorbell Status Control register.

Solution Status
This issue is fixed in version 8.1 of the RapidIO MegaCore function.

Problems After a Read Transaction Address is Outside the Enabled Address Mapping Windows

After a read transaction to an address outside the enabled address mapping windows is attempted on the Input/Output Avalon-MM slave interface, the RapidIO MegaCore function can send two or more request packets with the same transaction ID or it can continuously assert the io_s_rd_waitrequest or io_s_wr_waitrequest signal.

Affected Configurations
All RapidIO variations that implement an Input/Output Avalon-MM slave interface.

Design Impact
A response packet might be matched with the wrong request packet, or the Input/Output Avalon-MM read or write slave interface might stall by asserting the wait-request signal indefinitely.

Workaround
Avoid submitting Avalon-MM read transactions with addresses outside the enabled address mapping windows to the Input/Output Avalon-MM read slave interface. For example, you can define and enable an address mapping window that includes all possible addresses.

Solution Status
This issue is fixed in version 8.1 of the RapidIO MegaCore function.
RapidIO MegaWizard Interface Does Not Set Transceiver VCCH to 1.2 V

If VCCH is set to 1.2 V in the RapidIO MegaWizard interface, the value remains at the default setting of 1.5 V in the transceiver.

Affected Configurations
All Stratix II GX RapidIO variations that implement a transceiver with a VCCH setting of 1.2 V.

Design Impact
The RapidIO MegaWizard interface cannot be used to implement a transceiver with VCCH set to 1.2 V.

Workaround
To set the RapidIO transceiver VCCH to 1.2 V, perform the following workaround:
1. Generate the RapidIO MegaCore function using the MegaWizard interface.
2. In a text editor, open the generated transceiver wrapper file, `<variation_name>_riophy_gxb.v`.
3. In the `alt2gxb` component `defparm` section, replace `alt2gxb_component.tx_analog_power="1.5v";` with `alt2gxb_component.tx_analog_power="1.2v";`

Solution Status
This issue is fixed in version 8.0 SP1 of the RapidIO MegaCore function.

Receipt of a Write Request for 5, 6, or 7 Bytes by the I/O Master Causes an Invalid Avalon-MM Burst Transaction

If a RapidIO Input/Output Avalon-MM master Logical layer module in a 1× (32-bit wide) RapidIO MegaCore variation receives an `NWRITE` or `NWRITE_R` write request for 5, 6, or 7 bytes of data, the module creates an invalid Avalon-MM burst transaction. The module translates the request to a burst with burstcount value 2 but with different byteenable values in the two cycles. The Avalon-MM interface specification requires that a burst have a uniform byteenable value.

Affected Configurations
All RapidIO 1× variations that implement an Input/Output Avalon-MM master Logical layer module.

Design Impact
When this violation of the Avalon-MM interface specification occurs, the behavior of an Avalon-MM slave connected to this Avalon-MM master is undefined.

Workaround
Avoid sending write requests for 5, 6 or 7 bytes in the system, or add a small adapter to translate these two-word bursts to two single-word transfers.
Solution Status
This issue will be fixed in a future release of the RapidIO MegaCore function.

Request Packets are Sent When the Read Transaction Address is Outside the Enabled Address Mapping Windows

The RapidIO MegaCore function sends an NREAD request packet when the address of a read transaction on the Input/Output Avalon-MM slave interface is outside the enabled address mapping windows. The read Avalon-MM slave block waits for a response to the request packet or for a response timeout. Only after it receives one of these two responses does the read Avalon-MM slave block complete the read transaction on the Input/Output Avalon-MM read slave interface by asserting the io_s_rd_readdatavalid and io_s_rd_readerror signals.

Affected Configurations
All RapidIO variations that implement the Input/Output Avalon-MM slave interface.

Design Impact
The Input/Output Avalon-MM read slave interface stalls waiting for a response or a timeout after it sends an out-of-bounds NREAD packet. Undesired NREAD packets are sent and long delays can occur while this interface stalls.

Workaround
Avoid submitting Avalon-MM read transactions with addresses outside the enabled address mapping windows to the Input/Output Avalon-MM read slave interface. For example, you can define and enable an address mapping window that includes all possible addresses.

Solution Status
This issue is fixed in version 8.0 of the RapidIO MegaCore function.

Wrong Value Returned From Maintenance Read Transactions in SOPC Builder Generated Systems

In a system generated using SOPC Builder, an Avalon-MM master that attempts to execute a read transfer from the Maintenance Avalon-MM interface using mnt_s returns an undefined value before the read transaction completes.

Affected Configurations
All RapidIO variations that implement the Maintenance Avalon-MM slave interface in an SOPC Builder system.

Design Impact
Read transactions from the Maintenance Avalon-MM Slave module in an SOPC Builder generated system do not execute.
**Workaround**

Perform the following workaround:

1. Create or edit your SOPC Builder project.
2. In the SOPC Builder, click **Generate** to generate the SOPC Builder system.
   
   The SOPC Builder writes the generation system peripheral template file `<SOPC_system_name>.ptf`.
3. Click **Exit** to close SOPC Builder.
4. Open the newly generated `.ptf` for editing.
5. Replace
   
   `Maximum_Pending_read_transactions = "0";
   `with
   
   `Maximum_Pending_read_transactions = "64";

6. Close the `.ptf`.
7. Open the Nios II EDS Command Shell.
8. Navigate to the directory in which your `.ptf` is located.
9. Type `sopc_builder --classic --generate` to generate the new system.

**Solution Status**

This issue is fixed in version 8.0 of the RapidIO MegaCore function.

**Exchange of Packets Stops if Link Partner Sends Restart-From-Error in Response to Packet-Retry Instead of Restart-From-Retry**

If a link partner sends a `link-request input-status` control symbol (also known as `restart-from-error` control symbol) in response to a `packet-retry` control symbol sent by the RapidIO MegaCore function, the MegaCore function responds with a `link-response OK` control symbol, but the input port remains in the retry-stopped mode until a `restart-from-retry` control symbol is received.

**Affected Configurations**

All serial RapidIO variations.

**Design Impact**

Processing of incoming traffic stops until the MegaCore function receives a `restart-from-retry` control symbol, detects an input error, or is reset.

**Workaround**

Perform one of the following workarounds:

- Make sure the link partner sends a `restart-from-retry` in response to a `packet-retry`.

  **or**
Monitor the state of the input control state machine with software and have the link partner cause a detectable error or reset the MegaCore function when the input state machine remains in the retry-stopped for excessive amounts of time.

**Solution Status**
This issue is fixed in version 8.0 of the RapidIO MegaCore function.

### Enabling Port-Writes Forces Instantiation of Maintenance Avalon-MM Slave Interface

If any of the Port Write options are turned on in the Transport and Maintenance page, the Maintenance Avalon-MM slave interface is instantiated even if the Maintenance logical layer interface(s) parameter is set to None or Avalon-MM Master.

**Affected Configurations**
All variations with Port Write options turned on and Maintenance logical layer interface(s) set to None or Avalon-MM Master.

**Design Impact**
The generated MegaCore has a Maintenance Avalon-MM slave interface when none was expected and the demonstration testbench terminates with the TESTBENCH INCOMPLETE message instead of TESTBENCH PASSED.

**Workaround**
Make sure Port Write options are turned off in the Transport and Maintenance page if no Maintenance Avalon-MM slave interface is desired, or set the Maintenance logical layer interface(s) parameter to Avalon-MM Master and Slave or Avalon-MM Slave if a Maintenance Avalon-MM slave interface is desired.

**Solution Status**
This issue is fixed in version 8.0 of the RapidIO MegaCore function.

### Input/Output Avalon-MM Master Module Stops Accepting Write Request Packets

The Input/Output Avalon-MM master module stops accepting write request packets if it receives too many malformed packets. When the Input/Output Avalon-MM master module receives a malformed packet that has an invalid payload size (larger than 8-bytes but not a multiple of 8-bytes) but with valid CRC(s), it executes the burst write transfer, using undefined values to fill in for the missing payload on the last word of the Avalon-MM burst write transfer. Furthermore, the Input/Output Avalon-MM master module fails to de-allocate some internal resources. If this occurs several times, the Input/Output Avalon-MM master module eventually expends all aforementioned resources and is unable to accept any further write request packets, causing traffic to back up in the transport and physical layer, and causing the received packets to be retried indefinitely.

**Affected Configurations**
All RapidIO variations using the Avalon-MM write master interface of the Input/Output Avalon-MM master module.
Design Impact
The MegaCore function stops accepting all incoming packets.

Workaround
Avoid sending malformed packets of the type described above.

Solution Status
This issue is fixed in version 8.0 of the RapidIO MegaCore function.

Illegal IO Slave Write Transaction Prevents Sending of Doorbell Packet
An IO Slave Write Transaction with the byteenable bus set to all zeros causes the RapidIO MegaCore function to miss sending a DOORBELL packet.

Affected Configurations
This issue affects all variants that have the IO Slave and Doorbell modules enabled. Both 1x and 4x at all data rates are affected.

Design Impact
The DOORBELL packet is never received by the intended target. Any processing by the remote processing endpoint dependent on the DOORBELL message is affected.

Workaround
Avoid a zero value on the io_s_wr_byteenable bus when issuing write transactions across the IO Slave Write port.

Solution Status
This issue is fixed in version 8.0 of the RapidIO MegaCore function.

Reception of Malformed Write Request Packet Causes Loss of the Next Request Packet
If an NWRITE or NWRITE_R request packet without any payload (that is, shorter than 10 bytes), but with a valid CRC, is received by the Input/Output Avalon-MM master module, the following request packet received by the Input/Output Avalon-MM master is silently discarded.

Affected Configurations
This issue affects variations with a 64-bit wide internal data path that implements the input/output Avalon-MM master module.

Design Impact
In the unlikely event that such a malformed request packet is received, the following request packet is ignored. If that request requires a response, the response is not sent and the request eventually times out. The far end entity decides how to deal with the timed out request. If the request does not require a response, it is silently ignored and normal operation continues.
Workaround
Avoid sending write request packets with no payload.

Solution Status
This issue is fixed in version 8.0 of the RapidIO MegaCore function.

Propagation Delay Before New Timeout Value Used For New Packets
A new value in the VALUE field of the Port Response Time-Out Control CSR (0x124) might not propagate quickly enough to be applied to the next transaction. Any packet sent within 64 Avalon clock cycles of the value change in the register might be sent using the previous timeout value.

Previously, this issue was not well understood, and was reported as an erroneous internal write transaction that overwrites a write transfer to registers in the physical layer with an invalid value.

Affected Configurations
This issue affects all RapidIO MegaCore function variations.

Design Impact
A packet sent within 64 Avalon clock cycles of a change in the VALUE field of the Port Response Time-Out Control CSR might be sent using the previous timeout value.

Workaround
After writing a new timeout value to the CSR, wait at least 64 Avalon clock cycles after the value is written in the register before sending a new packet on the RapidIO link.

Solution Status
The documentation is corrected to include the required delay in v8.0.

Incorrect I/O Logical Layer Avalon-MM Slave Write Request Packets
The RapidIO Input/Output Logical layer Avalon-MM slave can generate an incorrect write request packet if an invalid combination of burstcount, byteenable and address is applied to the datapath write Avalon-MM slave interface.

Affected Configurations
This issue affects all variations that include the Input/Output logical layer module.

Design Impact
An incorrect write request packet can be sent. This incorrect packet may cause further complications in the attached devices.

Workaround
Avoid using invalid combinations of burstcount, byteenable, and address. The valid combinations are described in the Avalon-MM Burstcount and Byteenable Encoding in RapidIO Packets section in the Functional Description chapter of the RapidIO MegaCore Function User Guide.
Solution Status

RapidIO MegaCore function versions 7.1 and beyond check for several invalid combinations, and do not generate a write request on the RapidIO link in these cases. Future versions of the RapidIO MegaCore function will check for additional invalid combinations. However, Altera recommends that you avoid the use of invalid combinations of burstcount, byteenable, and address in any version of the RapidIO MegaCore function.
Revision History

Table 18–1 shows the revision history for the QDRII SRAM MegaCore® function.

For more information on the new features, refer to the QDRII SRAM MegaCore Function User Guide.

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>7.2</td>
<td>October 2007</td>
<td>Maintenance release.</td>
</tr>
</tbody>
</table>

Errata

Table 18–2 shows the issues that affect the QDRII SRAM MegaCore function v8.1, 8.0, and 7.2.

Not all issues affect all versions of the QDRII SRAM MegaCore function.

Termination Error When Compiling Design

The fitter reports the following error: “Error Bidirectional I/O “cq” uses the parallel termination but does not have dynamic termination control.”
Affected Configurations
This issue affects designs using the QDRII SRAM Controller.

Design Impact
The design fails to fit.

Workaround
At top-level design, change the pin direction from inout to input for 
- qdrii_cq_<index>; qdrii_cqn_<index>.

Solution Status
This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

Incorrect IP Toolbench Latency Behavior
When you open the IP Toolbench Parameterize window, you can select any latency for the default QDRII, but it only supports 1.5.

Affected Configurations
This issue affects all QDRII SRAM configurations.

Design Impact
IP Toolbench does not generate a variation and gives the following error message:

Megacore Function Generation Error
IP Functional Simulation creation Failed. The following error was returned:
Error: Top-level design entity
"qdr_auk_qdrii_sram_avalon_controller_ipfs_wrap" is undefined.

Workaround
For longer latency, select QDRII+.

Solution Status
This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

Simulating with the VCS Simulator
The QDRII SRAM Controller MegaCore function does not support the VCS simulator.

Affected Configurations
This issue affects all configurations.

Design Impact
The design does not simulate.
Workaround
There is no workaround for VHDL simulations. For Verilog HDL simulations. Change line 154 in the `qdrii_model.v` file to:

```
begin : f1
```

Also, change line 417 to:

```
begin : f2
```

Solution Status
This issue will not be fixed.

TimeQuest Timing Analyzer Failure
When you use the Quartus® II TimeQuest timing analyzer, it reports a recovery issue, because the reset is not in the same clock domain as the system clock.

Affected Configurations
This issue affects all configurations.

Design Impact
There is no design impact.

Workaround
Change the reset sequence for the signals clocked on the CQ clock, before you run the TimeQuest analyzer.

Solution Status
This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

PLL Placement
The IP Toolbench-generated example design uses a PLL phase shift of 90°, which can cause the design to fail hold timing analysis. The source synchronous PLL for the read capture should have a location constraint to place it on the same side of the device as the Q pins, otherwise, the source synchronous compensation does not compensate for the expected delays.

Affected Configurations
This issue affects all configurations.

Design Impact
The design fails hold timing analysis.

Workaround
The PLL must be located on the same side of the device as the CQ/CQn groups, for the PLL to compensate properly.
**Solution Status**
This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

**Constraints Errors With Companion Devices**
When you change the device in your project or add a HardCopy® II companion device to a Stratix® II project and you reopen the variation with IP Toolbench, the constraints editor sometimes does not show all previously set byte groups in the floorplan. The constraints editor only shows the constraints applied to byte groups that are valid for the current device.

**Affected Configurations**
This issue affects all configurations.

**Design Impact**
The design fails.

**Workaround**
Reassign the byte groups for the new device in the constraints editor.

**Solution Status**
This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

**Supported Device Families**
The QDRII SRAM Controller MegaCore function only supports Stratix and Stratix II series, and HardCopy II devices. However, if you choose an unsupported device for your Quartus II project and subsequently start the MegaWizard® Plug-In Manager, you can choose a different device family in the MegaWizard Plug-In Manager, which allows you to choose the QDRII SRAM Controller MegaCore function. There are no error messages when you perform this illegal operation.

**Affected Configurations**
This issue affects all configurations.

**Design Impact**
You cannot compile a design.

**Workaround**
Ensure you choose a supported device family for the Quartus II project.

**Solution Status**
This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.
Compilation Error (Stratix II Series & HardCopy II Devices Only)
The IP Toolbench constraints window allows the illegal situation where you can share DQ groups on the top and bottom banks for Stratix II series and HardCopy devices. When you compile your design the Quartus II software issues a no fit error.

Affected Configurations
This issue affects all DQS mode QDRII SRAM controllers on Stratix II series and HardCopy II devices.

Design Impact
When you choose Start Compilation, there is an error message and the design does not compile.

Workaround
If you are targeting Stratix II series or HardCopy II devices, in the Constraints window ensure you choose bytegroups on either the top or the bottom of the device, but not both.

Solution Status
This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

Gate-Level Simulation Filenames
Various Quartus II software options may cause it to generate a netlist with a different filename than that expected by the gate-level simulation script. The simulation script expects <project name>.vho or .vo and <project name>_v or _vhd.sdo files to be present.

Affected Configurations
This issue affects all configurations.

Design Impact
You cannot run gate-level simulations.

Workaround
For VHDL gate-level simulations, in the simulation/modelsim directory follow these steps:
1. Rename <filename>.vho file to <project name>.vho.
2. Rename <filename>.sdo file to <project name>_vhd.sdo.

For Verilog HDL gate-level simulations, in the simulation/modelsim directory follow these steps:
1. Rename the <filename>.vo file to <project name>.vo.
2. Rename the <filename>.sdo file to <project name>_v.sdo.
3. In the <project name>.vo file change the following line to point to the <project name>_v.sdo file:
initial $sdf_annotate("<project name>_v.sdo");

**Solution Status**
This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

**The ModelSim® Simulation Script Does Not Support Companion Devices**
If you have a HardCopy II companion device in a Stratix II project, be aware that the ModelSim simulation scripts do not work if you change to your companion device.

**Affected Configurations**
This issue affects designs with companion devices.

**Design Impact**
The simulation script does not run.

**Workaround**
Edit the Modelsim script to include the correct libraries.

**Solution Status**
This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.
Revision History

Table 19–1 shows the revision history for the Reed-Solomon Compiler.

For more information on the new features, refer to the Reed-Solomon Compiler User Guide.

Table 19–1. Reed-Solomon Compiler Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>Full support for Stratix® III devices.</td>
</tr>
</tbody>
</table>
| 8.0     | May 2008   | Full support for Cyclone® III devices  
|         |            | Preliminary support for Stratix IV devices      |
| 7.2     | October 2007 | Maintenance release.                             |

Errata

Table 19–2 shows the issues that affect the Reed-Solomon Compiler v8.1, 8.0, and 7.2.

Not all issues affect all versions of the Reed-Solomon Compiler.

Table 19–2. Reed-Solomon Compiler Errata

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Nov 08</td>
<td>Verilog HDL Simulation Fails</td>
<td>8.1 8.0 7.2</td>
</tr>
<tr>
<td></td>
<td>RS Decoder Fails When Number of Check Symbols and Symbols are Similar</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Display Symbol Button in IP Toolbench is Missing</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Verilog HDL Designs Do Not Simulate in Synopsys VCS</td>
<td>Fixed 8.1 8.0 7.2</td>
</tr>
<tr>
<td></td>
<td>No Symbol In IP Toolbench Symbol Window</td>
<td>Fixed 8.1 8.0 7.2</td>
</tr>
<tr>
<td></td>
<td>File Summary Does Not List All Generated Files</td>
<td>Fixed 8.1 8.0 7.2</td>
</tr>
<tr>
<td>01 Oct 07</td>
<td>Cannot Find Memory Initialization File if Not in Project Directory</td>
<td>8.1 8.0 7.2</td>
</tr>
</tbody>
</table>

Verilog HDL Simulation Fails

Running a simulation with the Verilog HDL testbench results in an empty summary_output.txt file.

Affected Configurations

This issue affects all Verilog HDL configurations.
**Design Impact**

You cannot use the `summary_output.txt` file to evaluate the functionality of the design. But you can evaluate the functionality by looking at the simulation waveform.

**Workaround**

Run the simulation with a VHDL design and use the VHDL testbench.

**Solution Status**

This issue will be fixed in a future release of the Reed-Solomon Compiler.

**RS Decoder Fails When Number of Check Symbols and Symbols are Similar**

With the variable decoder, when the **Number of check symbols** and **Symbols per codeword** values are similar, for example, 5 and 6 respectively, the Avalon-ST interface on the source side fails and the `sop` and `eop` overlap.

**Affected Configurations**

This issue affects all variable decoder designs.

**Design Impact**

The design fails.

**Workaround**

This issue has no workaround.

**Solution Status**

This issue will be fixed in a future version of the Reed-Solomon Compiler.

**Display Symbol Button in IP Toolbench is Missing**

The **Display Symbol** button in IP Toolbench does not appear, even though the screenshot in the user guide implies it should appear.

**Affected Configurations**

This issue affects all designs.

**Design Impact**

There is no design impact.

**Workaround**

This issue has no workaround.

**Solution Status**

This issue will be fixed in a future version of the Reed-Solomon Compiler.
Verilog HDL Designs Do Not Simulate in Synopsys VCS

When you simulate a Reed-Solomon Verilog HDL design in Synopsys VCS (2006.06-SP1), you receive an error message.

**Affected Configurations**
This issue affects all Verilog HDL designs.

**Design Impact**
You cannot simulate a Verilog HDL design in VCS.

**Workaround**
There is currently no workaround.

**Solution Status**
This issue will be fixed in a future release of the Reed-Solomon Compiler.

No Symbol In IP Toolbench Symbol Window

When you click Display Symbol, IP Toolbench does not always display a symbol.

**Affected Configurations**
This issue affects all configurations.

**Design Impact**
There is no design impact.

**Workaround**
To see a symbol, click Step 1: Parameterize, click Finish, click Display Symbol.

**Solution Status**
This issue will be fixed in a future version of the Reed-Solomon Compiler.

File Summary Does Not List All Generated Files

The file summary on the IP Toolbench Generate window does not always list all the generated files.

**Affected Configurations**
This issue affects all configurations.

**Design Impact**
There is no design impact.

**Workaround**
In the Parameterize window, when you finish parameterizing your variation, do not click Finish, just go to IP Toolbench and click Generate.
Solution Status
This issue will be fixed in a future version of the Reed-Solomon Compiler.

Cannot Find Memory Initialization File if Not in Project Directory
The Quartus II software cannot find the memory initialization files (HEX files) required by the design and issues a critical warning of the form:

Critical Warning: Can't find Memory Initialization File or Hexadecimal (Intel-Format) File C:/temp/mlab_test/fir_test0_coef_0.hex -- setting all initial values to 0

Affected Configurations
This issue is observed when the generated IP files are not in the same directory as your project setting files .qsf and .qpf files. For example, if your project involves many submodules and each submodule resides in a separate subdirectory.

Design Impact
The Quartus II software issues critical warnings for the missing files and generates a functionally incorrect netlist due to the missing memory initialization files.

Workaround
Add the path of the folder containing your generated IP files to the user libraries parameter in the .qsf file. For example, if your top level project directory is C:/myprojects/bigSystem and you have generated the Reed Solomon module in C:/myprojects/bigSystem/RSmodule/.

In your project's .qsf file (in C:/myprojects/bigSystem), look for a line that starts

set_global_assignment -name USER_LIBRARIES ...

Append the IP directory C:/myprojects/bigSystem/RSmodule with the following code:

set_global_assignment -name USER_LIBRARIES "C:/altera/72/ip/reed_solomon/lib;C:/myprojects/bigSystem/RSmodule"

After you save your changes, recompile your project and check that the critical warning is no longer displayed.

Solution Status
This issue will be fixed in a future version of the Reed-Solomon Compiler.
Revision History

Table 20–1 shows the revision history for the RLDRAM II MegaCore® function.

For more information on the new features, refer to the RLDRAM II MegaCore Function User Guide.

Table 20–1. RLDRAM II MegaCore Function Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.1</td>
<td>15 November 2008</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>8.0</td>
<td>15 May 2008</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>7.2</td>
<td>October 2007</td>
<td>Maintenance release.</td>
</tr>
</tbody>
</table>

Errata

Table 20–2 shows the issues that affect the RLDRAM II MegaCore function v8.1, 8.0, and 7.2.

Not all issues affect all versions of the RLDRAM II MegaCore function.

Table 20–2. RLDRAM II MegaCore Function Errata

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Nov 08</td>
<td>RLDRAM II Verilog HDL Design Doesn’t Work</td>
<td>✔</td>
</tr>
<tr>
<td></td>
<td>Error when Upgrading</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>Use Undelayed DQS Signal As Write Clock for the Example Driver FIFO</td>
<td>—</td>
</tr>
<tr>
<td>01 Dec 06</td>
<td>NativeLink Fails with the ModelSim® Simulator</td>
<td>✔</td>
</tr>
<tr>
<td>01 Nov 06</td>
<td>Add an RLDRAM II Controller to a Project with Other Memory Controllers</td>
<td>✔</td>
</tr>
<tr>
<td></td>
<td>Simulating with the NCsim Software</td>
<td>✔</td>
</tr>
<tr>
<td></td>
<td>Simulating with the VCS Simulator</td>
<td>✔</td>
</tr>
<tr>
<td></td>
<td>Multiple Instances of the auk_ddr_functions.vhd File</td>
<td>✔</td>
</tr>
<tr>
<td></td>
<td>Gate-Level Simulation Filenames</td>
<td>✔</td>
</tr>
<tr>
<td></td>
<td>Unpredictable Results for Gate-Level Simulations (HardCopy® II Devices only)</td>
<td>✔</td>
</tr>
<tr>
<td></td>
<td>Editing the Custom Variation (non-DQS Mode)</td>
<td>✔</td>
</tr>
</tbody>
</table>

RLDRAM II Verilog HDL Design Doesn’t Work

If you generate a Verilog HDL instance of the RLDRAM II Controller version 8.1, the design will not work in hardware or simulation.
Affected Configurations
This issue affects all Verilog HDL configurations. VHDL designs are not affected.

Workaround
If you require a Verilog HDL instance of the RLDRAM II Controller MegaCore function, you can use one of the following workarounds:

- Continue to use your existing version 8.0 instance. There are no functional changes between versions 8.0 and 8.1 of the RLDRAM II Controller MegaCore function, so you are not required to upgrade.
- If you choose to update your existing instance or if you do not have a version 8.0 instance, change all instances of the line:
  ```
  else if (0)
  ```
  to
  ```
  else if (1)
  ```
  in the following files:
  - `<variation name>_auk_rldramii_addr_cmd_reg.v`
  - `<variation name>_auk_rldramii_dqs_group.v`
  - `<variation name>_auk_rldramii_pipeline_addr_cmd.v`
  - `<variation name>_auk_rldramii_pipeline_qvld.v`
  - `<variation name>_auk_rldramii_pipeline_rdata.v`
  - `<variation name>_auk_rldramii_pipeline_wdata.v`

Some files may only require editing if pipeline options are enabled in your RLDRAM II Controller MegaCore variation.

Design Impact
Your design will not work in hardware or simulation.

Solution Status
This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

Error when Upgrading
If you upgrade an existing custom variation of the RLDRAM II MegaCore function to a newer version, for example from v7.1 to v7.2, the following error occurs:

```
Error (10430): VHDL Primary Unit Declaration error at
auk_rldramii_functions.vhd(5): primary unit "auk_rldramii_functions"
already exists in library "work"
```

IP Toolbench adds files to your Quartus® II project when you generate your custom variation. When you upgrade your MegaCore function, the same files from the previous and current versions are present in the same Quartus II project, which causes a VHDL error.
Affected Configurations
This issue affects all designs that were created in a previous version of the MegaCore function and then upgraded.

Workaround
From your Quartus II project, remove the Device Design Files that were added by the earlier version of the MegaCore function. These files can be identified by the files’ directory names.

Design Impact
You cannot compile your Quartus II project until you remove the duplicate files.

Solution Status
This issue is fixed in v8.1 of the RLDRAM II Controller MegaCore function.

Use Undelayed DQS Signal As Write Clock for the Example Driver FIFO
The RLDRAM II Controller in version 8.0 of the Quartus II uses undelayed DQS signal for the FIFO write clock, instead of delayed DQS signal as in the previous versions of the controller. Due to this change, the MegaWizard® now generates timing constraints for this path based on the fastest FPGA speed grade and 333-MHz RLDRAM II devices. In addition, DTW also generates similar timing constraints for both the Classic and TimeQuest Timing Analyzer. You need to disable the assignments from the MegaWizard after you rerun DTW.

1 If you are using a different speed grade for the FPGA or RLDRAM II device, you need to calculate the constraints manually. You may get the FPGA numbers from the DC & Switching Characteristics chapter in volume 1 of the Stratix II Handbook. The value for the FPGA uncertainties is always 200 ps regardless of speed grade.

1 You still need these assignments even when you are not using a FIFO to synchronize your capture data from the IOE. These constraints serve as the constraints for your IOE-to-core paths as long as you use the undelayed DQS signal to resynchronize data from the IOE registers in the FPGA core.

Affected Configurations
This issue affects all designs that were created in a previous version of the MegaCore function using the Quartus II version 7.2SP3 or lower.

Design Impact
You will not get accurate timing results on your IOE-to-core transfer unless you perform the workaround.

Workaround
From your Quartus II project, regenerate the RLDRAM II core, rerun DTW and make the manual SDC and TAN modifications as described.
MegaWizard-generated TAN Constraints

When generating an RLDRAM II core in Quartus II version 8.0, the MegaWizard generates the required IOE-to-core assignment for used with the Classic Timing Analyzer. The timing constraints are between capture registers and the FIFO where you need to add setup and hold relationship from the capture data to the FIFO. They look as follows:

```plaintext
set_instance_assignment -name HOLD_RELATIONSHIP "0.753 ns" -from *dqs_group_1|dq_captured_rising* -to * -tag sii_legacy_rlii_core
set_instance_assignment -name SETUP_RELATIONSHIP "2.247 ns" -from *dqs_group_1|dq_captured_rising* -to * -tag sii_legacy_rlii_core
set_instance_assignment -name HOLD_RELATIONSHIP "0.753 ns" -from *dqs_group_1|dq_captured_falling* -to * -tag sii_legacy_rlii_core
set_instance_assignment -name SETUP_RELATIONSHIP "2.247 ns" -from *dqs_group_1|dq_captured_falling* -to * -tag sii_legacy_rlii_core
set_instance_assignment -name HOLD_RELATIONSHIP "0.285 ns" -from *dqs_group_0|dq_captured_rising* -to * -tag sii_legacy_rlii_core
set_instance_assignment -name SETUP_RELATIONSHIP "2.715 ns" -from *dqs_group_0|dq_captured_rising* -to * -tag sii_legacy_rlii_core
set_instance_assignment -name HOLD_RELATIONSHIP "0.285 ns" -from *dqs_group_0|dq_captured_falling* -to * -tag sii_legacy_rlii_core
set_instance_assignment -name SETUP_RELATIONSHIP "2.715 ns" -from *dqs_group_0|dq_captured_falling* -to * -tag sii_legacy_rlii_core
set_instance_assignment -name HOLD_RELATIONSHIP "0.285 ns" -from *control_qvld* -to * -tag sii_legacy_rlii_core
set_instance_assignment -name SETUP_RELATIONSHIP "2.715 ns" -from *control_qvld* -to * -tag sii_legacy_rlii_core
```

The following assumptions are used to calculate the values for the setup and hold relationship above and the calculation is described below:

1. 300 MHz RLDRAM II device
2. FPGA in -3 speed grade
3. DQS Logic Block delay chain 3 usage
4. Board skew of 50 ps

Note that these constraints are pessimistic, as in a 300-MHz design, 2 delay chains are used instead of 3.

The FIFO clock always uses QK0 for write clock, such that the timing relationship for data transfer captured by QK0 is calculated as follows:

Setup relationship

\[
\text{Setup relationship} = \frac{t\text{CK}}{2} - 0.1 t\text{CK} - \text{FPGA uncertainties} - \frac{t\text{DQS}_{\text{PHASE,JITTER}}}{2} - \frac{t\text{DQS}_{\text{PSERR}}}{2} \\
= 3.333 - 0.333 - 200 - 90/2 (3-stage) - 75/2 (3 stage, -3 speed grade) \\
= 2.718 \text{ ns}
\]

Hold relationship

\[
\text{Hold relationship} = \text{FPGA uncertainties} + \frac{t\text{DQS}_{\text{PHASE,JITTER}}}{2} + \frac{t\text{DQS}_{\text{PSERR}}}{2} \\
= 200 + 90/2 + 75/2 \\
= 283 \text{ ps}
\]

If your RLDRAM II device has 2 QK signals, the timing relationship between the data captured by QK1 and the FIFO is calculated as follows:
Setup relationship  
= tCK - 0.1 tCK - FPGA uncertainties - tDQS_PHASE_JITTER/2 - 
tDQS_PSERR/2 - board skew - QK_QK skew  
= 3333 - 333 - 200 - 90/2 - 75/2 - 50 - 420  
= 2247 ps  

Hold relationship = FPGA uncertainties + tDQS_PHASE_JITTER/2 + 
tDQS_PSERR/2 + board skew + QK_QK skew  
= 200+ 90/2 + 75/2 + 50 + 420  
= 753 ps  

DTW-generated SDC and TAN Constraints  
The DTW also generates constraints for these paths in terms of clock uncertainties for 
both Classic Timing Analyzer and TimeQuest Timing Analyzer usage. These 
constraints are more accurate as they take into account your actual RLDRAM II 
device, your target FPGA speed grade, the number of DQS Logic Block delay chains 
used in the design, and your actual board skews.  

The following is an example of the SDC constraints for a 300-MHz RLDRAM II design  
in a Stratix® II C3 speed grade with 20ps board skew. The design uses 2 DQS Logic 
Block delay chains. 

# Specifies the setup uncertainty of transfers within each QK clock 
domain:  
# Clock Setup Uncertainty = 0.1 * tCK + fpga_tMINMAX_VARIATION + 
# fpga_tDQS_PHASE_JITTER + fpga_tDQS_PSERR  
# = 0.1 * 3.333 + 0.2 + 0.03 + 0.025  
# = 0.5883  
foreach {from_node} [list {rldramii_qk[0]}] {  
    foreach {to_node} [list {rldramii_qk[0]}] {  
        set_clock_uncertainty -setup 0.588 -from $from_node -to $to_node 
    }  
}  
foreach {from_node} [list {rldramii_qk[1]}] {  
    foreach {to_node} [list {rldramii_qk[1]}] {  
        set_clock_uncertainty -setup 0.588 -from $from_node -to $to_node 
    }  
}  

# Specifies the hold uncertainty of transfers within each QK clock 
domain:  
# Clock Hold Uncertainty = fpga_tMINMAX_VARIATION + 
# fpga_tDQS_PHASE_JITTER  
# + fpga_tDQS_PSERR  
# = 0.2 + 0.03 + 0.025  
# = 0.255  
foreach {from_node} [list {rldramii_qk[0]}] {  
    foreach {to_node} [list {rldramii_qk[0]}] {  
        set_clock_uncertainty -hold 0.255 -from $from_node -to $to_node 
    }  
}  
foreach {from_node} [list {rldramii_qk[1]}] {  
    foreach {to_node} [list {rldramii_qk[1]}] {  
        set_clock_uncertainty -hold 0.255 -from $from_node -to $to_node 
    }  
}  

# Specifies the uncertainty of any transfers between the QK clock 
domains:
Table 20–3 shows the TAN constraints created by DTW.

<table>
<thead>
<tr>
<th>From</th>
<th>To</th>
<th>Assignment Name</th>
<th>Value (ns)</th>
<th>Enabled</th>
</tr>
</thead>
<tbody>
<tr>
<td>rldramii_qk[0]</td>
<td>rldramii_qk[0]</td>
<td>Clock Setup Uncertainty</td>
<td>0.588</td>
<td>Yes</td>
</tr>
<tr>
<td>rldramii_qk[1]</td>
<td>rldramii_qk[1]</td>
<td>Clock Setup Uncertainty</td>
<td>0.588</td>
<td>Yes</td>
</tr>
<tr>
<td>rldramii_qk[0]</td>
<td>rldramii_qk[1]</td>
<td>Clock Setup Uncertainty</td>
<td>1.033</td>
<td>Yes</td>
</tr>
<tr>
<td>rldramii_qk[1]</td>
<td>rldramii_qk[0]</td>
<td>Clock Setup Uncertainty</td>
<td>1.033</td>
<td>Yes</td>
</tr>
<tr>
<td>rldramii_qk[0]</td>
<td>rldramii_qk[0]</td>
<td>Clock Hold Uncertainty</td>
<td>0.255</td>
<td>Yes</td>
</tr>
<tr>
<td>rldramii_qk[1]</td>
<td>rldramii_qk[1]</td>
<td>Clock Hold Uncertainty</td>
<td>0.255</td>
<td>Yes</td>
</tr>
<tr>
<td>rldramii_qk[0]</td>
<td>rldramii_qk[1]</td>
<td>Clock Hold Uncertainty</td>
<td>0.699</td>
<td>Yes</td>
</tr>
<tr>
<td>rldramii_qk[1]</td>
<td>rldramii_qk[1]</td>
<td>Clock Hold Uncertainty</td>
<td>0.699</td>
<td>Yes</td>
</tr>
</tbody>
</table>

You need to disable the setup and hold relationship assignments created by the MegaWizard Plug-In Manager if you are using DTW assignments for Classic Timing Analyzer to avoid double-counting.

**Solution Status**

This issue is fixed in v8.0 of the RLDRAM II Controller MegaCore function.
**NativeLink Fails with the ModelSim® Simulator**

When using NativeLink to run VHDL gate-level simulations using the ModelSim software, the simulation fails with the following error message:

```
# ** Error: (vcom-19) Failed to access library 'altera' at "altera".
```

**Affected Configurations**
The issue affects VHDL gate-level simulations.

**Design Impact**
The design does not simulate.

**Workaround**
The following lines need to be added to the NativeLink-generated gate-level simulation script:

```
vlib vhdl_libs/altera
vmap altera vhdl_libs/altera
vcom -work altera <Quartus installation directory>/libraries/vhdl/altera/altera_europa_support_lib.vhd
```

**Solution Status**
This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

---

**Add an RLDRAM II Controller to a Project with Other Memory Controllers**

If you try to generate a new RLDRAM II controller in a project that already contains a DDR, DDR2, QDRII, or RLDRAM II controller, the example design gets corrupted and the compilation fails.

**Affected Configurations**
This issue affects all configurations.

**Design Impact**
The design does not compile.

**Workaround**
To workaround this issue, follow these steps:

1. Generate the RLDRAM II controller in a new project and update the required project to instantiate the new RLDRAM II controller.
2. Copy the constraints from the new RLDRAM II project to the target project.
3. Copy the new RLDRAM II design files into the target project directory.

**Solution Status**
This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.
Simulating with the NCSim Software

The RLDRAM II Controller MegaCore function does not fully support the NCSim software.

Affected Configurations
This issue affects all configurations.

Design Impact
The design does not simulate.

Workaround
Set the -relax switch for all calls to the VHDL or Verilog HDL analyzer.

Solution Status
This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

Simulating with the VCS Simulator

The RLDRAM II Controller MegaCore function does not fully support the VCS simulator.

Affected Configurations
This issue affects all configurations.

Design Impact
The design does not simulate.

Workaround
For VHDL simulations, in the <variation name>_example_driver.vhd file, change all when statements from:

```vhdl
when std_logic_vector'("<bit_pattern>")
```
to:

```vhdl
when "<bit_pattern>"
```

Solution Status
This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

Multiple Instances of the auk_ddr_functions.vhd File

When a project contains multiple memory MegaCore functions, the Quartus II project has multiple instances of the auk_ddr_functions.vhd file (one per MegaCore function).

Affected Configurations
This issue affects all configurations.
Design Impact
The Quartus II project fails during compilation.

Workaround
Remove the `auk_ddr_functions.vhd` file associated with the RLDRAM II controller from the list of files added to the Quartus II project, by choosing Add/Remove Files from Project (Project menu). Keep only the `auk_ddr_functions.vhd` file associated with the DDR or DDR2 SDRAM controller.

Solution Status
This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

Gate-Level Simulation Filenames
Various Quartus II software options may cause it to generate a netlist with a different filename to that expected by the gate-level simulation script. The simulation script expects `<project name>.vho` or `.vo` and `<project name>_v or _vhd.sdo` files to be present.

Affected Configurations
This issue affects all configurations.

Design Impact
You cannot run gate-level simulations.

Workaround
For VHDL gate-level simulations, in the `simulation/modelsim` directory follow these steps:

1. Rename `<filename>.vho` file to `<project name>.vho`.
2. Rename `<filename>.sdo` file to `<project name>_vhd.sdo`.

For Verilog HDL gate-level simulations, in the `simulation/modelsim` directory follow these steps:

1. Rename the `<filename>.vo` file to `<project name>.vo`.
2. Rename the `<filename>.sdo` file to `<project name>_v.sdo`.
3. In the `<project name>.vo` file change the following line to point to the `<project name>_v.sdo` file:

   ```
   initial $sdf_annotate("<project name>_v.sdo");
   ```

Solution Status
This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

Unpredictable Results for Gate-Level Simulations (HardCopy II Devices only)
Gate-level simulations may not work as expected on HardCopy II devices, because HardCopy II timing is preliminary in the Quartus II software.
Affected Configurations
This issue affects all configurations on HardCopy II devices.

Design Impact
There is no design impact.

Workaround
This issue has no workaround.

Solution Status
This issue will be fixed in a future version of the Quartus II software.

Editing the Custom Variation (non-DQS Mode)
When you generate a non-DQS mode custom variation with large databus widths, you may encounter one of the following characteristics when you try to edit the custom variation:

■ IP Toolbench does not reload
■ IP Toolbench reloads, but the databus width and constraints are set to the default for the selected RLDRAM II device
■ IP Toolbench reloads, but the databus width is set to the default value for the selected RLDRAM II device and the constraints floorplan shows no chosen byte groups

Affected Configurations
This issue affects non-DQS mode designs only.

Design Impact
There is no design impact, if you implement the workaround.

Workaround
Use one of the following workarounds:

■ If IP Toolbench does not reload, you must regenerate a new custom variation and re-enter your parameters
■ If IP Toolbench reloads, but the databus width and constraints are set to the default, reselect the databus width and rechoose the byte groups in the constraints floorplan
■ If IP Toolbench reloads, but the databus width is set to the default and the constraints floorplan shows no byte groups, reselect the databus width and rechoose the byte groups in the constraints floorplan

Solution Status
This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.
Revision History

Table 21–1 shows the revision history for the SDI MegaCore® function.

For more information on the new features, refer to the SDI MegaCore Function User Guide.

Table 21–1. SDI MegaCore Function Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>Support for Stratix® IV devices.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Added GX transceiver based core for Arria® GX devices.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Improved receiver lock algorithm — minimization of resets between standards changes and improved tolerance of corrupt SDI streams.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Updated 425MB support.</td>
</tr>
<tr>
<td>7.2</td>
<td>September 2007</td>
<td>Support for Arria GX devices.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Support for SMPTE 425MB dual link 1080i standard.</td>
</tr>
</tbody>
</table>

Errata

Table 21–2 shows the issues that affect the SDI MegaCore function v8.1, 8.0, and 7.2.

Not all issues affect all versions of the SDI MegaCore function.

Table 21–2. SDI MegaCore Function Errata

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Nov 08</td>
<td>Quartus® II Fitter Reports Error When PLL-Generated Clock of 67.5 MHz Used in Stratix GX</td>
<td>8.1 8.0 7.2</td>
</tr>
<tr>
<td></td>
<td>Example Designs Are Out of Date</td>
<td></td>
</tr>
<tr>
<td>15 May 08</td>
<td>NativeLink Fails with ModelSim® Simulator</td>
<td>8.1 8.0 7.2</td>
</tr>
<tr>
<td></td>
<td>SMPTE425MB Multiplexing Scheme is Incorrect</td>
<td></td>
</tr>
<tr>
<td>01 Mar 08</td>
<td>Timing Not Met in C5 Speed Grade Stratix II GX Devices</td>
<td>8.1 8.0 7.2</td>
</tr>
</tbody>
</table>

Quartus® II Fitter Reports Error When PLL-Generated Clock of 67.5 MHz Used in Stratix GX

The Quartus II fitter reports error when you use PLL-generated clock inputs of 67.5 MHz frequency in SDI-SD MegaCore targeting Stratix GX.
Affected Configurations
This issue affects all Stratix GX SDI-SD MegaCore functions with PLL-generated clock inputs of 67.5 MHz frequency.

Design Impact
The design cannot be fitted in the device.

Workaround
Set the input clock to 29.7 MHz frequency so that the PLL generates the frequency of the output clock to 74.25 MHz.

Solution Status
This issue will be fixed in a future version of the SDI MegaCore function.

Example Designs Are Out of Date
The example designs and testbenches included in the simulation directory were generated with v7.2 of the SDI MegaCore function. They must be updated before they can be used correctly with v8.0 of the SDI MegaCore function.

Affected Configurations
This issue affects HD-SDI, HD-SDI 3G and HD-SDI dual-link examples in the simulation directory.

Design Impact
The example designs do not successfully simulate. There is no impact on your design.

Workaround
The three examples require different steps to upgrade them in order to work with v8.0 of the SDI MegaCore function.

- To simulate the HD-SDI example, which is stored in the simulation/hdsdi directory, you must regenerate the SDI instance by opening it in the version 8.0 of the MegaWizard® and clicking Finish. You must also update the testbench by connecting upper 11 bits of the 22 bit transmit line number signal to zero, as shown below:

```vhdl
hd_duplex hd_duplex_inst
  ...
  .tx_ln  ( {11'b0, gen_ln} ), // connect the upper 11 bits to zero
);
```

- To simulate the HD-SDI 3G example, which is stored in the simulation/hdsdi_3g directory, you must regenerate the SDI instance by opening it in the version 8.0 of the MegaWizard and clicking Finish. You must also update the testbench by adding the connections to SDI instance and connecting upper 11 bits of the 22 bit transmit line number signal to zero, as shown below:
hd_3g_duplex hd_3g_duplex_inst
(
  ...
  .gxb2_cal_clk (sdi_ref), // required for hard serdes designs
  .tx_data_valid_a_bn (1'b1),
  .tx_data_type_a_bn (1'b1),
  .tx_ln  {11'b0, gen_ln} ), // connect the upper 11 bits to zero
);

■ To simulate the HD-SDI dual-link example, which is stored in the
  simulation/hdsdi_dual_link directory, you must regenerate the SDI instance by
  opening it in the version 8.0 of the MegaWizard and clicking Finish. No changes
  are required to the testbench.

**Solution Status**
This issue is fixed in version 8.1 of the SDI MegaCore function.

**NativeLink Fails with ModelSim® Simulator**
When using NativeLink to run simulations with the ModelSim simulator, the
testbench fails.

**Affected Configurations**
This issue affects all configurations.

**Design Impact**
The design does not simulate and the testbench reports a failure.

**Workaround**
Use the ModelSim simulation scripts provided by Altera or carry out the following
steps:
1. Edit the NativeLink generated script to command
   “vsim -t 100fs”.
2. Reexecute the script in ModelSim.

**Solution Status**
This issue will be fixed in a future version of the SDI MegaCore function.

**SMPTE425MB Multiplexing Scheme is Incorrect**
The SDI MegaCore function uses an incorrect multiplexing of video data for the
425MB stream. In addition, the SDI MegaCore Function User Guide shows this incorrect
multiplexing.

**Affected Configurations**
This issue affects the following cores when carrying the 425MB format of 3-Gbps SDI
data:

■ 3-Gbps SDI receiver, transmitter, and duplex
■ Triple standard receiver, transmitter, and duplex
Design Impact
The design impact for the transmitter and receiver is different.

Transmitter
The line number insertion feature of the core does not perform correctly.

Receiver
The core correctly performs the CRC checking. However, two of the four CRC error flags are transposed. If there is an error on the luma channel of virtual channel B, the core indicates an error on the chroma channel of virtual channel A. This mapping is fixed.

The extracted line number (LN) for virtual channel A is output for both virtual channels. The LN for one of the virtual channels is not correctly extracted.

Workaround
There is a workaround for the transmitter and a workaround for the receiver.

Transmitter
Figure 21–1 shows how you should format the data and the control signals to provide.

Figure 21–1. Correct 425MB Transmitter Mapping

You can perform the LN insertion outside the core.
Refer to the relevant SMPTE specification for placement and encoding of these data words.

Receiver
Figure 21–2 shows how the output of a receiver core presents data.

Figure 21–2. Correct 425MB Receiver Mapping

You can swap the \texttt{crc} \texttt{c} flag of virtual channel A with the \texttt{crc} \texttt{y} flag of virtual channel B in your design.
For the LN insertion, you can perform the LN extraction outside the core.
Refer to the relevant SMPTE specification for placement and encoding of these data words.
Solution Status
This issue is fixed in version 8.0 of the SDI MegaCore function.

Timing Not Met in C5 Speed Grade Stratix II GX Devices
The 3-Gbps and triple rate variants of the SDI MegaCore function may not meet the timing requirements in the C5 speed grade device of the Stratix II GX device family.

Affected Configurations
This issue affects the 3-Gbps and triple-rate SDI MegaCore functions.

Design Impact
Your design does not meet timing requirements.

Workaround
Use either a C4 or C3 speed grade device.

Solution Status
This issue will be fixed in a future version of the SDI MegaCore function.
 Revision History

Table 22–1 shows the revision history for the SerialLite II MegaCore® function.

For more information on the new features, refer to the *SerialLite II MegaCore Function User Guide*.

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>8.0 SP1</td>
<td>July 2008</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>Preliminary support Stratix® IV devices.</td>
</tr>
<tr>
<td>7.2</td>
<td>October 2007</td>
<td>Added <em>gxbl_powerdown</em> signal to ease merging of multiple SerialLite II cores into the same transceiver block.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Added VHDL testbench for some configurations.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Moved the ALT2GXB megafunction instantiation into a separate file to ease post-generation changes.</td>
</tr>
</tbody>
</table>

Errata

Table 22–2 shows the issues that affect the SerialLite II MegaCore v8.1, 8.0, and 7.2.

Not all issues affect all versions of the SerialLite II MegaCore.

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Nov 08</td>
<td>Demo Testbench Cannot Be Simulated With Arria® GX Variants Generated Using IP 8.0 in Quartus® II 8.1</td>
<td>8.1 8.0 SP1 8.0 7.2</td>
</tr>
<tr>
<td></td>
<td>Timing Analyzer Reports “Critical Warning: Timing Requirements Not Met”</td>
<td>Fixed</td>
</tr>
<tr>
<td></td>
<td>Stratix IV Internal Core Clocking Is Incorrect for a Design Using TSIZE = 2 and Data Rate &gt; 3125 Mbps</td>
<td>Fixed</td>
</tr>
<tr>
<td>15 May 08</td>
<td>Link Management FIFO May Overflow When Small Packets Are Sent Continuously Over a Long Period of Time.</td>
<td>— Fixed</td>
</tr>
<tr>
<td></td>
<td>Rx Only Mode With Clock Compensation Does Not Support All Reference Clock Selections</td>
<td>— Fixed</td>
</tr>
<tr>
<td>01 Dec 06</td>
<td>Generation Fails or Corrupt Variation Generated if Asymmetric Broadcast Mode Used</td>
<td>— Fixed</td>
</tr>
</tbody>
</table>

© 1 November 2008 Altera Corporation  Library Version 8.1  MegaCore IP Library Release Notes and Errata
Demo Testbench Cannot Be Simulated With Arria® GX Variants Generated Using IP 8.0 in Quartus® II 8.1

When the SerialLite II MegaCore version 8.0 is generated using the Quartus II software version 8.1, the demonstration testbench simulation script targets Stratix II GX libraries, instead of the required Arria GX libraries. A syntax error occurs indicating a required library is missing.

Affected Configurations
This issue affects all variations of the SerialLite II version 8.0 designs compiled in the Quartus II software version 8.1, targeting the Arria GX family.

Design Impact
The demonstration testbench simulation is unable to run.

Workaround
Upgrade the IP to version 8.1, and regenerate your configuration.

If you are unable to upgrade the IP, follow these steps:

1. Open the `<variation name>_run_modelsim.tcl` script.
2. Locate the Quartus II Libraries section of the file, and add the following commands:
   ```
   append libraries {arriagx arriagx_hssi }
   append lib_files {{arriagx_atoms.v} {arriagx_hssi_atoms.v} }
   ```

Solution Status
This issue is fixed in v8.1 of the SerialLite II MegaCore function.

Timing Analyzer Reports “Critical Warning: Timing Requirements Not Met”

The Quartus II TimeQuest Timing Analyzer reports that certain SerialLite II designs fail to meet timing requirements on one of the following clocks:

- `slite2_top_inst|xcvr_inst|alt4gxb_component|auto_generated|transmit_pcs0|clkout`
- `slite2_top_inst|xcvr_inst|alt4gxb_component|auto_generated|receive_pcs0|clkout`

The failure is a negative hold slack, normally a very small figure (less than 0.05ns).

Affected Configurations
This issue affects selected SerialLite II designs targeting the Stratix IV family.

Design Impact
The design may fail to function properly on hardware if the TimeQuest Timing Analyzer reports that timing requirements are not met.
Workaround
Add this command into the `<quartus project name>.qsf` file:
```
set_global_assignment -name OPTIMIZE_HOLD_TIMING "ALL PATHS"
```
or

Follow these steps:
1. Open the Quartus II software.
2. On the Assignments menu, click Settings and select Fitter Settings.
3. Enable the Optimize hold timing; option and select All paths from the drop-down menu.
4. Click OK to save your settings.

Solution Status
This issue is fixed in v8.1 of the SerialLite II MegaCore function.

Stratix IV Internal Core Clocking Is Incorrect for a Design Using TSIZE = 2 and Data Rate > 3125 Mbps

Due to an error in the transceiver parameters, a variation using Stratix IV, TSIZE = 2 and a data rate greater than 3125 Mbps, fails to use the proper transceiver clocking.

Affected Configurations
This issue affects all SerialLite-II variations using Stratix IV, transfer size of 2 and a data rate greater than 3125 Mbps.

Design Impact
While simulation works fine, this design does not meet the timing requirements on the transceiver output clocks. This likely results in data errors if implemented in hardware.

Workaround
Open the generated transceiver wrapper file (`<variation name>_slite2_xcvr.v`) in a text editor. Make the following changes to the alt4gxb component defparam section:
```
// Change:
alt4gxb_component.rx_rate_match_fifo_mode = "normal", // Change (Was None)
alt4gxb_component.rx_use_clkout="false", // Change (Was True)
// Add:
alt4gxb_component.rx_rate_match_pattern1 = "00110000111010000011", // Add
alt4gxb_component.rx_rate_match_pattern2 = "11001111000101111100", // Add
alt4gxb_component.rx_rate_match_pattern_size = 20, // Add
alt4gxb_component.rx_use_rate_match_pattern1_only = "false", // Add
```

Solution Status
This issue is fixed in v8.1 of the SerialLite II MegaCore function.
Link Management FIFO May Overflow When Small Packets Are Sent Continuously Over a Long Period of Time.

For configurations that have Enable flow control option turned on and small packets are sent continuously for a significant amount of time (more than 50 clock cycles), the processing of the link management packets will be delayed indefinitely. This causes the Link Management FIFO to overflow. Small packet means packet with sizes equal to or less than \((\text{TSIZE} \times \text{TX_NUM_LANES})\) bytes.

**Affected Configurations**

This issue affects all configurations that have Enable flow control option turned on, and when small packets are sent continuously over the link for a long period of time.

**Design Impact**

The link management FIFO will overflow, and flow control gets delayed indefinitely, resulting in loss of data.

**Workaround**

Do not send small packets continuously for a long period of time. Allow a few idle clock cycles in between the small packets every 20 clock cycles.

**Solution Status**

This issue is fixed in v8.0 SP1 of the SerialLite II MegaCore function.

Rx Only Mode With Clock Compensation Does Not Support All Reference Clock Selections

For a Non-Stratix GX receiver only configuration with Clock Compensation turned on, the GUI currently allows multiple reference clock selections. Choosing a reference clock frequency in mode less than \(\text{RefFreq} = \text{DRATE} / (\text{TSIZE} \times 10)\), causes the rate match FIFO to overflow.

**Affected Configurations**

This issue affects all receiver only SerialLite-II variations in a Non-Stratix GX family when Clock Compensation is turned on, with the reference clock set to a frequency less than \(\text{DRATE} / (\text{TSIZE} \times 10)\).

**Design Impact**

The internal rate match FIFO will overflow, causing data loss.

**Workaround**

Do not use a lower frequency reference clock.

or

Turn off Clock Compensation in this configuration. The data will be transmitted out of the Rx core on the rrefclk domain instead of the trefclk domain.

**Solution Status**

Configurations that cause this error can no longer be generated.
Generation Fails or Corrupt Variation Generated if Asymmetric Broadcast Mode Used

The SerialLite II MegaCore function fails to generate or generates corrupted variations that use the broadcast mode in an asymmetric configuration.

If the state machine is not self-synchronized, the syntax error shown in Figure 22–1 appears and the generation fails. If the state machine is self-synchronized, an invalid configuration is generated, data is corrupted, and the testbench fails.

Affected Configurations

This issue affects configurations that use the broadcast mode and for which the transmitter number of lanes does not equal the receiver number of lanes (asymmetric).

Design Impact

If the state machine is not self-synchronized, the syntax error shown in Figure 22–1 appears and the generation fails. If the state machine is self-synchronized, an invalid configuration is generated, data is corrupted, and the testbench fails.

Workaround

If the self-synchronized state machine is required, use the MegaWizard® interface to generate a transmitter-only broadcast variation. Use the MegaWizard interface again to generate a single lane receiver-only self-synchronized variation. Then instantiate as many of these receiver variations as required to match the number of lanes needed.

You cannot select options such as retry-on-error and flow control for your workaround variation.

If self-synchronized state machine is not required, there is no workaround other than to use a self-synchronized state machine and configure the system as previously described.

Solution Status

Configurations that cause this error can no longer be generated.
Revision History

Table 23–1 shows the revision history for the Triple Speed Ethernet MegaCore® function.

For more information on the new features, refer to the Triple Speed Ethernet MegaCore Function User Guide.

Table 23–1. Triple Speed Ethernet MegaCore Function Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>Support for dynamic reconfiguration.</td>
</tr>
<tr>
<td>8.0 SP1</td>
<td>July 2008</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>■ Preliminary support for Stratix® IV device family.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Support for multi-port MAC.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Option to exclude internal FIFOs during synthesis.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Support for RGMII in fast Ethernet (10/100 Mbps).</td>
</tr>
<tr>
<td>7.2</td>
<td>October 2007</td>
<td>■ Preliminary support for Stratix III device family.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ New configuration option—Small MAC, a compact version of MAC which utilizes less combinational, and ALUT resources.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ New synthesis options—pause frames generation and detection, magic packet detection, and VLAN packet detection and classification support.</td>
</tr>
</tbody>
</table>

Errata

Table 23–2 shows the issues that affect the Triple Speed Ethernet MegaCore function v8.1, 8.0 SP1, 8.0, and 7.2.

Not all issues affect all versions of the Triple Speed Ethernet MegaCore function.

Table 23–2. Triple Speed Ethernet MegaCore Function Errata

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>Issue</td>
<td>8.1</td>
</tr>
<tr>
<td>01 Dec 08</td>
<td>✓</td>
</tr>
<tr>
<td>Connection Point Validation Failed in SOPC Builder</td>
<td></td>
</tr>
<tr>
<td>Intermittent Payload Corruption When 32-Bit Byte Alignment is On</td>
<td></td>
</tr>
<tr>
<td>Testbench Compilation Fails When Using Nativelink with ModelSim</td>
<td>✓</td>
</tr>
</tbody>
</table>
### Table 23–2. Triple Speed Ethernet MegaCore Function Errata

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Nov 08</td>
<td>Limited Multi-Channel Support in Cyclone III and Arria GX Device Families</td>
<td>✔ ✔ ✔</td>
</tr>
<tr>
<td></td>
<td>Timing Not Met in 12-Port Configurations Targeting Stratix IV Devices</td>
<td>✔ ✔ ✔</td>
</tr>
<tr>
<td></td>
<td>Incorrect Number of Packets Received During Simulation</td>
<td>Fixed ✔ ✔</td>
</tr>
<tr>
<td></td>
<td>Simulation Fails in NC Sim When Using VHDL Testbench</td>
<td>Fixed ✔ ✔</td>
</tr>
<tr>
<td></td>
<td>Bit SW_RESET Doesn’t Get Cleared After Software Reset</td>
<td>Fixed ✔ ✔</td>
</tr>
<tr>
<td></td>
<td>Simulation Fails in ModelSim</td>
<td>Fixed ✔ ✔</td>
</tr>
<tr>
<td></td>
<td>Incorrect Detection of PHY</td>
<td>Fixed ✔ ✔</td>
</tr>
<tr>
<td>15 May 08</td>
<td>Non-Compliant Implementation of Bit PAGE_RECEIVE in PCS Register</td>
<td>✔ ✔ ✔ ✔</td>
</tr>
<tr>
<td></td>
<td>Non-Compliant Implementation of AlignmentError Statistics Counter</td>
<td>✔ ✔ ✔</td>
</tr>
<tr>
<td></td>
<td>Software Driver Aligns Good Data</td>
<td>Fixed ✔ ✔</td>
</tr>
<tr>
<td></td>
<td>Software Driver Doesn’t Update ENA_10 When Operating Speed Changes</td>
<td>Fixed ✔ ✔</td>
</tr>
<tr>
<td></td>
<td>to 10 Mbps</td>
<td>Fixed ✔ ✔</td>
</tr>
<tr>
<td></td>
<td>Late Collision Not Detected in Small MAC 10/100 Mbps</td>
<td>Fixed ✔ ✔</td>
</tr>
<tr>
<td>01 Mar 08</td>
<td>Intermittent Corrupted Packets Received on Avalon Streaming Interface</td>
<td>Fixed ✔ ✔</td>
</tr>
<tr>
<td></td>
<td>When Byte Shifting is Used</td>
<td></td>
</tr>
<tr>
<td>15 Oct 07</td>
<td>Using Nativelink with VCS Simulator Fails</td>
<td>Fixed ✔ ✔</td>
</tr>
</tbody>
</table>

### Connection Point Validation Failed in SOPC Builder

The connection point validation for SOPC Builder systems that contain the MAC block without internal FIFOs and the PCS block with embedded GXB PMA fails. This variation of the Triple Speed Ethernet MegaCore function contains two unassociated clocks, `rx_afull_clk` and `cal_blk_clk`, when SOPC Builder only allows for one unassociated clock.

#### Affected Configuration

This issue affects all SOPC Builder systems that contain the core variation 10/100/1000 Ethernet MAC with 1000BASE-X/SGMII PCS with the following options:

- Use internal FIFO is turned off.
- Use transceiver block and GXB are selected.

#### Workaround

None.

#### Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.
Intermittent Payload Corruption When 32-Bit Byte Alignment is On

The payload is occasionally corrupted when 32-bit byte alignment is turned on in MACs without internal FIFOs.

Affected Configuration

This issue affects all configurations that contain the core variations 10/100/1000 Mbps Ethernet MAC only or 10/100/1000 Mbps Ethernet MAC with 1000BASE-X/SMII PCS with the following options:

- Use internal FIFO is turned off
- Align packet headers to 32-bit boundaries is turned on

Workaround

None.

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Testbench Compilation Fails When Using Nativelink with ModelSim

The following error occurs during the testbench compilation when Nativelink is used with ModelSim:

```
# ** Error: (vlog-7) Failed to open design unit file
"D:/altera/81/ip/altera/triple_speed_ethernet/lib/altera_tse_alt2gxb_gige.vo" in read mode.
# No such file or directory. (errno = ENOENT)
# Error in macro ./tse_run_msim_rtl_verilog.do line 9
```

This error is caused by a wrong extension in the Nativelink Tcl script.

Affected Configuration

This issue affects all configurations with the following characteristics:

- Targets Stratix II GX or Arria GX.
- Contains the core variation 10/100/1000 Ethernet MAC with 1000BASE-X/SGMII PCS or 1000BASE-X/SGMII PCS.
- The option Use transceiver block is turned on.

Workaround

Edit the script `tse_run_msim_rtl_<verilog/phdl>.do` and change the extension of `altera_tse_alt2gxb_gige.vo` to `.v`.

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.
Limited Multi-Channel Support in Cyclone III and Arria GX Device Families

Full multi-channel support is not available in configurations targeting Cyclone® III and Arria GX device families due to device limitations. In these device families, only up to 12 ports are supported.

Affected Configuration
All.

Workaround
None.

Solution Status
This information will be added in a future version of the Triple Speed Ethernet User Guide.

Timing Not Met in 12-Port Configurations Targetting Stratix IV Devices

Required timing is not met in 12-port configurations that target Stratix IV device family and implement LVDS I/O.

Affected Configuration
This issue affects only 12-port configurations that implement LVDS I/O targetting Stratix IV device family.

Workaround
None.

Solution Status
This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Simulation Fails in ModelSim

Simulating the MegaCore function in ModelSim fails when the MegaCore function is generated in Verilog with RGMII selected. The core includes needless MII signals in the top-level file, thus conflicting with the signal definition in the loopback module.

Affected Configuration
This issue affects all configurations that are instantiated in SOPC Builder with RGMII and Verilog selected.

Workaround
Remove the MII signals from the top-level file generated by the SOPC Builder.

Solution Status
This issue is fixed in version 8.1 of the Triple Speed Ethernet MegaCore function.
Incorrect Detection of PHY

The software driver of the Triple Speed Ethernet MegaCore function detects Marvell 88E1145 as Marvell 88E1111 and National DP83848C as National DP83865. In the latter, the MAC operating speed and duplex mode are wrongly configured.

Affected Configuration
This issue affects all configurations.

Workaround
Replace line 1206 in altera_avalon_tse.c to the following line:

```c
if((pphy_profiles[i]->oui == oui) && (pphy_profiles[i]->model_number == model_number))
```

Solution Status
This issue is fixed in version 8.1 of the Triple Speed Ethernet MegaCore function.

Non-Compliant Implementation of Bit PAGE_RECEIVE in PCS Register

The Triple Speed Ethernet MegaCore function sets the PAGE_RECEIVE bit in the PCS register an_expansion to 1 when a /C/ ordered set is received. This does not comply with the IEEE 802.3 Standard clause 37.

Affected Configuration
This issue affects all configurations that include the PCS function.

Workaround
None.

Solution Status
This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Non-Compliant Implementation of aAlignmentError Statistics Counter

The Triple Speed Ethernet MegaCore function increments the aAlignmentError statistics counter when an SFD error is encountered. This does not comply with the IEEE 802.3 Standard clause 5.2.2.1.7.

Affected Configuration
This issue affects all configurations.

Workaround
None.

Solution Status
This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.
Incorrect Number of Packets Received During Simulation

At the end of a simulation, the number of packets received by the MAC in affected configurations is one packet less than expected. The MAC is expected to receive the same number of packets generated by the frame generator and sent to the MAC. This is due to the algorithm used by the simulation model in initializing the memory block in the PCS receive FIFO converter.

Affected Configuration

This issue affects all configurations that contain 10/100/1000 Mbps Ethernet MAC with 1000BASE-X/SGMII PCS core variations with the following options:

- Generated in Verilog HDL.
- Use internal FIFO is turned off.
- Use transceiver block is turned on.
- Enable SGMII bridge logic is turned on.

Workaround

None.

Solution Status

This issue is fixed in version 8.1 of the Triple Speed Ethernet MegaCore function.

Simulation Fails in NC Sim When Using VHDL Testbench

The signal `prmbl_len` ranges from 0 to 15 in the VHDL testbench files (*.tb.vhd) but from 0 to 40 in the frame generator files (ethgen2.vhd and ethgen.vhd). The NC Sim simulator is more stringent in its checking thus failing the simulation.

Affected Configurations

This issue affects all configurations in VHDL simulated in the NC Sim simulator.

Workaround

Before running the simulation, change the upper range 15 to 40 in the following line in the VHDL testbench files (*.tb.vhd):

```vhdl
prmble_len : in integer range 0 to 15; -- length of preamble
```

Solution Status

This issue is fixed in version 8.1 of the Triple Speed Ethernet MegaCore function.

Bit SW_RESET Doesn’t Get Cleared After Software Reset

When a software reset is triggered by setting the SW_RESET bit in the command_config register to 1, the bit doesn’t get cleared at the end of the software reset.
Affected Configurations
This issue affects all configurations that contain the multi-port MAC function with the options Use internal FIFO and Implement statistics counter turned off.

Workaround
Set the bits SW_RESET and CNT_RESET in the command_config register to trigger a software reset.

Solution Status
This issue is fixed in version 8.1 of the Triple Speed Ethernet MegaCore function.

Software Driver Aligns Good Data
The software driver doesn’t differentiate aligned data from unaligned data thus aligning both. This results in unnecessary processing time.

Affected Configuration
This issue affects all configurations.

Design Impact
The performance drops when the payload is sent in small packets.

Workaround
Replace the condition in line 540 in the source file ins_tse_mac.c to the following condition:

```
if(((unsigned int)data & 0x03) == 0)
```

Solution Status
This issue is fixed in version 8.0 SP1 of the Triple Speed Ethernet MegaCore function.

Software Driver Doesn’t Update Bit ENA_10 When Operating Speed Changes to 10 Mbps
The ENA_10 bit in the command_config register, which is directly wired to the signal ena_10, is not updated by the software driver accordingly when the operating speed of the MAC changes to 10Mbps.

Affected Configuration
This issue affects configurations in RGMII mode that use the provided software driver and rely on the signal ena_10 to determine the speed of the MAC.

Design Impact
The design stops working when the operating speed changes to 10 Mbps.

Workaround
Edit the source files as shown in Table 23–3.
Late Collision Not Detected in Small MAC 10/100 Mbps

By definition, late collisions are collisions that happen after the first 64 bytes are sent. The Triple Speed Ethernet MegaCore function does not detect collisions that happen on the 65th and 66th byte as late collisions. Hence, such instances of late collisions are not properly handled and results in incomplete retransmission.

Affected Configuration

This issue affects all configurations that contain the Small MAC 10/100 Mbps function.

Workaround

None.

Solution Status

This issue is fixed in version 8.1 of the Triple Speed Ethernet MegaCore function.

Intermittent Corrupted Packets Received on Avalon Streaming Interface When Byte Shifting is Used

Corrupted packets are intermittently received on the MAC’s Avalon Streaming (Avalon-ST) interface when the byte shifting feature is used. The actual payload length of the corrupted packets doesn’t match the LENGTH field in the packet.

Affected Configuration

All configurations that use the 16-bit byte shifting feature.
**Workaround**
None.

**Solution Status**
This issue is fixed in version 8.0 of the Triple Speed Ethernet MegaCore function.

**Using Nativelink with VCS Simulator Fails**
Using the Quartus® II NativeLink feature with the VCS simulator results in the following error:

```
Error: VCS: Parsing design file
/tools/altera/7.2/150/linux/ip/triple_speed_ethernet/lib/
altera_tse_<custom variation>.v
Error: VCS: Top Level Modules:
Error: VCS: altera_tse_<custom variation>
Error: VCS: Error-[URMI] Instances with unresolved modules remain in the
design.
Error: VCS: Invalid instantiation at: 
Error: VCS: /tools/altera/7.2/150/linux/ip/triple_speed_ethernet/lib/
altera_tse_<custom variation>.v
```

**Affected Configuration**
This issue affects all configurations that are simulated with the VCS simulator.

**Workaround**
When you encounter this error, add `altera_tse_<custom variation>.v` in the MegaCore function variation file, `<variation name>.v/hd`, under the related files section.

Example:

```
// ===============================
// Triple Speed Ethernet Wizard Data
// ===============================
// Retrieval info: </MEGACORE>
// ===============================
...
// RELATED_FILES: nativelink.v,altera_tse_<custom variation>.v;
// IPFS_FILES: nativelink.vo;
// ===============================
```

**Solution Status**
This issue is fixed in version 8.0 of the Triple Speed Ethernet MegaCore function.
Revision History

Table 24–1 shows the revision history for the UTOPIA Level 2 Master MegaCore® function.

For more information on the new features, refer to the UTOPIA Level 2 Master MegaCore Function User Guide.

Table 24–1. UTOPIA Level 2 Master MegaCore Function Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>Full support for Stratix® III devices.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>• Full support for Cyclone® III devices</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Preliminary support for Stratix IV devices</td>
</tr>
<tr>
<td>7.2</td>
<td>October 2007</td>
<td>Maintenance release.</td>
</tr>
</tbody>
</table>

Errata

There are no issues that affect the UTOPIA Level 2 Master MegaCore function v8.1, 8.0, and 7.2.
Revision History

Table 25–1 shows the revision history for the UTOPIA Level 2 Slave MegaCore® function.

For more information on the new features, refer to the UTOPIA Level 2 Slave MegaCore Function User Guide.

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>Full support for Stratix® III devices.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>■ Full support for Cyclone® III devices&lt;br&gt;■ Preliminary support for Stratix IV devices</td>
</tr>
<tr>
<td>7.2</td>
<td>October 2007</td>
<td>Maintenance release.</td>
</tr>
</tbody>
</table>

Errata

There are no issues that affect the UTOPIA Level 2 Slave MegaCore function v8.1, 8.0, and 7.2.
26. Video and Image Processing Suite

Revision History

Table 26–1 shows the revision history of the Video and Image Processing Suite MegaCore® functions.

For information on the new features, refer to the Video and Image Processing Suite User Guide.

Table 26–1. Video and Image Processing Suite Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
</table>
| 8.1     | November 2008 | ■ Added new Test Pattern Generator.  
 ■ The Deinterlacer supports pass-through mode and run-time algorithm switching.  
 ■ The Deinterlacer and Frame Buffer support clock crossing for improved external memory access efficiency.  
 ■ The Clocked Video Input and Clocked Video Output support run-time switching between standard definition (SD) and high definition (HD) video streams.  
 ■ The Color Space Converter supports run-time changing of coefficients.  
 ■ The Gamma Corrector supports parallel data processing for three channels.  
 ■ The 2D FIR Filter supports run-time changing of coefficients.  
 ■ Full support for Stratix® III devices.  
 ■ Withdrawn support for UNIX. |
| 8.0 SP1 | July 2008   | ■ Fixed several errata issues (see Table 26–2).                                                                   |
| 8.0     | May 2008    | ■ Added new Clipper, Clocked Video Input, Clocked Video Output, Frame Buffer, and Color Plane Sequencer MegaCore functions.  
 ■ All MegaCore functions now support 2,600 pixels height and width.  
 ■ Alpha Blending Mixer and Deinterlacer support parallel processing for 1080p60.  
 ■ Full support for Cyclone® III devices.  
 ■ Preliminary support for Stratix IV devices. |
| 7.2     | October 2007 | ■ The Deinterlacer now supports a new motion adaptive algorithm and double or triple buffering in external RAM.  
 ■ The Color Space Converter, Chroma Resampler, Gamma Corrector, 2D FIR Filter, 2D Median Filter, Alpha Blending Mixer, Scaler and Deinterlacer MegaCore functions can now be directly instantiated in SOPC Builder.  
 ■ The Alpha Blending Mixer now has a control register map for run-time control of the resolutions for each layer being mixed.  
 ■ The Chroma Resampler now has a control register map that supports run-time control of the image size, luma adaptive filtering and parallel color channel processing.  
 ■ The Color Space Converter and 2D filter have enhanced controls for output type conversion and now support half-even rounding.  
 ■ All MegaCore functions have full support for Arria® GX devices. |
Errata

Table 26–2 shows the issues that affect the Video and Image Processing Suite MegaCore® functions v8.1, v8.0 SP1, v8.0, and v7.2.

Not all issues affect all versions of the Video and Image Processing Suite MegaCore function.

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Nov 08</td>
<td>The 2D Median Filter Does Not Support 7×7 Filter Size</td>
<td>✔️  —  —  —</td>
</tr>
<tr>
<td></td>
<td>Misleading Error Message Issued by Color Plane Sequencer</td>
<td>✔️  —  —  —</td>
</tr>
<tr>
<td></td>
<td>Changing Target Device After Quartus II Compilation Causes Error</td>
<td>✔️  —  —  —</td>
</tr>
<tr>
<td></td>
<td>Active Picture Line Selection Should be Available for Separate Sync Mode</td>
<td>✔️  —  —  —</td>
</tr>
<tr>
<td></td>
<td>Control Port Behavior Unpredictable for Scaler and Clipper</td>
<td>Fixed ✔️ ✔️  —</td>
</tr>
<tr>
<td></td>
<td>Error in Clocked Video Output Constraint File</td>
<td>Fixed ✔️  —  —</td>
</tr>
<tr>
<td></td>
<td>Simulation Models Not Created For Clocked Video Functions</td>
<td>Fixed ✔️ ✔️  —</td>
</tr>
<tr>
<td></td>
<td>Cannot Connect Adapter in SOPC Builder For Multiple Parallel Planes</td>
<td>Fixed ✔️ ✔️  —</td>
</tr>
<tr>
<td></td>
<td>Line Buffer Compiler Does Not Generate for Arria GX</td>
<td>Fixed ✔️ ✔️  —</td>
</tr>
<tr>
<td></td>
<td>Misleading Warning Message for Color Plane Sequencer</td>
<td>Fixed ✔️ ✔️  —</td>
</tr>
<tr>
<td></td>
<td>Color Plane Sequencer Does Not Report GUI Messages</td>
<td>Fixed ✔️ ✔️  —</td>
</tr>
<tr>
<td></td>
<td>HEX Files for Simulation in SOPC Builder Systems Must be Moved</td>
<td>Fixed ✔️ ✔️ ✔️</td>
</tr>
<tr>
<td>15 Jul 08</td>
<td>Deinterlacer Fails to Generate in Some Configurations</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>Color Plane Sequencer Shows Parallel Bit Ranges in Reverse Order</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>Clipper Fails to Send EOP When Active Region is Bottom Right</td>
<td>—</td>
</tr>
<tr>
<td>15 Jul 08</td>
<td>File Name Clash for Files Generated by Clocked Video Functions</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>The F Falling Edge Line Clocked Video Output Parameter Not Loaded</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>Layers Supported by Alpha Blending Mixer Incorrect in User Guide</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>Addendum to the Alpha Blending Mixer Functional Description</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>Control Register Map for the Clipper Missing From User Guide</td>
<td>—</td>
</tr>
<tr>
<td>15 May 08</td>
<td>SOPC Builder Avalon-ST Adapter Does Not Support Avalon-ST Video</td>
<td>✔️  ✔️  ✔️  —</td>
</tr>
<tr>
<td></td>
<td>v7.2 MegaCore Functions Not Compatible with v8.X Quartus II</td>
<td>✔️  ✔️  ✔️  —</td>
</tr>
<tr>
<td></td>
<td>Packets Sent to VIP Cores Must Have Non-Empty Payload</td>
<td>✔️  ✔️  ✔️  —</td>
</tr>
<tr>
<td></td>
<td>Scaler Resets Channel Configuration when SOPC Builder Restarts</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>Line Buffer Compiler Generates Non-Functional HDL</td>
<td>—</td>
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<tr>
<td></td>
<td>64-Bit Windows Not Supported for SOPC Builder or DSP Builder</td>
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<tr>
<td></td>
<td>Control Register Map Table for Alpha Blending Mixer is Incomplete</td>
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<tr>
<td></td>
<td>Deinterlacer Cannot be Simulated with Avalon-MM Master Ports</td>
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<tr>
<td></td>
<td>SOPC Builder Interface Can Become Temporarily Unresponsive</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>Cannot Interrupt Hardware Generation</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>Cannot Enable Clipping in Scaler if Resolution Less Than Window</td>
<td>—</td>
</tr>
</tbody>
</table>
Table 26–2. Video and Image Processing Suite Errata (Part 2 of 2)

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
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<tbody>
<tr>
<td>15 May 08</td>
<td>Output Directory Must be Same as Project Directory</td>
<td>8.1 8.0 SP1 8.0 7.2</td>
</tr>
<tr>
<td>01 Oct 07</td>
<td>Scalar Coefficients Preview Window Cannot be Closed</td>
<td>8.1 8.0 SP1 8.0 7.2</td>
</tr>
<tr>
<td></td>
<td>Scaler with Run-Time Control Enabled Can Give Incorrect Data</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Long Generation Time for the Scaler</td>
<td></td>
</tr>
<tr>
<td>01 May 07</td>
<td>Precision Must be Set When Using Lanczos Coefficients in Scaler</td>
<td>8.1 8.0 SP1 8.0 7.2</td>
</tr>
<tr>
<td>01 Dec 06</td>
<td>Cyclone II M4K Fails in Alpha Blending Mixer &amp; Gamma Corrector</td>
<td>8.1 8.0 SP1 8.0 7.2</td>
</tr>
</tbody>
</table>

**The 2D Median Filter Does Not Support 7×7 Filter Size**

The 2D Median Filter MegaCore function does not support the 7×7 filter size.

**Affected Configurations**

Configurations including the 2D Median Filter MegaCore function.

**Design Impact**

An error message is issued when generating the simulation model.

**Workaround**

There is no workaround. Do not select the 7×7 filter size.

**Solution Status**

This issue will be fixed in a future version of the Video and Image Processing Suite.

**Misleading Error Message Issued by Color Plane Sequencer**

If you try to enable both ports din1 and dout1 in the MegaWizard interface for the Color Plane Sequencer MegaCore function a misleading error message is issued stating that "dout0 and dout1 cannot both be enabled." The message should state "din1 and dout1 cannot both be enabled."

**Affected Configurations**

Configurations including the Color Plane Sequencer MegaCore function.

**Design Impact**

None.

**Workaround**

None needed.

**Solution Status**

This issue will be fixed in a future version of the Video and Image Processing Suite.
Changing Target Device After Quartus II Compilation Causes Error

Changing the target device in a family after compilation in the Quartus II software can cause an error with subsequent Quartus II compilations.

**Affected Configurations**

Any Video and Image Processing Suite MegaCore function when the target device is changed within the same device family.

**Design Impact**

The generation flow does not correctly identify the change to the target device. This causes the HDL generation to be skipped for subsequent Quartus II compilations, and results in the following error message when re-compiling:

```
Error (10481): VHDL Use Clause error at ***_GN.vhd**: design library "altera" does not contain primary unit "alt_cusp81_package"
```

**Workaround**

Remove the db directory from the project directory and re-compile in the Quartus II software.

**Solution Status**

This issue will be fixed in a future version of the Video and Image Processing Suite.

Active Picture Line Selection Should be Available for Separate Sync Mode

The **Active picture line** selection box should be available when **On separate wires** is selected for **Sync signals**.

**Affected Configurations**

This issue affects the Clocked Video Output MegaCore function when sync signals on separate wires are selected.

**Design Impact**

An incorrect active picture line is selected.

**Workaround**

Select **Embedded in video** to enable the selection box, then switch back to **On separate wires** after specifying the required active picture line. The specified value is used although it is shown dimmed in the selection box.

**Solution Status**

This issue will be fixed in a future version of the Video and Image Processing Suite.

Control Port Behavior Unpredictable for Scaler and Clipper

The run-time control port has unpredictable behavior for the Scaler and Clipper MegaCore functions.
Affected Configurations
Instantiations of the Scaler or Clipper MegaCore functions where the run-time control port is enabled.

Design Impact
Values on the Avalon-MM bus are captured correctly and re-captured after a few cycles. However, the second capture does not respect the chipselect and write signals. This may have unpredictable results: for example, write data being corrupted, or writes to one control register affecting other addresses within the slave.

Workaround
A patch is available from Altera customer support.

Solution Status
This issue is fixed in v8.1 of the Video and Image Processing Suite.

Error in Clocked Video Output Constraint File
There is an error in the .sdc file for the Clocked Video Output MegaCore function.

Affected Configurations
Configurations using the Clocked Video Output MegaCore function.

Design Impact
An error message is issued by the TimeQuest Timing Analyzer:
Warning: Ignored assignment: set_false_path -to [get_keepers (*alt_vip_IS2Vid:*|is_line_count_f0[*][*])]

Workaround
Edit the <install path>/ip/clocked_video_output/lib/alt_vip_cvo.sdc file and change line 71 from:
set_false_path -to [get_keepers (*alt_vip_IS2Vid:*|is_line_count_f0[*][*])]
to:
set_false_path -to [get_keepers (*alt_vip_IS2Vid:*|is_line_count_f0[*][*])]

Solution Status
This issue is fixed in v8.1 of the Video and Image Processing Suite.

Simulation Models Not Created For Clocked Video Functions
The simulation check box in SOPC Builder is not triggering generation of the simulation models for the clocked video MegaCore functions.

Affected Configurations
SOPC Builder configurations including the Clocked Video Input or Clocked Video Output MegaCore functions.
**Design Impact**
No simulation model is available.

**Workaround**
Use the MegaWizard Plug-In Manager to generate the simulation models by performing the following steps:

1. In the Quartus II software, open the MegaWizard Plug-In Manager (from the Tools menu).
2. Click **Edit an existing custom megafunction variation**.
3. Select the `.vhd` file that matches the name of the MegaCore function (as shown in SOPC Builder) and select the **Megafunction name** that corresponds to the MegaCore function (Clocked Video Input v8.0 or Clocked Video Output v8.0).
4. Click **Ok** to display the MegaWizard interface and verify that the parameterization of the user interface is as expected.
5. Click on the **EDA** tab. Select **Generate simulation model**, then click **Finish**.
The simulation model is generated.

**Solution Status**
This issue is fixed in v8.1 of the Video and Image Processing Suite.

**Cannot Connect Adapter in SOPC Builder For Multiple Parallel Planes**

In SOPC Builder, any Video and Image Processing Suite MegaCore function that supports the Avalon-ST Video protocol can connect to any other Video and Image Processing Suite MegaCore function without error.

However, connecting any v8.0 Video and Image Processing Suite component, with more than one color plane in parallel, to an Avalon-ST adapter or user IP component which supports Avalon-ST Video, may cause SOPC Builder to display an error message.

The message states that there is an empty signal associated with the adapter but there is no empty signal associated with the Video and Image Processing Suite MegaCore function:

```
Error: my_alt_vip_<vip core>.dout/<Avalon-ST Adapter>.in: The sink has a empty signal of <n> bits, but the source does not.
```

**Affected Configurations**
SOPC Builder configurations that connect an Avalon-ST adapter to a Video and Image Processing MegaCore function that is parameterized for more than one color plane in parallel.

**Design Impact**
There is currently no SOPC Builder adapter that supports connection between packet-based Avalon-ST components with greater than one symbol per beat and the Video and Image Processing Suite MegaCore functions that support the Avalon-ST Video protocol. Error messages are displayed in the SOPC Builder message window.
However, the Video and Image Processing Suite MegaCore functions do not require the empty signal and the resulting system is valid if the connecting component supports the Avalon-ST Video protocol.

**Workaround**
Ignore the error message, and generate the system by holding down the Ctrl key while clicking Generate.

**Solution Status**
This issue is fixed in v8.1 of SOPC Builder and the Video and Image Processing Suite.

**HEX Files for Simulation in SOPC Builder Systems Must be Moved**

When simulation files are generated in SOPC Builder, the .hex files are generated in a different location to the .vho/.vo files. These files must be moved to the same directory as the .vho/.vo files.

**Affected Configurations**
This issue affects all Video and Image Processing Suite MegaCore functions that generate HEX files when the simulation models are generated through SOPC Builder.

**Design Impact**
If the .hex files are not in the same directory as the .vho/.vo file which uses them, the simulator tool will not be able to find the .hex files when a simulation is run and issues an error. For example, ModelSim reports an error of the form:

```
# ** Error: (vsim-7) Failed to open VHDL file
"alt_vip_scl_gny?hwrrns_v_coeffs0_reg_file_contents.hex" in r mode.
# No such file or directory.
```

**Workaround**
After SOPC Builder has reported that system generation is complete, the .hex files contained in `<project directory>\db\sopc_sim\db` should be copied to the project directory.

**Solution Status**
This issue is fixed in v8.1 of the Video and Image Processing Suite.

**Deinterlacer Fails to Generate in Some Configurations**

Some configurations of the Deinterlacer MegaCore function may fail to compile in the Quartus II software or fail to generate simulation models.

**Affected Configurations**
This issue affects a very limited number of configurations using double or triple buffering when buffering more than one non-image data packet per field.
Design Impact
The following error messages are issued during analysis and synthesis:

Error: IP Generator Error: Can't synthesise function ker_reader (Can't synthesise operation ASSIGN(current_packet_id, VCALL(ALT_FIFO::read; FIELD(this, packets_write_to_read))))
Error: IP Generator Error: Errors occurred converting parse tree to CDFG

Workaround
A patch is available from Altera customer support.

Solution Status
This issue is fixed in v8.0 SP1 of the Video and Image Processing Suite.

Color Plane Sequencer Shows Parallel Bit Ranges in Reverse Order
The MegaWizard interface for the Color Plane Sequencer MegaCore function uses tables to represent the color pattern used by video data packets. The tables label the bit ranges used for color planes in parallel. This labeling is incorrect; the bit range label for the most significant bits should be at the bottom of the tables, and the bit range label for the least significant bits should be at the top of the tables.

Affected Configurations
Configurations including the Color Plane Sequencer MegaCore function.

Design Impact
The bit ranges may be entered in the wrong order.

Workaround
Ignore the bit range labels. The color planes which use the most significant bits of the interface are on the bottom of the tables, and the color planes that use the least significant bits are on the top of the tables.

Solution Status
This issue is fixed in v8.0 SP1 of the Video and Image Processing Suite.

Clipper Fails to Send EOP When Active Region is Bottom Right
The Clipper MegaCore function fails to send an endofpacket signal when the active region touches the bottom-right corner.

Affected Configurations
Clipper MegaCore function in offsets mode where the bottom offset and right offset are 0, or in Rectangle mode where top offset + height = input height and left offset + width = input width.

Design Impact
The control packet from the next frame is included at the end of the image data in the current frame, then endofpacket is sent late.
Workaround
None.

Solution Status
This issue is fixed in v8.0 SP1 of the Video and Image Processing Suite.

File Name Clash for Files Generated by Clocked Video Functions
The Clocked Video Input and Clocked Video Output MegaCore functions generate database files `sync.v` and `fifo.v` when Verilog HDL is selected. This may lead to file name clashes if there are user files with the same names.

Affected Configurations
Verilog HDL configurations including the Clocked Video Input or Clocked Video Output MegaCore functions.

Design Impact
Compilation errors when the design is compiled in the Quartus II software.

Workaround
Avoid using `sync.v` or `fifo.v` for user specified filenames in a design that includes the Clocked Video Input and Clocked Video Output MegaCore functions.

Solution Status
This issue is fixed in v8.0 SP1 of the Video and Image Processing Suite.

The F Falling Edge Line Clocked Video Output Parameter Not Loaded
The F falling edge line parameter for the Clocked Video Output MegaCore function is not used for preset loading.

Affected Configurations
Any configuration including the Clocked Video Output MegaCore function.

Design Impact
The preset interlaced parameter sets for 1080i60, NTSC and PAL are incorrect.

Workaround
Set a value for the F falling edge line parameter, save the variation and reload. The parameters are then loaded correctly.

Solution Status
This issue is fixed in v8.0 SP1 of the Video and Image Processing Suite.

Layers Supported by Alpha Blending Mixer Incorrect in User Guide
The Alpha Blending Mixer is restricted to a maximum of 12 layers not 16 as specified in the v8.0 user guide.
Solution Status

This issue is fixed in the Video and Image Processing Suite User Guide for v8.0 SP1.

Addendum to the Alpha Blending Mixer Functional Description

The following text was missing from the functional description of the Alpha Blending Mixer in the v8.0 user guide:

When Alpha blending is turned on, the Avalon-ST input ports for the alpha channels expect a video stream compliant with the Avalon-ST Video protocol. Alpha frames contain a single color plane and are transmitted in video data packets. The first value in each packet, transmitted while the startofpacket signal is high, contains the packet type identifier 0. This holds true even when the width of the alpha channels data ports is less than 4-bits wide. The last alpha value for the bottom-right pixel is transmitted while the endofpacket signal is high.

It is not necessary to send control packets to the ports of the alpha channels. The width and height of each alpha layer are assumed to match with the dimensions of the corresponding foreground layer although the Alpha Blending Mixer MegaCore function recovers gracefully in case of mismatch. All non-image data packets (control packets included) are ignored and discarded just before the processing of a frame starts.

Solution Status

This issue is fixed in the Video and Image Processing Suite User Guide for v8.0 SP1.

Control Register Map for the Clipper Missing From User Guide

The control register map for the Clipper MegaCore function was omitted from the v8.0 user guide.

Table 26–3 on page 26–10 describes the Clipper control register map.

The control data is read once at the start of each frame and is buffered inside the MegaCore function, so the registers may be safely updated during the processing of a frame.

<table>
<thead>
<tr>
<th>Address</th>
<th>Register</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Control</td>
<td>The zeroth bit of this register is the Go bit, all other bits are unused. Setting this bit to 0 causes the Clipper MegaCore function to stop the next time control information is read. Refer to “Avalon-MM Slave Interfaces” on page 4–17 of the Video and Image Processing Suite User Guide for full details.</td>
</tr>
<tr>
<td>1</td>
<td>Status</td>
<td>The zeroth bit of this register is the Status bit, all other bits are unused. The Clipper MegaCore function sets this address to 0 between frames. It is set to 1 while the MegaCore function is processing data and cannot be stopped. Refer to “Avalon-MM Slave Interfaces” on page 4–17 of the Video and Image Processing Suite User Guide for full details.</td>
</tr>
<tr>
<td>2</td>
<td>Left Offset</td>
<td>The left offset, in pixels, of the clipping window/rectangle. (Note 1)</td>
</tr>
<tr>
<td>3</td>
<td>Right Offset of Width</td>
<td>In clipping window mode, the right offset of the window. In clipping rectangle mode, the width of the rectangle. (Note 1)</td>
</tr>
<tr>
<td>4</td>
<td>Top Offset</td>
<td>The top offset, in pixels, of the clipping window/rectangle. (Note 2)</td>
</tr>
</tbody>
</table>
Table 26–3. Clipper Control Register Map (Part 2 of 2)

<table>
<thead>
<tr>
<th>Address</th>
<th>Register</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>Bottom Offset</td>
<td>In clipping window mode, the bottom offset of the window. In clipping rectangle mode, the height of the rectangle. (Note 2)</td>
</tr>
<tr>
<td></td>
<td>or Height</td>
<td></td>
</tr>
</tbody>
</table>

Note to Table 26–3:

(1) The left and right offset values must be less than or equal to the input image width.
(2) The top and bottom offset values must be less than or equal to the input image height.

Solution Status

This issue is fixed in the Video and Image Processing Suite User Guide for v8.0 SP1.

Line Buffer Compiler Does Not Generate for Arria GX

The Line Buffer Compiler MegaCore function does not generate for Arria GX devices.

Affected Configurations

Line Buffer Compiler MegaCore function in any parameterization targeting Arria GX devices.

Design Impact

The MegaCore function cannot be generated.

Workaround

None.

Solution Status

This issue is fixed in v8.1 of the Video and Image Processing Suite.

Misleading Warning Message for Color Plane Sequencer

The MegaWizard interface for the Color Plane Sequencer shows the warning message "Data rates of channels on din0 and dout0 are not equal, inefficient use of the pipeline will result" at all times and for all parameterizations. This warning should not be shown for parameterizations that use the processing pipeline at full efficiency.

Affected Configurations

All configuration using the Color Plane Sequencer MegaCore function.

Design Impact

None.

Workaround

The message can be ignored. However note that when converting from channels in parallel to channels in sequence or vice versa, the data rate of the streaming connection will be slowed to the data rate of the slowest input or output.
Solution Status
This issue is fixed in v8.1 of the Video and Image Processing Suite.

Color Plane Sequencer Does Not Report GUI Messages
The Color Plane Sequencer MegaCore function does not report information messages regarding the GUI behavior.

Affected Configurations
Configurations including the Color Plane Sequencer MegaCore function.

Design Impact
The MegaWizard interface has some controls which cannot enter an invalid state. When a value is entered that would specify an invalid state, the GUI reverts to the previous parameter setting without issuing an information message explaining why it has reverted its settings.

Workaround
Take extra care to ensure that your parameter values are valid and have been accepted.

Solution Status
This issue is fixed in v8.1 of the Video and Image Processing Suite.

SOPC Builder Avalon-ST Adapter Does Not Support Avalon-ST Video
In SOPC Builder, the Avalon-ST data adapter does not support the Avalon-ST Video protocol. No error message is currently displayed when connecting the components.

Affected Configurations
SOPC Builder configurations that connect an Avalon-ST adapter to a Video and Image Processing MegaCore function.

Design Impact
Connecting any Video and Image Processing Suite MegaCore function to an Avalon-ST data adapter results in a generated system in which the Avalon-ST video protocol is corrupted.

Workaround
To connect Video and Image Processing MegaCore functions which have a different number of planes in parallel, use the Color Plane Sequencer. For example to convert between 3 colors in parallel (3 symbols per beat) and 3 colors in sequence (1 symbol per beat).

Solution Status
It will not be possible to connect unsupported Avalon-ST adapters in a future version of SOPC Builder and the Video and Image Processing Suite.
v7.2 MegaCore Functions Not Compatible with v8.X Quartus II
The v7.2 Video and Image Processing Suite MegaCore functions are not compatible with v8.0 or v8.1 of the Quartus II software, SOPC Builder or DSP Builder.

Affected Configurations
All designs including v7.2 Video and Image Processing Suite MegaCore functions.

Design Impact
Errors are issued when you attempt to compile the design.

Workaround
Upgrade the MegaCore functions to v8.0 or v8.1.

Solution Status
This issue will be fixed in a future version of the Video and Image Processing Suite.

Packets Sent to VIP Cores Must Have Non-Empty Payload
The packets sent to Video and Image Processing Mega Core functions must have non-empty payload. If a packet is sent with a type but without any further information, the packet processing logic may enter an inconsistent state.

Affected Configurations
All configurations supporting Avalon-ST Video.

Design Impact
If a packet with an empty payload is received, the MegaCore function may not output correct data until a few non-empty packets have been received.

Workaround
If an empty packet is intended, send one symbol of data with it.

Solution Status
This issue will be fixed in a future version of the Video and Image Processing Suite.

Scaler Resets Channel Configuration when SOPC Builder Restarts
Closing and reopening SOPC Builder, then opening the MegaWizard resets the Color plane transmission format control to Sequence, and the Number of color planes control to 1.

Affected Configurations
This issue affects the Scaler MegaCore function when it is parameterized through SOPC Builder and the Color plane transmission format control is set to Parallel.
**Design Impact**
This issue could cause the Color plane transmission format and Number of color planes settings to become incorrect.

If affected instances of the Scaler MegaCore function are connected to other MegaCore functions, SOPC Builder reports these incorrect settings as an error, due to the symbols per beat of the Scaler not matching the symbols per beat of its source and sink. When the Scaler is re-parameterized the error will disappear.

**Workaround**
Check the parameterization and reset as necessary when SOPC Builder is started when a design is loaded containing a Scaler MegaCore function that uses Parallel for Color plane transmission format.

**Solution Status**
This issue is fixed in V8.0 of the Video and Image Processing Suite.

**Line Buffer Compiler Generates Non-Functional HDL**
The Line Buffer Compiler generates non-functional HDL for some parameterizations.

**Affected Configurations**
This issue affects configurations of the Line Buffer Compiler when the number of lines is one and the line width is also one.

**Design Impact**
Compilation fails with an error message of the form:

VHDL error: range direction of object slice must be same as range direction of object File

**Workaround**
None.

**Solution Status**
This issue is fixed in v8.0 of the Video and Image Processing Suite.

**64-Bit Windows Not Supported for SOPC Builder or DSP Builder**
The Video and Image Processing Suite MegaCore functions do not support 64-bit Windows operating systems when instantiated using SOPC Builder or DSP Builder.

**Affected Configurations**
This issue affects all MegaCore functions in the Video and Image Processing Suite when the MegaCore functions are instantiated using SOPC Builder or DSP Builder.

**Design Impact**
Compilation fails with an error message of the form:

Error: IP Generator Error: Unable to start JAVA virtual machine
Workaround

None.

Solution Status

This issue is fixed in v8.0 of the Video and Image Processing Suite.

Control Register Map Table for Alpha Blending Mixer is Incomplete

The v7.2 user guide states that addresses 2–6 in the control register map for the Alpha Blending Mixer are unused, but addresses 2 and 3 are the width and height of the background layer. Addresses 4–6 are still unused.

Solution Status

This issue is fixed in v8.0 of the *Video and Image Processing Suite User Guide*.

Deinterlacer Cannot be Simulated with Avalon-MM Master Ports

If the Avalon-MM master ports on the Deinterlacer MegaCore function are connected to DSP Builder Avalon-MM Master blocks then Simulink detects algebraic loops and cannot simulate.

Affected Configurations

This issue affects the Deinterlacer v7.2 MegaCore function with double or triple buffering selected.

Design Impact

The design can be synthesized as normal, but simulation cannot be performed in Simulink.

Workaround

The issue occurs because Avalon-MM masters have to respond combinatorially to their `waitrequest` port. This means that the `waitrequest` ports on the Deinterlacer have to be marked as direct-feed through so that Simulink can simulate them correctly. However, if Simulink finds a loop where an output of a block could drive an input to the same block via only direct feed-through connections then an algebraic loop is reported and simulation cannot be performed.

This happens when the Deinterlacer’s master ports are connected to the Avalon-MM Master block because the master block is also direct-feed through, and Simulink cannot see that its `waitrequest` input is only connected to its `waitrequest` output.

The issue can be worked around by incorrectly asserting to Simulink that the `waitrequest` port of the Deinterlacer is not direct-feed through. This does have the limitation that if `waitrequest` is ever set high during the simulation then the simulation results are incorrect. The Altera External RAM simulation block does not assert `waitrequest` unless it is specifically configured to do so in its GUI, so this allows some level of simulation to be performed.

To mark the port as delayed rather than direct feed through, there are two options. Either:

1. Download the *Video Processing Reference Design* from the Altera website.
2. Open example_design_data_path.mdl.
3. Copy and paste the block named algebraic_loop_cut_dil into your design.
   Or:
   1. Click on the Deinterlacer MegaCore function block to select it.
   2. In the MATLAB command window, type:

   ```matlab
   set(gca,'inDelayed', regexpr(get(gca,'inDelayed'),'0','1'));
   ```

   **Solution Status**
   This issue is fixed in v8.0 of DSP Builder.

**SOPC Builder Interface Can Become Temporarily Unresponsive**

When a MegaCore function is parameterized in the SOPC Builder tool, changing the value of controls which affect the size or number of ports of the MegaCore can cause the user interface to become unresponsive for several seconds.

**Affected Configurations**

This issue affects all MegaCore functions in the Video and Image Processing Suite when the MegaCore functions are parameterized through SOPC Builder.

**Design Impact**

This interface appears to be unresponsive, however waiting for a short while is all that is necessary.

**Workaround**

Change the controls only when necessary, and where possible directly enter values into controls to avoid intermediate parameter steps.

**Solution Status**

This issue is fixed in v8.0 of the Video and Image Processing Suite.

**Cannot Interrupt Hardware Generation**

The Cancel button in the MegaCore function Generation Report window may not immediately take effect because the "Generating hardware..." stage will only respond to an interrupt once it has completed.

**Affected Configurations**

This issue affects all MegaCore functions in the Video and Image Processing Suite when you are using the MegaWizard Plug-In Manager flow but is not a issue for the DSP Builder or SOPC Builder flows.

**Design Impact**

The hardware generation phase must be allowed to complete. This may take several minutes. You can then exit from the generation report window and re-invoke the MegaWizard Plug-In Manager to update the MegaCore function.
Workaround
You must wait until the hardware generation phase has been completed.

Solution Status
This issue is fixed in v8.0 of the Video and Image Processing Suite.

Cannot Enable Clipping in Scaler if Resolution Less Than Window
Clipping in the Scaler cannot be enabled when the input resolution is smaller than the value shown for the clipping window.

Affected Configurations
This issue affects configurations of the Scaler MegaCore function where the input resolution is smaller than the disabled value for the clipping window (default 1024×768).

Design Impact
Clipping cannot be enabled.

Workaround
Set the input resolution to be larger than the clipping resolution. Then enable clipping and make the clipping window small enough to be inside the required input resolution. Set the input resolution as required.

Solution Status
This issue is fixed in v8.0 of the Video and Image Processing Suite. (Clipping is now performed by a separate MegaCore Function.)

Output Directory Must be Same as Project Directory
The output directory specified in the MegaWizard interface must be the same as the project directory.

Affected Configurations
This issue affects all MegaCore functions in the Video and Image Processing Suite.

Design Impact
If the output directory of a MegaWizard interface generated file is different from the project directory, an error is issued the generation fails to complete.

Workaround
Specify the same directory for your output files and the Quartus II project.

Solution Status
This issue is fixed in v8.0 of the Video and Image Processing Suite.
Scalar Coefficients Preview Window Cannot be Closed

The Scalar Coefficients Preview window cannot be closed when it is used in SOPC Builder.

Affected Configurations
This issue affects the Scalar MegaCore Function when it is parameterized in the SOPC Builder flow.

Design Impact
This issue does not prevent you from parameterizing the Scalar and therefore has no design impact.

Workaround
The Coefficient Preview window will close when you close the main Scalar parameterization interface.

Solution Status
This issue will be fixed in a future version of the Video and Image Processing Suite.

Scaler with Run-Time Control Enabled Can Give Incorrect Data

The Scaler MegaCore function can produce too little data and incorrect values in a small set of configurations.

Affected Configurations
This issue affects the v7.1 Scaler MegaCore function with run-time resolution control enabled and the input/output sizes set to be unequal. (These sizes refer to the maximums that values that can be set during run time.) All filtering algorithms are affected.

Design Impact
When the run-time registers are set to scale video streams down, there may be too little output data and the data will have incorrect values.

Workaround
Set the input/output resolutions to be the same, and large enough to cope with the largest values you intend to set at run time.

Solution Status
This issue is fixed in a v7.2 of the Video and Image Processing Suite.

Long Generation Time for the Scaler

The generation time for some configurations of the Scaler MegaCore function can be several hours.
**Affected Configurations**

This issue affects configuration of the Scaler MegaCore function with more than nine horizontal and nine vertical taps used in conjunction with run-time control.

**Design Impact**

Selecting run-time control in conjunction with a large number of taps (more than nine) can cause long generation times. For example, a scaler with 16 horizontal taps and 16 vertical taps may take three hours to generate.

**Workaround**

There is no workaround.

**Solution Status**

This issue is fixed in version 7.2 of the Video and Image Processing Suite.

### Precision Must be Set When Using Lanczos Coefficients in Scaler

When configuring the Scaler MegaCore function, you must choose the correct coefficient precision when using Lanczos coefficients.

**Affected Configurations**

This issue affects configurations of the Scaler MegaCore function using the polyphase algorithm with Lanczos coefficients.

**Design Impact**

The MegaCore function fails to generate.

**Workaround**

If you select polyphase mode with Lanczos coefficients, you must set the coefficient precision to be signed with one integer bit. Fraction bits can be set within the full range available in the MegaWizard interface.

**Solution Status**

The coefficient precision restriction will be enforced in future versions of the Video and Image Processing Suite.

### Cyclone II M4K Fails in Alpha Blending Mixer & Gamma Corrector

M4K block write operations may fail for Cyclone II devices with the Alpha Blending Mixer and Gamma Corrector MegaCore functions.

**Affected Configurations**

This issue affects configurations using Cyclone II devices and the Alpha Blending Mixer or Gamma Corrector MegaCore function.
Design Impact

The following error message is issued:

```
Error: M4K memory block WYSIWYG primitive
"vhdl_gam vhdl_gam_inst|TTA_X_smem_av:gamma_lut|altsyncram:ds1:altsyncram_component|altsyncram_rvh1:auto_generated|ram_block1a0" utilizes the dual-port dual-clock mode. However, this mode is not supported in Cyclone II device family in this version of Quartus II software. Please refer to the Cyclone II FPGA Family Errata Sheet for more information on this feature.
```

Workaround

If you are targeting any affected revision (Rev a or b of the 2c35 or Rev a of any other Cyclone II part), set the CYCLONEII_SAFE_WRITE variable to RESTRUCTURE. This causes the Quartus II software to fix the issue at a cost in M4Ks and Fmax. If you are using a newer revision device, set the CYCLONEII_SAFE_WRITE variable to VERIFIED_SAFE which turns off the error message.

Solution Status

This issue has been fixed for the latest silicon devices but remains an issue if you are using the earlier silicon.

Refer to the Cyclone II FPGA Family Errata Sheet for more information about this issue.
Revision History

Table 27–1 shows the revision history for the Viterbi Compiler.

For more information on the new features, refer to the Viterbi Compiler User Guide.

Table 27–1. Viterbi Compiler Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>Full support for Stratix® III devices.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>■ Full support for Cyclone® III devices</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Preliminary support for Stratix IV devices</td>
</tr>
<tr>
<td>7.2</td>
<td>October 2007</td>
<td>Maintenance release.</td>
</tr>
</tbody>
</table>

Errata

Table 27–2 shows the issues that affect the Viterbi Compiler v8.1, 8.0, and 7.2.

Not all issues affect all versions of the Viterbi Compiler.

Table 27–2. Viterbi Compiler Errata

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 Nov 08</td>
<td>Display Symbol Button in IP Toolbench is Missing</td>
<td>✓</td>
</tr>
<tr>
<td>15 May 08</td>
<td>IP Functional Simulation Model Fails</td>
<td>✓ ✓ –</td>
</tr>
<tr>
<td>01 Oct 07</td>
<td>File Summary Does Not List All Generated Files</td>
<td>✓ ✓ –</td>
</tr>
<tr>
<td>01 Jul 07</td>
<td>Trellis Mode Fails</td>
<td>✓ ✓ ✓</td>
</tr>
</tbody>
</table>

Display Symbol Button in IP Toolbench is Missing

The Display Symbol button in IP Toolbench does not appear, even though the screenshot in the user guide implies it should appear.

Affected Configurations

This issue affects all designs.

Design Impact

There is no design impact.

Workaround

This issue has no workaround.
Solution Status
This issue will be fixed in a future version of the Viterbi Compiler.

IP Functional Simulation Model Fails
The IP functional simulation model for your Verilog HDL design may fail.

Affected Configurations
This issue affects all Verilog HDL designs.

Design Impact
There is no design impact.

Workaround
Create a VHDL variation and use the VHDL IP functional simulation model.

Solution Status
This issue will be fixed in a future version of the Viterbi Compiler.

File Summary Does Not List All Generated Files
The file summary on the IP Toolbench Generate window does not always list all the generated files.

Affected Configurations
This issue affects all configurations.

Design Impact
There is no design impact.

Workaround
In the Parameterize window, when you finish parameterizing your variation, do not click Finish, just go to IP Toolbench and click Generate.

Solution Status
This issue will be fixed in a future version of the Viterbi Compiler.

Trellis Mode Fails
The trellis mode does not work correctly in the parallel continuous architecture.

Affected Configurations
This issue affects the parallel architecture, continuous optimization.

Design Impact
You cannot use the trellis mode.
Workaround
There is no workaround. Contact Altera, if you need this issue fixed.

Solution Status
This issue will be fixed in a future version of the Viterbi Compiler.
How to Contact Altera

For the most up-to-date information about Altera® products, see the following table.

<table>
<thead>
<tr>
<th>Contact (Note 1)</th>
<th>Contact Method</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technical support</td>
<td>Website</td>
<td><a href="http://www.altera.com/support">www.altera.com/support</a></td>
</tr>
<tr>
<td>Technical training</td>
<td>Website</td>
<td><a href="http://www.altera.com/training">www.altera.com/training</a></td>
</tr>
<tr>
<td></td>
<td>Email</td>
<td><a href="mailto:custrain@altera.com">custrain@altera.com</a></td>
</tr>
<tr>
<td>Altera literature services</td>
<td>Email</td>
<td><a href="mailto:literature@altera.com">literature@altera.com</a></td>
</tr>
<tr>
<td>Non-technical support (General)</td>
<td>Email</td>
<td><a href="mailto:nacomp@altera.com">nacomp@altera.com</a></td>
</tr>
<tr>
<td>(Software Licensing)</td>
<td>Email</td>
<td><a href="mailto:authorization@altera.com">authorization@altera.com</a></td>
</tr>
</tbody>
</table>

Note:
(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions that this document uses.

<table>
<thead>
<tr>
<th>Visual Cue</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bold Type with Initial Capital Letters</td>
<td>Indicates command names, dialog box titles, dialog box options, and other GUI labels. For example, Save As dialog box. For GUI elements, capitalization matches the GUI.</td>
</tr>
<tr>
<td>bold type</td>
<td>Indicates directory names, project names, disk drive names, file names, file name extensions, dialog box options, software utility names, and other GUI labels. For example, \qdesigns directory, d: drive, and chiptrip.gdf file.</td>
</tr>
<tr>
<td>Italic Type with Initial Capital Letters</td>
<td>Indicates document titles. For example, AN 519: Stratix IV Design Guidelines.</td>
</tr>
<tr>
<td>Italic type</td>
<td>Indicates variables. For example, n + 1. Variable names are enclosed in angle brackets (&lt; &gt;). For example, &lt;file name&gt; and &lt;project name&gt;.pof file.</td>
</tr>
<tr>
<td>Initial Capital Letters</td>
<td>Indicates keyboard keys and menu names. For example, Delete key and the Options menu.</td>
</tr>
<tr>
<td>“Subheading Title”</td>
<td>Quotation marks indicate references to sections within a document and titles of Quartus II Help topics. For example, “Typographic Conventions.”</td>
</tr>
<tr>
<td>Courier type</td>
<td>Indicates signal, port, register, bit, block, and primitive names. For example, data1, tdi, and input. Active-low signals are denoted by suffix n. For example, resetn. Indicates command line commands and anything that must be typed exactly as it appears. For example, c:\qdesigns\tutorial\chiptrip.gdf. Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword SUBDESIGN), and logic function names (for example, TRI).</td>
</tr>
<tr>
<td>Visual Cue</td>
<td>Meaning</td>
</tr>
<tr>
<td>-------------------------</td>
<td>-------------------------------------------------------------------------</td>
</tr>
<tr>
<td>1., 2., 3., and a., b., c., and so on.</td>
<td>Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.</td>
</tr>
<tr>
<td>■ ■ ■ ■</td>
<td>Bullets indicate a list of items when the sequence of the items is not important.</td>
</tr>
<tr>
<td>■ ■ ■ ■</td>
<td>The hand points to information that requires special attention.</td>
</tr>
<tr>
<td>CAUTION</td>
<td>A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.</td>
</tr>
<tr>
<td>WARNING</td>
<td>A warning calls attention to a condition or possible situation that can cause you injury.</td>
</tr>
<tr>
<td>▼ ▼ ▼ ▼</td>
<td>The angled arrow instructs you to press Enter.</td>
</tr>
<tr>
<td>▼ ▼ ▼ ▼</td>
<td>The feet direct you to more information about a particular topic.</td>
</tr>
</tbody>
</table>