



Intel FPGA IP

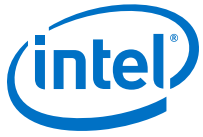
Release Notes

Updated for Intel® Quartus® Prime Design Suite: **18.1**



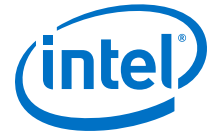
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1. About the Intel® FPGA IP Release Notes

These release notes include links to Intel FPGA IP cores, including the Intel FPGA IP Library and other IP cores.

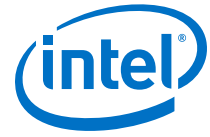
- [1G/10GbE and Backplane Ethernet 10GBASE-KR PHY Release Notes](#)
- [10-Gbps Ethernet \(10GbE\) MAC IP Core Release Notes](#)
- [1G/2.5G/10G Multi-rate Ethernet PHY Release Notes](#)
- [10GBASE-R PHY IP Core Release Notes](#)
- [25G Ethernet IP Core Release Notes](#)
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- [100G Interlaken IP Core Release Notes](#)
- [Advanced SEU Detection Intel FPGA IP Core Release Notes](#)
- [Arria V GZ Hard IP for PCI Express IP Core Release Notes](#)
- [Arria V Hard IP for PCI Express IP Core Release Notes](#)
- [Arria 10 1G/10GbE and 10GBASE-KR PHY IP Core Release Notes](#)
- [Intel Arria 10 External Memory Interface IP Core Release Notes](#)
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- [Intel Arria 10 and Intel Cyclone 10 Hard IP for PCI Express IP Core Release Notes](#)
- [Arria 10 Transceiver ATX PLL IP Core Release Notes](#)
- [Arria 10 Transceiver CMU PLL IP Core Release Notes](#)
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- [BCH IP Core Release Notes](#)
- [CIC IP Core Release Notes](#)
- [Clock Control Intel Stratix 10 FPGA IP Core Release Notes](#)
- [CPRI IP Core Release Notes](#)
- [Cyclone V Hard IP for PCI Express IP Core Release Notes](#)
- [DDR2 and DDR3 SDRAM Controller with UniPHY IP Core Release Notes](#)
- [Embedded Memory \(RAM: 1-PORT, RAM: 2-PORT, RAM: 4-PORT, ROM: 1-PORT, and ROM: 2-PORT IP Core Release Notes](#)
- [eSRAM IP Core Release Notes](#)
- [Intel FPGA DisplayPort IP Core Release Notes](#)

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- [FIFO IP Core Release Notes](#)
- [FIFO2 IP Core Release Notes](#)
- [FIR II IP Core Release Notes](#)
- [FFT IP Core Release Notes](#)
- [Intel FPGA HDMI IP Core Release Notes](#)
- [High-speed Reed-Solomon IP Core Release Notes](#)
- [Hybrid Memory Cube Controller IP Core Release Notes](#)
- [Intel® Stratix® 10 H-Tile Hard IP for Ethernet IP Core Release Notes](#)
- [Intel Stratix 10 Hard IP for PCI Express* IP Core Release Notes](#)
- [Intel Stratix 10 Low Latency 40-Gbps Ethernet IP Core Release Notes](#)
- [Low Latency 100G Ethernet Intel Stratix 10 FPGA IP Core Release Notes](#)
- [Intel Stratix 10 1G/2.5G/5G/10G Multi-rate Ethernet PHY IP Core Release Notes](#)
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- [RLDRAM II Controller with UniPHY and RLDRAM 3 PHY-Only IP Core Release Notes](#)



1. About the Intel® FPGA IP Release Notes

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- [SDI IP Core Release Notes](#)
- [Intel FPGA SDI II IP Core Release Notes](#)
- [Intel FPGA SDI Audio IP Cores Release Notes](#)
- [SerialLite II Release Notes](#)
- [SerialLite III Streaming IP Core Release Notes](#)
- [SmartVID Controller IP Core Release Notes](#)
- [Stratix V Hard IP for PCI Express IP Core Release Notes](#)
- [Triple Speed Ethernet IP Core Release Notes](#)
- [Turbo IP Core Release Notes](#)
- [Video and Image Processing Suite Release Notes](#)
- [Viterbi IP Core Release Notes](#)
- [V-Series Avalon-MM DMA for PCI Express IP Core Release Notes](#)
- [XAUI PHY Release Notes](#)
- [Other IP Cores Release Notes](#)
- [Other Transceiver IP Cores Product Release Notes](#)

Related Information

- [Introduction to Intel FPGA IP Cores](#)
- [Intel FPGA Software Installation and Licensing](#)

1.1. Errata

Errata are functional defects or errors, which may cause the product to deviate from published specifications. Documentation errata include errors, unclear descriptions, or omissions from current published specifications or product documents.

For full information on errata and the versions affected by errata, refer to the Knowledge Base on the Intel FPGA website.

Related Information

[Knowledge Base](#)