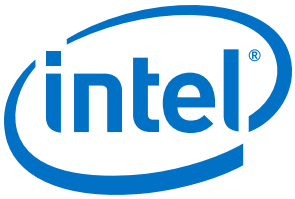

Intel FPGA IP

Release Notes

Updated for Intel® Quartus® Prime Design Suite: **18.0**

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Related Information

- Introduction to Intel FPGA IP Cores
- Intel FPGA Software Installation and Licensing

1.1. Errata

Errata are functional defects or errors, which may cause the product to deviate from published specifications. Documentation errata include errors, unclear descriptions, or omissions from current published specifications or product documents.

For full information on errata and the versions affected by errata, refer to the Knowledge Base on the Intel FPGA website.

Related Information

Knowledge Base