FIR Compiler

May 2007, Version 7.1 Release Notes

These release notes for the Altera® FIR Compiler, v7.1 contain the following information:

System Requirements

The FIR Compiler is part of the MegaCore® IP library which is distributed with the Quartus II software.

For system requirements and install instructions, refer to the *Quartus II Installation & Licensing for Windows* manual or the *Quartus II Installation & Licensing for UNIX and Linux* manual on the *Altera Literature website*.

New Features & Enhancements

The FIR Compiler implements a finite impulse response filter MegaCore® function.

The following list outlines new features and enhancements in this release:

- New symmetric interpolation reduces the number of multipliers required
- Preliminary support for Arria™ GX

Errata Fixed in This Release

The following errata were fixed in this release:

- Decimation half-band did not support logic cells
- Simulation result was incorrect using the multicycle mode
- Negative numbers were generated for unsigned input data type
- Missing `coef_ld` port for MCV architecture
- Output bit selection was incorrect when MegaCore was reopened

Known errata for the FIR Compiler are listed in a separate errata sheet.

For existing up-to-date errata, refer to the *FIR Compiler, v7.1 Errata Sheet* on the Errata Sheets page of the Altera literature website.

How to Contact Altera

Although every effort has been made to ensure that this version of the FIR Compiler Compiler works correctly, if any problems occur, please use the following contact information to communicate issues to the appropriate Altera representative.

Table 1. Contacting Altera

Information Type	Contact *Note (1)*
Technical support	www.altera.com/mysupport/
Product literature	www.altera.com
Altera literature services	literature@altera.com
FTP site	ftp.altera.com

Note to Table 1
(1) You can also contact your local Altera sales office or sales representative.

Revision History

Table 2 shows the revision history for the FIR Compiler.

Table 2. FIR Compiler Revision History

Version	Date	Revision
7.1	May 2007	• Added interpolation symmetry support. • Added Arria™ GX device support.
7.0	December 2006	Added Cyclone® III device support.
6.1	December 2006	• Added Stratix® III device support. • New Avalon® Streaming interfaces. • New half-band decimator filter support.
3.3.1	April 2006	Minor bug fixes.
3.3.0	October 2005	• Symmetric optimization to reduce the number of multipliers used in MCV decimating FIR filters. • Channel indicator for multichannel FIR filters. • Verilog testbench generator. • Preliminary support for Stratix II GX and HardCopy II devices.
3.1.0	June 2004	• Support for Cyclone® II device family. • DSP Builder ready (with version 2.2.0 or higher). • Taxonomy change - FIR Compiler now resides under DSP-Filters instead of Signal Processing-Filters. • Update to IP Toolbench 1.2.5.

Table 2. FIR Compiler Revision History

Version	Date	Revision
3.0.1		• Fixed bug in coefficient and data alignment for multi-channel multi-coefficient set structure. • Fixed bug in data initialize file zero.hex for multichannel MCV structure which only effect. • Support for ModelSim simulation.
3.0.0		• New Java based GUI with Multi-Platform support (Windows, Solaris, Linux). • Added Support for Stratix II Ternary Adders (with single rate distributed arithmetic filters). • Dramatic speed increases and/or area reductions in Stratix II architecture. • Serial FIR filters in Stratix II now achieve up to 350 MHz operation. • Parallel Distributed Arithmetic FIR filters can achieve 320 MHz operation. • Ternary adder structures combined with distributed arithmetic can reduce area by 30%-50% • Added Atlantic based flow control and updated clock enable based flow control circuitry. • Added Filter Design Assistant (more messages to indicate which configurations are supported and various error conditions). • Encrypted RTL Simulation is now replaced with IP Functional Simulation. • Updated OpenCore Plus hardware evaluation encryption. • Removed Visual IP Support. • Removed all DSP Builder support. • Removed support for older families (APEX, Mercury, ACEX, FLEX). • Updated report file - removed latency information. • Auto scaling information (actual scaling factor) was displayed in a disabled edit box in the older GUI. This information is no longer available.

101 Innovation Drive
San Jose, CA 95134
www.altera.com
Literature Services:
literature@altera.com

Copyright © 2007 Altera Corporation. All rights reserved. Altera, The Programmable Solutions Company, the stylized Altera logo, specific device designations, and all other words and logos that are identified as trademarks and/or service marks are, unless noted otherwise, the trademarks and service marks of Altera Corporation in the U.S. and other countries. All other product or service names are the property of their respective holders. Altera products are protected under numerous U.S. and foreign patents and pending applications, maskwork rights, and copyrights. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera Corporation. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.

I.S. EN ISO 9001