DSP Builder
Release Notes and Errata

101 Innovation Drive
San Jose, CA 95134
www.altera.com

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Chapter 1. Standard Blockset

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This chapter describes new features, revision history, known errata and documentation changes for the DSP Builder standard blockset.

Revision History

Table 1–1 lists the revision history for the DSP Builder standard blockset v9.0, v8.1, v8.0 SP1, and v8.0.

Table 1–1. DSP Builder Standard Blockset Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Revision</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.0 SP1</td>
<td>May 2009</td>
<td>■ Maintenance release.</td>
</tr>
<tr>
<td>9.0</td>
<td>March 2009</td>
<td>■ Support for Linux operating systems.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Support for Arria® II GX.</td>
</tr>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>■ Removed obsolete Simulation Accelerator block and deprecated support for the Video and Image Processing Suite.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Updated Hardware in the loop (HIL) block user interface.</td>
</tr>
<tr>
<td>8.0 SP1</td>
<td>July 2008</td>
<td>■ Maintenance release.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>■ New Display Pipeline Depth block.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Export HDL option added to Signal Compiler.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Integration with the Quartus® II state machine editor.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Added support for Stratix® IV devices.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Stratix III DSP block renamed as DSP block.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Added support for the Cyclone® III 3C120 and Stratix III 3SL150 DSP development boards.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Added support for MATLAB R2007b and R2008a (dropped R14 SP3).</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Added support for the Quartus II IP (.qip) file and design archiving.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Expanded platform support (Windows Vista 32-bit and 64-bit with 32-bit MATLAB). Several errata fixes and documentation updates.</td>
</tr>
</tbody>
</table>

Errata

Errata are functional defects or errors which may cause DSP Builder to deviate from published specifications. Table 1–2 shows the errata that affect the DSP Builder standard blockset v9.0, v8.1, v8.0 SP1, and v8.0.

For the latest errata information, refer to the DSP Builder Release Notes and Errata on the Altera literature website.
### DSP Block Naming Issue in Software Version 8.1

The **Stratix III DSP** block was renamed to **DSP** block in the v8.0 software because it also supports Stratix IV devices. A forwarding table in the library model ensured that any blocks named **Stratix III DSP** block upgraded from the previous release was recognized as a **DSP** block in the v8.0 software.

The name of the block incorrectly reverted to **Stratix III DSP** in the v8.1 software.

**Affected Configurations**

Designs upgraded from v8.0 that use the **DSP** block.

**Design Impact**

A **DSP** block in a design upgraded from v8.0 is not recognized in the v8.1 software.

**Workaround**

If you upgrade to v9.0, any blocks named **DSP** or **Stratix III DSP** are recognized as **DSP** blocks.

Alternatively, you can edit the `<install directory>\quartus\dsp_builder\bin\mdllibrary\allblocks_alteradspbuilder2.mdl` file in the v8.1 software and add the following reverse forwarding table string:

```plaintext
ForwardingTableString "||__slOldName__||allblocks_alteradspbuilder2/DSP Block||__slNewName__||allblocks_alteradspbuilder2/Stratix III DSP Block"
```

**Solution Status**

This issue is fixed in v9.0 of the DSP Builder advanced blockset.
Incorrect Pin Assignments Test2S60Board.mdl Design Example

The pin assignments for the PLL output clock resets are incorrect in the design example Test2S60Board.mdl.

Affected Configurations
Design example Test2S60Board.mdl.

Design Impact
Errors are issued reporting invalid pin assignments when you run the Quartus II Fitter from the Signal Compiler block.

Workaround
Perform the following steps to correct the pin assignments.

1. In MATLAB, navigate to the directory `<install directory>`\quartus\dsp_builder\DesignExamples\Demos\Board\StratixII_DSPBoard_2S60 and open the model Test2S60Board.mdl.
2. Double-click on the Quartus II assignments block to open the subsystem window.
3. Double-click on the Quartus II Pinout Assignments1 block to open the Block Parameters dialog box for PLL clock reset out. Change the pin location assignments to Pin_AD32, Pin_AB30, Pin_M30, Pin_N29. Click OK to apply and save the changes.
4. Save the model.
5. Use the normal procedures to compile and download the design to the board, and run SignalTap II Analysis on the design.

Solution Status
This issue is fixed in v9.0 SP1 of DSP Builder.

MATLAB Runs Out of Java Virtual Machine Heap Memory

For a very large design, MATLAB may have insufficient heap memory available for the Java virtual machine.

Affected Configurations
Very large designs containing many thousand blocks.

Design Impact
Compilation fails and MATLAB issues an error message of the form:

“OutOfMemoryError: Java heap space”

Workaround
Increase the heap space available to the Java virtual machine. For more information, refer to:

http://www.mathworks.com/support/solutions/data/1-18I2C.html
Solution Status
This issue will be documented in a future release of DSP Builder.

VCD Sink Block Does Not Generate HDL Files on Linux

The VCD Sink block does not generate HDL files on Linux systems.

Affected Configurations
Linux configurations.

Design Impact
No HDL is generated for the VCD Sink block.

Workaround
None.

Solution Status
This issue will be fixed in a future release of DSP Builder.

Errors Issued With Imported Quartus II Project

HDL Import blocks that import Quartus II projects may cause errors while executing the Signal Compiler or TestBench flows.

Affected Configurations
Models with HDL Import blocks that reference Quartus II projects with SEARCH_PATH assignments, rather than USER_LIBRARIES assignments.

Design Impact
Models containing HDL Import blocks that import Quartus II projects generated using Quartus II v8.0 may fail to generate hardware because the library settings are not recognized.

Workaround
Add a USER_LIBRARIES setting to the .qsf file for the Quartus II project to be imported. The assignment value should be the concatenation of all the project’s SEARCH_PATH assignment values, separated by semi-colons and enclosed within quotes. These required search path values may be in the top-level .qsf file, or in .qip files included in the project. Then recompile the HDL Import block.

Solution Status
This issue is fixed in v9.0 of DSP Builder.

Cannot Compare Simulink Against ModelSim When Using VIP Suite IP

Execution of the Compare against HDL or Generate HDL steps in the Testbench Generator dialog box issues an error for Video and Image Processing Suite MegaCore functions.
Affected Configurations
Designs using Video and Image Processing Suite MegaCore function blocks.

Design Impact
Testbench generation does not complete successfully, and automatic comparison of the Simulink simulation results against the results from ModelSim® is not possible.

Workaround
A MATLAB m-script is provided that give access to the testbench flow, with the flow output being sent to the MATLAB command window. The command required to use this script is:

```
alt_dspbuilder_compare_VIP_design_against_HDL(<model>, <performcompare>)
```

where:
- `<model>` is the name of the .mdl file for which the flow is to be run.
- `<performcompare>` is optional, setting it to 0 causes the final Compare Results step to be skipped. The default value of 1 causes the Compare Results step to be run.

After the script is run, you can use the features available in the Advanced tab of the Testbench Generator dialog box (excluding the Generate HDL step).

Solution Status
The Video and Image Processing Suite MegaCore functions are not supported in DSP Builder v9.0 or later.

MATLAB Hangs If You Press Enter in Signal Compiler Device Box
MATLAB hangs if you press the Enter or Return key in the Device box on the Signal Compiler dialog box.

Affected Configurations
All configurations.

Design Impact
None.

Workaround
Take care to avoid pressing the Enter or Return key after typing the device name.

Solution Status
This issue will be fixed in a future release of DSP Builder.

Reset Signal Inverted if _n Appended to Signal Name
The reset signal is inverted if _n is appended to the signal name specified in the Clock or Clock_Derived block.
Affected Configurations
Designs which include a Clock or Clock_Derived block.

Design Impact
The inverted reset signal is propagated through the design.

Workaround
Do not append _n to the reset signal specified in a Clock or Clock_Derived block unless you explicitly want the signal to be inverted. Note that you can append _N (uppercase) without inverting the reset signal.

Solution Status
This issue will be fixed in a future release of DSP Builder.

Error Generating HDL for State Machine Editor Block
Generating HDL from some State Machine Editor block configurations can cause an access violation to occur.

Affected Configurations
Designs using the State Machine Editor block which include the == operator in conditional expressions.

Design Impact
HDL generation does not complete successfully, and the block configuration is not integrated into the DSP Builder design.

Workaround
Do not use the == operator in conditional expressions. However, you can use the ~ operator. For example, use in1 and ~in1 rather than in1==1 and in1==0.

Solution Status
This issue is fixed in v8.1 of the Quartus II software.

Error During Fast Functional Simulation of FFT MegaCore Function
Designs implementing a fast Fourier transform (FFT) using the FFT MegaCore function block cannot be simulated using the fast functional simulation technology.

Affected Configurations
Any v8.0 design containing v7.1, v7.2, or v8.0 FFT MegaCore function blocks.

Design Impact
A run-time error is issued if you attempt to perform a bit-accurate (faster) simulation.

Workaround
Select cycle-accurate mode before performing simulation.
Solution Status
Fast functional simulation is obsolete in v8.1.

Additional Project Assignments Required for User Libraries
Additional project assignments may be required when using the Export HDL flow with user libraries.

Affected Configurations
Configurations that include MegaCore function, HDL Import, or State Machine Editor blocks.

Design Impact
Compilation fails in the Quartus II software with an error of the form:

```
Error: Node instance <block_name> instantiates undefined entity <entity_name>
```

Workaround
Add the following to the Quartus II project:
- The .qip file corresponding to the entity named in the error message. (This file is located in the import subdirectory corresponding to the library model.)
- In some cases you may also need to add any libraries which are referenced by HDL Import block(s) in the library model.

Solution Status
This issue will be fixed in a future release of DSP Builder.

Dual-Clock FIFO Simulation Does Not Match ModelSim
The Dual-Clock FIFO simulation in Simulink is functionally equivalent to hardware, but not cycle-accurate.

Affected Configurations
Most configurations are affected.

Design Impact
The delay between the write-side adding data and the read-side seeing it, and between the read-side clearing space in the FIFO and the write-side seeing it, does not match hardware.

Workaround
Do not rely on these timing characteristics for correctness of a design.

Solution Status
This issue will be fixed in a future release of DSP Builder.
This chapter describes new features, revision history, known errata and documentation changes for the DSP Builder advanced blockset.

Revision History

Table 2–1 lists the revision history for the DSP Builder advanced blockset.

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Revision</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.0 SP1</td>
<td>May 2009</td>
<td>Maintenance release. Support for Linux operating systems. Support for Arria® II GX. Updated SOPC Builder support and procedures for instantiating a design. Support for running all the automatic testbenches in a design. Improved documentation for the NCO block including multichannel design examples with support for multiple banks.</td>
</tr>
<tr>
<td>9.0</td>
<td>March 2009</td>
<td>Support for Linux operating systems.</td>
</tr>
<tr>
<td>8.1</td>
<td>November 2008</td>
<td>New W-CDMA example designs. Latency display option on ModelIP blocks. DONT_CARE option on Dual Memory block. Diagrammatic channelization format display for ModelIP blocks. Quartus II IP (.qip) file support. Latency constraints can be applied using the SynthesisInfo block.</td>
</tr>
<tr>
<td>8.0 SP1</td>
<td>July 2008</td>
<td>Maintenance release.</td>
</tr>
<tr>
<td>8.0</td>
<td>May 2008</td>
<td>First release of the DSP Builder Advanced Blockset.</td>
</tr>
</tbody>
</table>

Errata

Errata are functional defects or errors which may cause DSP Builder to deviate from published specifications. Table 2–2 shows the errata that affect the DSP Builder advanced blockset v9.0, v8.1, v8.0 SP1, or V8.0.

For the latest errata information, refer to the DSP Builder Release Notes and Errata on the Altera literature website.

<table>
<thead>
<tr>
<th>Added or Updated</th>
<th>Issue</th>
<th>Affected Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>15May09</td>
<td>Multiplier Optimizations Can Cause Signal Width Mismatch in Synthesis</td>
<td>✔ 0 0 0</td>
</tr>
<tr>
<td></td>
<td>HIL Simulation of Combined Blockset Design Outputs All Zeros</td>
<td>Fixed</td>
</tr>
</tbody>
</table>
Multiplier Optimizations Can Cause Signal Width Mismatch in Synthesis

Multiplier optimizations can lead to signal bit width mismatches and VHDL errors in synthesis.

Affected Configurations

Primitive subsystems where a multiplier feeds directly into an output port.

Design Impact

When you compile for synthesis in the Quartus II software, an error is issued of the form:

```
Error: Actual width (34) of port "q1" on instance "<model>:<submod>" is not compatible with the formal port width (30) declared by the instantiated entity
```

This is because the output signal is smaller than expected because of a multiplier optimization not being propagated on to a fixed width entity (usually an subsystem boundary or other fixed-width block).

Workaround

Use a Convert block from the ModelPrim library to explicitly set the required signal format on the output of the multiplier.

Solution Status

This issue will be fixed in a future release of the DSP Builder advanced blockset.
HIL Simulation of Combined Blockset Design Outputs All Zeros

A Hardware in the loop (HIL) design containing blocks from both the standard and advanced blocksets sometimes outputs all zeros when simulated. This problem occurs when the reset type is set to Low in the Signals block.

The DSP Design Flow Guide currently states that an embedded advanced blockset design should have the same reset type as the standard blockset design in which it is embedded. This is incorrect; the advanced blockset design must always have an active high reset.

Affected Configurations
HIL designs derived from a model created using the advanced blockset.

Design Impact
The HIL simulation output remains zero.

Workaround
Change the reset type specified in the Signals block to High by performing the following steps:

1. In the original combined blockset design, set the Reset name to aclr and Reset active to High in the Signals block.
2. Delete all the generated files from the rtl directory specified as the Hardware destination directory in the Control block.
3. Delete all the files from the DSPBuilder_<top level>_import directory.
4. Delete all the files from <top level>_dspbuilder directory.
5. Run Simulink simulation (to generate HDL for the advanced blockset).
6. Compile the design in the Signal Compiler block (generate HDL and create a Quartus II project for the whole design).
7. Open the HIL model and run the normal HIL flow.

The reset level specified in the Clock block is not relevant.

Solution Status
This issue is fixed in the latest version of the DSP Design Flow Guide.

Latency Not Balanced for ModelBus blocks Outside Primitive Subsystem

If you are using ModelBus blocks outside of a primitive subsystem with Scheduled synthesis style, it is likely that the latencies on the address, write enable and data paths created for these blocks may not be balanced in v9.0.

Affected Configurations
Configurations using ModelBus blocks outside of a primitive subsystem with Scheduled synthesis style. ModelBus blocks inside a scheduled subsystem are not affected.
Design Impact
The latencies on the address, write enable and data paths created for ModelBus blocks outside of a primitive subsystem may not be balanced.

Workaround
To ensure the data path is registered in line with the address and write enable for such unscheduled blocks, define the following workspace variable before performing simulation and HDL generation (for example in the model InitFnc callbacks):

DSPBA_Features.useScheduledDataBus = false;

The default v9.0 behavior can be restored by setting this variable to true.

Solution Status
This issue will be fixed in a future release of the DSP Builder advanced blockset.

Hardware Tcl Files Do Not Have Correct Port Names for Vector Ports
If any input ports to the synthesizable system have vector inputs (for example if they feed into a FIR filter with more than one channel and a sample rate matching the clock rate), the <hardware>_hw.tcl file generated for SOPC Builder has misnamed ports.

Affected Configurations
Any synthesizable system that has vector input ports.

Design Impact
The port names in the <hardware>_hw.tcl file are not vectorized. For example, it might only list an input a and an output q, although the VHDL actually contains input port names a0, a1,... and output port names q0, q1,...

Workaround
Manually correct the Tcl file using the generated VHDL as a reference. For example:

add_interface_port exp a export Input 17

becomes:

add_interface_port exp a0 export Input 17
add_interface_port exp a1 export Input 17
add_interface_port exp a2 export Input 17
...

Solution Status
This issue will be fixed in a future release of the DSP Builder advanced blockset.

Bus and System Clocks Must Match When Using Bus Stimulus Block
Testbench simulation results are incorrect when using the Bus Stimulus block if the bus clock frequency is different from the frequency of the system clock.
Affected Configurations
Any design that uses the Bus Stimulus block.

Design Impact
The testbench simulation results are incorrect.

Workaround
The bus clock frequency must be the same as the frequency of the system clock. Turn on Separate Bus Clock and Bus Clock Synchronous with System Clock in the Signal block for your model.

Solution Status
This issue will be fixed in a future release of the DSP Builder advanced blockset.

Primitive Automatic Testbench Flow Incorrect with Many Integer Bits
The primitive automatic testbench flow may be incorrect when using fractional representations with many integer bits.

Affected Configurations
Designs that require a large number of integer bits.

Design Impact
Unexpected simulation mismatches are reported.

Workaround
Reduce the number of integer bits required by your model.

Solution Status
This issue is fixed in v9.0 of the DSP Builder advanced blockset.

Limit of 50 Subsystem Ports Anywhere in a Design
All blocks that become functional units are restricted to a maximum of 50 ports.

Affected Configurations
Any block or subsystem that has more than 50 ports.

Design Impact
An assert m_inCount <= m_maxInCount which crashes MATLAB.

Workaround
Avoid creating a subsystem or block with more than 50 ports.

Solution Status
This issue is fixed in v9.0 of the DSP Builder advanced blockset.
Saturation Limitation When using the Scale Block

When you increase the number of fractional bits used for a signal, the MSB may be truncated.

**Affected Configurations**
Configurations using the Scale block.

**Design Impact**
The MSB may be truncated.

**Workaround**
Use a Convert block inside the primitive subsystem.

**Solution Status**
This issue will be fixed in a future release of the DSP Builder advanced blockset.

Very High Hard Multiplier Threshold Does Not Force the Use of Logic

Setting a very high Hard Multiplier Threshold should avoid using any DSP blocks.

**Affected Configurations**
All configurations.

**Design Impact**
Unwanted use of DSP blocks.

**Workaround**
None.

**Solution Status**
This issue will be fixed in a future release of the DSP Builder advanced blockset.

No Forward Flow Control in Primitive Subsystems

'Bursty' input data is not supported for primitive subsystems, that is designs where the valid signal toggles high and low repeatedly.

**Affected Configurations**
Any primitive subsystem.

**Design Impact**
The simulation results are incorrect.

**Workaround**
Avoid using bursts of data.
Solution Status
This issue will be fixed in a future release of the DSP Builder advanced blockset.

Limitations of the ModelSim Testbench Flow

The \texttt{Run ModelSim} block can be used to simulate a model in ModelSim. This flow attempts to make a ModelSim testbench by synthesizing all the block (including any Simulink blocks in the top-level). However only a limited number of Simulink blocks are synthesizable and an empty subsystem is created for the unsupported blocks.

Affected Configurations
Any model with unsynthesizable Simulink blocks in the top-level.

Design Impact
The testbench cannot be simulated.

Workaround
Use only the supported blocks in the testbench for your design or write your own HDL for the empty subsystems. (A full list of synthesizable blocks is given in the description of the \texttt{Run ModelSim} block.) Alternatively, you can use the automatic testbench flow to simulate each subsystem in your design separately.

Solution Status
This issue will be fixed in a future release of the DSP Builder advanced blockset.

HIL Error When Using Async Clear as Async Load

A HIL design does not work when the reset is used both as Async Clear and Async Load, and is tied to the JTAG reset.

Affected Configurations
Advanced blockset designs that integrate a \texttt{HIL} block from the standard blockset.

Design Impact
The design stays in reset and all outputs are zero.

Workaround
None.

Solution Status
This issue is fixed in v8.1 of the DSP Builder advanced blockset.

Results for ModelPrim Blocks May be Incorrect for Fractional Types

The ModelPrim blocks give an incorrect result if you specify a fractional output bit width that is different to the width that would be selected if you choose the \texttt{Inherit via Internal Rule} option.
**Affected Configurations**
Configurations of ModelPrim blocks where the **Specify via dialog** option has been used.

**Design Impact**
The simulation value does not match the Simulink multiplier.

**Workaround**
When using fractional types, ensure that the output bit width is specified to be the sum of the input bit widths. Alternatively, add a `Convert` block if you need any other fractional output bit width.

**Solution Status**
This behavior is described in v8.1 of the *DSP Builder Advanced Blockset User Guide*.

**Cannot Import a Combined Blockset Design into SOPC Builder**
You cannot import a design that combines blocks from the standard and advanced blocksets into SOPC Builder.

**Affected Configurations**
Configurations which combine blocks from the standard and advanced blocksets.

**Design Impact**
If you attempt to import a combined blockset design into SOPC Builder, warning are issued stating that there are multiple clocks with the same name and the component is not added to the system.

**Workaround**
There is no workaround.

**Solution Status**
This issue will be fixed in a future release of the DSP Builder advanced blockset.

**Incorrect Simulation Results if Word Length Greater Than 64 bits**
The simulation results are incorrect for ModelIP blocks if the word length is greater than 64 bits.

**Affected Configurations**
Configurations which include ModelIP blocks are affected. However, ModelPrim blocks do support word lengths greater than 64 bits.

**Design Impact**
The simulation results are incorrect.
Workaround
Restrict the word length used by ModelIP blocks to 64 bits.

Solution Status
This issue will be fixed in a future release of the DSP Builder advanced blockset.

Compilation Error if Unused Channel Out Port is Terminated
Quartus II compilation fails if an unused channel or valid signal from a Channel Out block is connected to a Simulink Terminator block inside a primitive subsystem.

Affected Configurations
Primitive subsystems with unused channel or valid output signals.

Design Impact
Incorrect HDL is generated and errors are issued when you attempt to compile the design in the Quartus II software.

Workaround
Leave the unused signals unconnected or terminate them outside the subsystem.

Solution Status
This issue will be fixed in a future release of the DSP Builder advanced blockset.
Update Status

The following table displays the update status for these release notes.

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes Made</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 June 2009</td>
<td>4.3</td>
<td>Added an errata in the standard blockset chapter.</td>
</tr>
<tr>
<td>May 2009</td>
<td>4.2</td>
<td>Updated for software version 9.0 SP1.</td>
</tr>
<tr>
<td>April 2009</td>
<td>4.1</td>
<td>Added and updated errata in the advanced blockset chapter.</td>
</tr>
<tr>
<td>March 2009</td>
<td>4.0</td>
<td>Updated for software version 9.0.</td>
</tr>
<tr>
<td>November 2008</td>
<td>3.0</td>
<td>Updated for software version 8.1.</td>
</tr>
<tr>
<td>July 2008</td>
<td>2.1</td>
<td>Added one errata to standard blockset chapter.</td>
</tr>
<tr>
<td>May 2008</td>
<td>2.0</td>
<td>Added separate chapter for the advanced blockset and moved install information to new DSP Design Flow User Guide.</td>
</tr>
<tr>
<td>December 2007</td>
<td>1.2</td>
<td>Fixed two errata.</td>
</tr>
<tr>
<td>15 October 2007</td>
<td>1.1</td>
<td>Added two errata.</td>
</tr>
<tr>
<td>October 2007</td>
<td>1.0</td>
<td>New combined release notes and errata document for the current and previous two releases.</td>
</tr>
</tbody>
</table>

How to Contact Altera

For the most up-to-date information about Altera® products, refer to the following table.

<table>
<thead>
<tr>
<th>Contact 1</th>
<th>Contact Method</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technical support</td>
<td>Website</td>
<td><a href="http://www.altera.com/support">www.altera.com/support</a></td>
</tr>
<tr>
<td>Technical training</td>
<td>Website</td>
<td><a href="http://www.altera.com/training">www.altera.com/training</a></td>
</tr>
<tr>
<td></td>
<td>Email</td>
<td><a href="mailto:custrain@altera.com">custrain@altera.com</a></td>
</tr>
<tr>
<td>Product literature</td>
<td>Website</td>
<td><a href="http://www.altera.com/literature">www.altera.com/literature</a></td>
</tr>
<tr>
<td>Non-technical support (General) (Software Licensing)</td>
<td>Email</td>
<td><a href="mailto:nacomp@altera.com">nacomp@altera.com</a></td>
</tr>
<tr>
<td></td>
<td>Email</td>
<td><a href="mailto:authorization@altera.com">authorization@altera.com</a></td>
</tr>
</tbody>
</table>

Note to table:
(1) You can also contact your local Altera sales office or sales representative.
## Typographic Conventions

This document uses the typographic conventions shown in the following table.

<table>
<thead>
<tr>
<th>Visual Cue</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Bold Type with Initial Capital Letters</strong></td>
<td>Indicates command names, dialog box titles, dialog box options, and other GUI labels. For example, <strong>Save As</strong> dialog box.</td>
</tr>
<tr>
<td><strong>bold type</strong></td>
<td>Indicates directory names, project names, disk drive names, file names, file name extensions, and software utility names. For example, \qdesigns\ directory, <strong>d:</strong> drive, and <strong>chiptrip.gdf</strong> file.</td>
</tr>
<tr>
<td><strong>Italic Type with Initial Capital Letters</strong></td>
<td>Indicates document titles. For example: <strong>AN 519: Stratix IV Design Guidelines.</strong></td>
</tr>
<tr>
<td><strong>Italic type</strong></td>
<td>Indicates variables. For example, <strong>n + 1.</strong></td>
</tr>
<tr>
<td>Variable names are enclosed in angle brackets (&lt;&gt;). For example, <code>&lt;file name&gt;</code> and <code>&lt;project name&gt;.pof</code> file.</td>
<td></td>
</tr>
<tr>
<td><strong>Initial Capital Letters</strong></td>
<td>Indicates keyboard keys and menu names. For example, <strong>Delete key</strong> and the <strong>Options menu.</strong></td>
</tr>
<tr>
<td><strong>“Subheading Title”</strong></td>
<td>Quotation marks indicate references to sections within a document and titles of Quartus II Help topics. For example, “<strong>Typographic Conventions.”</strong></td>
</tr>
<tr>
<td><strong>Courier type</strong></td>
<td>Indicates signal, port, register, bit, block, and primitive names. For example, <strong>data1, tdi, and input.</strong> Active-low signals are denoted by suffix <strong>n.</strong> Example: <strong>resetn.</strong></td>
</tr>
<tr>
<td>Indicates command line commands and anything that must be typed exactly as it appears. For example, <strong>c:\qdesigns\tutorial\chiptrip.gdf.</strong> Also indicates sections of an actual file, such as a <strong>Report File</strong>, references to parts of files (for example, the AHDL keyword <strong>SUBDESIGN</strong>), and logic function names (for example, <strong>TRI</strong>).</td>
<td></td>
</tr>
<tr>
<td><strong>1., 2., 3., and a., b., c., and so on.</strong></td>
<td>Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.</td>
</tr>
<tr>
<td><strong>■ ■</strong></td>
<td>Bullets indicate a list of items when the sequence of the items is not important.</td>
</tr>
<tr>
<td><strong>•</strong></td>
<td>The hand points to information that requires special attention.</td>
</tr>
<tr>
<td><strong>⚠️</strong></td>
<td>A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.</td>
</tr>
<tr>
<td><strong>⚠️</strong></td>
<td>A warning calls attention to a condition or possible situation that can cause you injury.</td>
</tr>
<tr>
<td><strong>→</strong></td>
<td>The angled arrow instructs you to press the enter key.</td>
</tr>
<tr>
<td><strong>→→</strong></td>
<td>The feet direct you to more information about a particular topic.</td>
</tr>
</tbody>
</table>