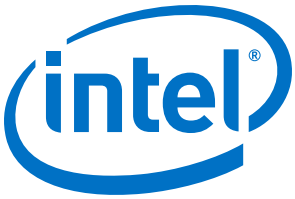

DSP Builder for Intel® FPGAs Release Notes

Updated for Intel® Quartus® Prime Design Suite: **19.1**

Subscribe
Send Feedback

RN-DSP004 | 2019.07.25
Latest document on the web: PDF | HTML

Contents

1. DSP Builder for Intel® FPGAs Release Notes

Related Information

- Knowledge Base
- Software Installation and Licensing
- System requirements

1.1. Errata

Errata are functional defects or errors, which may cause the product to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.
For full information on errata and the versions affected by errata, refer to the Knowledge Base page of the Intel® website.

Related Information

Knowledge Base

1.2. DSP Builder for Intel FPGAs Advanced Blockset Revision History

Table 1. Revision History

Version	Date	Description
19.1	2019.04.01	• Added support for two new floating-point types `float16_m7` (bfloat) and `float19_m10`. • Added dependent latency feature. • Added FIFO buffer fill-level reporting.
18.1	2018.09.17	• Added HDL import. • Added C++ software models.
18.0	2018.05.08	• Added support for automatic reset minimization of DSP Builder designs. Reset minimization determines the minimal set of registers in a design that require reset, while retaining the design's correct functionality. Reducing the number of registers that DSP Builder resets may give improved quality of results i.e. reduced area and increased Fmax. • Added support for bit fields to the **SharedMem** block. These fields provide analogous functionality to the existing bit field support in the **RegField** and **RegOut** blocks. • Added beta support for HDL import, which incorporates VHDL or Verilog HDL synthesizable designs into a DSP Builder design. You can then cosimulate the imported design with DSP Builder Simulink components. HDL import includes a minimal user interface, but requires some manual setup. To use this feature, you require a license for the MathWorks HDL Verifier tool.
17.1	2017.11.06	• Added super-sample NCO design example. • Added support for Intel Cyclone® 10 and Intel Stratix® 10 devices. • Removed instances of **Signals** block. • Deleted WYSIWYG option on **SynthesisInfo** block.

continued...

Version	Date	Description
17.0	2017.05.05	• Rebranded as Intel • Deprecated **Signals** block • Added Gaussian and Random Number Generator design examples • Added variable-size supersampled FFT design example • Added **HybridVFFT** block • Added **GeneralVTwiddle** and **GeneralMultVTwiddle** blocks
16.1	2016.11.10	• Added 4-channel 2-antenna DUC and DDC for LTE reference design • Added BFU_simple block • Created Standard and Pro editions. Pro supports Arria 10 devices; Standard supports all other families. • Deprecated the **Signals** block • Added functionality for setting the Avalon-MM interface settings in the DSP Builder menu
16.0	2016.05.02	• Reorganized libraries • Improved folding results on MAX 10 devices • Added new design examples: — Gaussian Random Number Generator — DUC_4C4T4R and DDC_4C4T4R LTE digital-up and down-conversion • Added new FFT pruning strategy: `prune_to_widths()`
15.1	2015.11.11	• Deprecated **Run Quartus II** and **Run Modelsim** blocks • Added clock crossing support • Added reconfigurable FIR filters • Improved bus interfaces: — Improved error checking and reporting — Improved simulation accuracy — Improved bus slave logic implementation — Improved clock crossing • Changed some Avalon-MM interfaces • Added new blocks: — **Capture Values** — **Fanout** — **Pause** — **Vectorfanout** • Added IIR: full-rate fixed-point and IIR: full-rate floating-point demos • Added transmit and receive modem reference design
15.0	May 2015	• Added support for SystemVerilog output • Added external memories library • Added **External Memory** block • Added new **Allow write on both ports** parameter to **DualMem** block • Changed parameters on **AvalonMMSlaveSettings** block
14.1	December 2014	• Added support for Arria 10 hard-floating-point blocks • Added BusStimulus and BusStimulusFileReader blocks to memory-mapped registers design example. • Added AvalonMMSlaveSettings block and **DSP Builder > Avalon Interfaces > Avalon-MM slave** menu option • Removed bus parameters from Control and Signal blocks

continued...

Version	Date	Description
		• Removed the following design examples: — Color Space Converter (Resource Sharing Folding) — Interpolating FIR Filter with Updating Coefficients — Primitive FIR Filter (Resource Sharing Folding) — Single-Stage IIR Filter (Resource Sharing Folding) — Three-stage IIR Filter (Resource Sharing Folding) • Added system-in-the-loop support • Added new blocks: — Floating-point classifier — Floating-point multiply accumulate — Added hypotenuse function to math block • Added design examples: — Color space converter — Complex FIR — CORDIC from Primitive Blocks — Crest factor reduction — Folding FIR — Variable Integer Rate Decimation Filter — Vector sort - sequential and iterative • Added reference designs: — Crest factor reduction — Direct RF with Synthesizable Testbench — Dynamic Decimation Filter — Reconfigurable Decimation Filter — Variable Integer Rate Decimation Filter • Removed resource sharing folder • Updated ALU folder
14.0	June 2014	• Added support for MAX 10 FPGAs. • Removed support for Cyclone III and Stratix III devices • Improved **DSP Builder Run ModelSim** option, which now allows you to run ModelSim for the top-level design or individual submodules • Changed the generation of HDL into the device level directory (under the specified target RTL directory) rather than in a hierarchy of directories • Added read signal on bus interface • Added clear port on the FIFO

continued...

Version	Date	Description
		• Deprecated 13 FFT blocks • Added new design examples: — Avalon-ST Interface (Input and Output FIFO Buffer) with Backpressure — Avalon-ST Interface (Output FIFO Buffer) with Backpressure — Fixed-point maths functions — Fractional square root using CORDIC — Normalizer — Parallel FFT — Parallel Floating-Point FFT — Square root using CORDIC — Switchable FFT/iFFT — Variable-Size Fixed-Point FFT — Variable-Size Fixed-Point FFT without BitReverseCoreC Block — Variable-Size Fixed-Point iFFT — Variable-Size Fixed-Point iFFT without BitReverseCoreC Block — Variable-Size Floating-Point FFT — Variable-Size Floating-Point FFT without BitReverseCoreC Block — Variable-Size Floating-Point iFFT — Variable-Size Floating-Point iFFT without BitReverseCoreC Block • Added new blocks: — Anchored Delay — Enabled Delay Line — Enabled Feedback Delay — FFT2P, FFT4P, FFT8P, FFT16P, FFT32P, and FFT64P — FFT2X, FFT4X, FFT8X, FFT16X, FFT32X, and FFT64X — FFT2, FFT4, VFFT2, and VFFT4 — General Multitwiddle and General Twiddle (GeneralMultiTwiddle, GeneralTwiddle) — Hybrid FFT (Hybrid_FFT) — Parallel Pipelined FFT (PFFT_Pipe) — Ready
13.1	November 2013	• Removed support for the following devices: — Arria GX — Cyclone II — HardCopy II, HardCopy III, and HardCopy IV — Stratix, Stratix II, Stratix GX, and Stratix II GX • Improved ALU folding flow • Added new functions to Math block.

continued...

Version	Date	Description
		• Added Simulink fi block option to Const, DualMem, and LUT blocks • Added new design examples: — Variable-precision real-time FFT — Interpolating FIR Filter with updating coefficients — Time-delay beamformer • Added new blocks: — Anchored Delay — Polynomial — TwiddleAngle — TwiddleROM and TwiddleROMF — VariableBitReverse — VFFT
13.0	May 2013	• Updated device block with new Device Selector menu. • Added new ModelPrim blocks: — Const Mult — Divide — MinMax — Negate — Scalar Product • Added nine new FFT blocks • Added ten new FFT demonstrations
12.1	November 2012	• Added ALU folding feature • Added enhanced precision floating-point options • Added the following new ModelPrim blocks: — AddSub — AddSubFused — CmpCtrl — Math — Maximum and Minimum — MinMaxCtrl — Round — Trig • Added the following new FFT blocks: — Edge Detect (EdgeDetect) — Pulse Divider (PulseDivider) — Pulse Multiplier (PulseMultiplier) — Bit-Reverse FFT with Natural Output (FFT_BR_Natural) • Added the following new FIR design examples: — Super-sample decimating FIR filter — Super-sample fractional FIR filter • Added the position, speed, and current control for AC motors (with ALU folding) design example

Related Information

- DSP Builder Handbook Volume 3: DSP Builder Advanced Blockset
- Errata for DSP Builder advanced blockset in the Knowledge Base