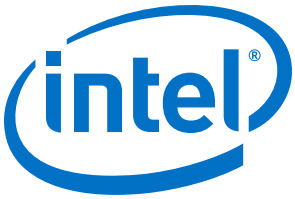

Intel® FPGA SDK for OpenCL™ Pro Edition

Version 20.2 Release Notes

Updated for Intel® Quartus® Prime Design Suite: **20.2**

Subscribe
Send Feedback

RN-OCL004 | 2020.06.22
Latest document on the web: PDF | HTML

Contents

1. Intel® FPGA SDK for OpenCL™ Pro Edition Version 20.2 Release Notes

The *Intel® FPGA SDK for OpenCL™ Pro Edition Release Notes* provides late-breaking information about the Intel FPGA Software Development Kit (SDK) for OpenCL[1][2] Pro Edition and the Intel FPGA Runtime Environment (RTE) for OpenCL Pro Edition Version 20.2.

1.1. New Features and Enhancements

The Intel FPGA SDK for OpenCL Pro Edition and the Intel FPGA RTE for OpenCL Pro Edition include the following new features:

- Removed board support packages from the Intel FPGA SDK for OpenCL installer.
- Added support for the `stall_enable` cluster control attribute.

1.2. Operating System Support

Information about OS support for the Intel FPGA SDK for OpenCL is available on the Operating System Support page of the Intel FPGA website.

Related Information

Operating System Support

1.3. Changes to Software Behavior

Items listed in the following table represent cases in which the behaviors of the current release of the Intel FPGA SDK for OpenCL and the Intel FPGA RTE for OpenCL differ from the previous version.

Description	Required Actions
The board support packages (BSP) are no longer part of the Intel FPGA SDK for OpenCL installation.	Download the BSPs from the Download Center for FPGAs.

Related Information

OpenCL 2.0 Headers

(1) OpenCL and the OpenCL logo are trademarks of Apple Inc. used by permission of the Khronos Group™.

(2) The Intel FPGA SDK for OpenCL is based on a published Khronos Specification, and has passed the Khronos Conformance Testing Process. Current conformance status can be found at www.khronos.org/conformance.

1.4. Known Issues and Workarounds

This section provides information about known issues that affect the Intel FPGA SDK for OpenCL and the Intel FPGA RTE for OpenCL Version 20.2.

Description	Workaround

The following crash can occur when using the Intel FPGA Emulation Platform on Windows system:
`Stack dump:`
`0. Running pass 'CallGraph Pass Manager' on module 'main'`
This crash is caused by the use of high number of function calls in the design (more than 10,000).
	Reduce the number of function calls used in the design. Alternatively, you can use the Intel FPGA Emulation Platform for OpenCL on a Linux system.

When compiling an OpenCL kernel containing calls to library functions containing HLS tasks, incremental compile may trigger recompilation for unaffected kernels.	No known workaround. However, this is not a functional bug. It may result in a more conservative incremental compile.
Using HLS streams in HLS System-Of-Tasks (SOT) in OpenCL library does not work with hyper-optimized-handshaking protocol when targeting Intel Stratix® 10 devices, and results in the following error: `internal compiler error: node internal validation failed`	Turn off the protocol by setting `-hyper-optimized-handshaking=off`.
The emulator runtime emits an assertion error if a kernel is enqueued 16,000 times.	Do not enqueue a kernel more than 16,000 times.
OpenCL kernels with names longer than 61 characters might fail in the Intel Quartus® Prime Pro Edition compiler with an error similar to the following error: `Error (16045): Instance "...|<long_kernel_name>_cra_slave_inst" instantiates undefined entity "<long_kernel_name>_function_cra_slave" File: <filename> Line: <linenumber>`	Reduce the size of the OpenCL kernel name.
OpenCL kernel pipes cannot be passed as arguments in some cases. The symptom is the runtime receives a `CL_INVALID_BUFFER_SIZE (-61)` error when you enqueue your kernel.	Modify your design to use channels instead of pipes.
When alternatively using sub-buffers and their parent buffers, changes written to one might not be reflected in the other.	Unmapping and mapping a buffer forces the sub-buffers and their parent buffers to be synced. Unmapping and mapping a buffer between buffer uses should prevent this issue.
In the OpenCL runtime, making more than one OpenCL context in a multithreaded environment might cause a segmentation fault.	—

This section provides information about known issues that affect the current release of the Intel FPGA SDK for OpenCL Custom Platform Toolkit and Reference Platforms. These issues might also affect Custom Platforms you create for use with the Intel FPGA SDK for OpenCL.

Description	Workaround
Terminating the host process in BSPs (all versions of `a10_ref`, `s10_ref`, and `s10mx_ref`) can cause the machine to crash or freeze when OpenCL is running. BSPs require the host user process to stay active during certain	Use the Intel Acceleration Stack.

continued...

Description	Workaround
operations, such as DMA transfers. If you terminate the host process while such operations are active, the operating system crashes. If your BSP is affected by this issue, you should avoid performing the following: • Pressing Ctrl + C keys combination • Using assertions • Calling the `exit()` function • Performing any abnormal termination in the host programs, such as null dereference, bus error, uncaught exception, and so on.	
Race conditions can occur between enqueue and dequeue buffer operations and host pipe operations. These conditions can results in incorrect data being read or written.	Manually make sure that no enqueue or dequeue buffer operations occur in parallel with host pipe API calls. A way to ensure that buffer operations do not occur in parallel with host pipe API calls is to do buffer operations as blocking calls before the first host pipe operation and after you are certain that the last host pipe operation has been completed (for example, all the data is read back).
For Windows, when the host application queries the number of devices, calls to `clGetDeviceIDs` return 128 devices regardless of the actual number of devices present. *Note:* You can find the actual available devices at the beginning of the device list returned by `clGetDeviceIDs`. This issue affects the Intel Arria® 10 GX FPGA Development Kit Reference Platform and the Intel Stratix 10 GX FPGA Development Kit Reference Platform.	Perform one of the following workarounds: • Rewrite the host application to limit the query for `clGetDeviceIDs` to the actual number of devices. • Rewrite the host application to use `clGetDeviceInfo` to query which devices are available. Calling `clGetDeviceInfo` with the `CL_DEVICE_AVAILABLE` flag correctly reports that extraneous devices are unavailable. • Rewrite the host application to only call `clCreateContext` with the actual number of devices. Calling `clCreateContext` with extraneous devices will fail with the error `CL_DEVICE_NOT_AVAILABLE`. • Set the environment variable *`CL_OVERRIDE_NUM_DEVICES_INTELFPGA`* to the correct number of devices. Doing so fixes the erroneous behavior of `clGetDeviceIDs`.

Latest Known Intel FPGA SDK for OpenCL Software Issues

For additional known issue information for the current Intel FPGA SDK for OpenCL version and for previous versions, refer to the Knowledge Base web page.

Related Information

Knowledge Base

1.5. Software Issues Resolved

The following issues were corrected or otherwise resolved in the Intel FPGA SDK for OpenCL and the Intel FPGA RTE for OpenCL Version 20.2.

Table 1. Issues Resolved in the Intel FPGA SDK for OpenCL and the Intel FPGA RTE for OpenCL Version 20.2

Customer Service Request Numbers	
00501613	00480296

1.6. Software Patches Included in this Release

No software patches included in this release.

1.7. Intel FPGA SDK for OpenCL Pro Edition Release Notes Archives

If the table does not list a software version, the user guide for the previous software version applies.

Intel Quartus Prime Version	User Guide
20.1	Intel FPGA SDK for OpenCL Pro Edition Version 20.1 Release Notes
19.4	Intel FPGA SDK for OpenCL Pro Edition Version 19.4 Release Notes
19.3	Intel FPGA SDK for OpenCL Pro Edition Version 19.3 Release Notes
19.2	Intel FPGA SDK for OpenCL Pro Edition Version 19.2 Release Notes
19.1	Intel FPGA SDK for OpenCL Pro Edition Version 19.1 Release Notes
18.1	Intel FPGA SDK for OpenCL Pro Edition Version 18.1 Release Notes
18.0	Intel FPGA SDK for OpenCL Pro Edition Release Notes
17.1	Intel FPGA SDK for OpenCL Release Notes
17.0	Intel FPGA SDK for OpenCL Release Notes
16.1	Intel FPGA SDK for OpenCL Release Notes
16.0	Altera SDK for OpenCL Version 16.0 Release Notes
15.1	Altera SDK for OpenCL Version 15.1 Release Notes
15.0	Altera SDK for OpenCL Version 15.0 Release Notes

1.8. Document Revision History of the Intel FPGA SDK for OpenCL Pro Edition Release Notes

Document Version	Intel Quartus Prime Version	Changes
2020.06.22	20.2	Initial release.