F-Tile Interlaken Intel® FPGA IP Release Notes

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1. F-Tile Interlaken Intel® FPGA IP Release Notes

The Intel® FPGA IP version (X.Y.Z) number can change with each Intel Quartus® Prime software version. A change in:

- X indicates a major revision of the IP. If you update the Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Related Information

- Introduction to Intel FPGA IP Cores
- F-Tile Interlaken Intel FPGA IP User Guide
- F-Tile Interlaken Intel FPGA IP Design Example User Guide

1.1. F-Tile Interlaken Intel FPGA IP v3.0.0

Table 1. v3.0.0 2021.10.04

Intel Quartus Prime Pro Edition Version	Description	Impact
21.3	Added support for the following combinations of number of lanes and data rates: • 4 x 6.25G • 4 x 12.5G • 4 x 25.78125G • 10 x 12.5G • 10 x 25.78125G • 12 x 10.3125G • 12 x 12.5G	—
	Added support for Siemens EDA* Questa* simulator.	—

Related Information

Intel Quartus Prime Pro Edition: Version 21.3 Software and Device Support Release Notes

1.2. F-Tile Interlaken Intel FPGA IP v2.0.0

Table 2. v2.0.0 2021.06.21

Intel Quartus Prime Pro Edition Version	Description	Impact
21.2	Initial release.	—

Related Information

Intel Quartus Prime Pro Edition: Version 21.2 Software and Device Support Release Notes