

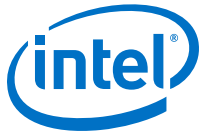


XAUI PHY Release Notes

RN-1136
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Contents

1 XAUI PHY Release Notes.....	3
1.1 XAUI PHY IP Core v17.0 Revision History.....	3
1.2 XAUI PHY IP Core v14.1 Revision History.....	3
1.3 XAUI PHY IP Core v14.0 Arria 10 Revision History.....	4
1.4 XAUI PHY IP Core v14.0 Revision History.....	5
1.5 XAUI PHY IP Core v13.1 Revision History.....	5



1 XAUI PHY Release Notes

If a release note is not available for a specific IP core version, the IP core has no changes in that version. Information on the latest update releases is in the *Intel Quartus Prime Design Suite Update Release Notes*.

Related Links

[Intel Quartus Prime Design Suite Update Release Notes](#)

1.1 XAUI PHY IP Core v17.0 Revision History

Table 1. v17.0 May 2017

Description	Impact
<p>When opening a Quartus Prime Pro Edition software version 16.0 or 16.1 XAUI PHY IP core design in Quartus Prime Pro Edition software version 17.0, you may encounter the following issues:</p> <ul style="list-style-type: none"> The IP upgrade required error message appears When the Upgrade IP Components window opens, it may display the incorrect IP component name in the IP Component column with an incorrect URL to the release notes Incorrect descriptions may appear in the Description column 	<p>This issue only occurs when you generate the XAUI IP core from the Quartus Prime Pro Edition software. The Quartus Prime Standard Edition software is not affected by this issue.</p> <p>Despite these display issues, the Perform Automatic Update function correctly performs the necessary update.</p>

Related Links

- [Altera Transceiver PHY IP Core User Guide](#)
- [Arria 10 Transceiver PHY User Guide](#)
- [Errata for XAUI PHY IP Core in the Knowledge Base](#)
- [Introduction to Altera IP Cores](#)

1.2 XAUI PHY IP Core v14.1 Revision History

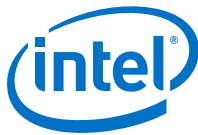
Table 2. v14.1 December 2014

Description	Impact
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade, but does not clarify the reason.	You must ensure that you specify a device for your v13.1 Arria 10 Edition or v14.0 Arria 10 Edition IP core variation and regenerate it in the Quartus II software v14.1.
Added the Enable phase compensation FIFO parameter.	-
<i>continued...</i>	

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Description	Impact
Added the <code>xgmii_rx_inclk</code> port, which is available when Enable phase compensation FIFO is enabled.	-
Added the <code>pll_cal_busy_i</code> port, which connects to the <code>pll_cal_busy</code> output port of the external PLL.	-
Added a new Arria 10 SDC constraint requirement. Refer to the "XAUI PHY TimeQuest SDC Constraint" section of the <i>Arria 10 Transceiver PHY User Guide</i> .	-

Related Links

- [Altera Transceiver PHY IP Core User Guide](#)
- [Arria 10 Transceiver PHY User Guide](#)
- [Errata for XAUI PHY IP Core in the Knowledge Base](#)
- [Introduction to Altera IP Cores](#)

1.3 XAUI PHY IP Core v14.0 Arria 10 Revision History

Table 3. v14.0 Arria 10 Edition August 2014

Description	Impact
Added support for Arria 10 devices. To use the XAUI PHY IP core for Arria 10 devices, you must instantiate an external transmit PLL. You can only use the ATX PLL IP core with the XAUI PHY IP core for Arria 10 devices.	-
Added Enable dynamic reconfiguration parameter.	-
Removed the following parameters: <ul style="list-style-type: none"> • PLL type. • External PMA control and configuration. 	-
Added new port to enable connectivity with an external transmit PLL and with the dynamic reconfiguration interface. Refer to the <i>Arria 10 Transceiver PHY User Guide</i> parameter and port descriptions.	-
The XAUI PHY IP core does not support NCSIM simulator. You will see an error message during elaboration.	-
The XAUI PHY IP core does not support VHDL. You will get a compilation error when you simulate the XAUI PHY IP core generated in VHDL. You must generate this IP core in Verilog.	-

Related Links

- [Altera Transceiver PHY IP Core User Guide](#)
- [Arria 10 Transceiver PHY User Guide](#)
- [Errata for XAUI PHY IP Core in the Knowledge Base](#)
- [Introduction to Altera IP Cores](#)



1.4 XAUI PHY IP Core v14.0 Revision History

Table 4. v14.0 July 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .	-

Related Links

- [Altera Transceiver PHY IP Core User Guide](#)
- [Errata for XAUI PHY IP Core in the Knowledge Base](#)
- [Introduction to Altera IP Cores](#)

1.5 XAUI PHY IP Core v13.1 Revision History

Table 5. v13.1 November 2013

Description	Impact
Verified in the Quartus II software v13.1	-

Related Links

- [Altera Transceiver PHY IP Core User Guide](#)
- [Errata for XAUI PHY IP Core in the Knowledge Base](#)
- [Introduction to Altera IP Cores](#)