1 Viterbi IP Core Release Notes

1.1 Viterbi IP Core v17.1
1.2 Viterbi IP Core v16.0
1.3 Viterbi IP Core v15.0
1.4 Viterbi IP Core v14.1
1 Viterbi IP Core Release Notes

If a release note is not available for a specific IP core version, the IP core has no changes in that version. Information on the latest update releases is in the Intel Quartus Prime Design Suite Update Release Notes.

Related Links
Intel Quartus Prime Design Suite Update Release Notes

1.1 Viterbi IP Core v17.1

Table 1. v17.1 November 2017

<table>
<thead>
<tr>
<th>Description</th>
<th>Impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>Added support for Intel® Cyclone® 10 devices</td>
<td>-</td>
</tr>
<tr>
<td>Added support for Intel Stratix® 10 devices</td>
<td>-</td>
</tr>
</tbody>
</table>

Related Links
• Viterbi IP Core User Guide
• Introduction to Altera IP Cores
• Errata for Viterbi IP core in the Knowledge Base

1.2 Viterbi IP Core v16.0

Table 2. v16.0 May 2016

<table>
<thead>
<tr>
<th>Description</th>
<th>Impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Removed tb_type signal from hybrid designs</td>
<td>-</td>
</tr>
<tr>
<td>• Removed tb_length from parallel designs with optimization Block</td>
<td>-</td>
</tr>
</tbody>
</table>

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1.3 Viterbi IP Core v15.0

Table 3. v15.0 May 2015

<table>
<thead>
<tr>
<th>Description</th>
<th>Impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>Verified in the Quartus II software v15.0.</td>
<td>-</td>
</tr>
</tbody>
</table>

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1.4 Viterbi IP Core v14.1

Table 4. v14.1 December 2014

<table>
<thead>
<tr>
<th>Description</th>
<th>Impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>Added support for multiple codesets for Arria 10 devices.</td>
<td>-</td>
</tr>
<tr>
<td>Added final support for Arria 10 and MAX 10 devices</td>
<td>-</td>
</tr>
</tbody>
</table>

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- Errata for Viterbi IP core in the Knowledge Base