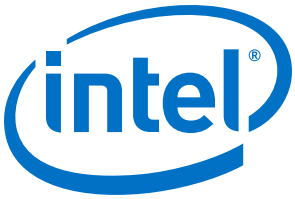

Video and Image Processing Suite Release Notes

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Contents

1. Video and Image Processing Suite Release Notes

If a release note is not available for a specific IP core version, the IP core has no changes in that version. Information on the latest update releases is in the *Intel Quartus Prime Design Suite Update Release Notes*.

Attention: The following IP cores are no longer supported in versions 17.0 and later:

- 2D FIR Filter
- Alpha Blending Mixer
- Chroma Resampler
- Color Space Converter
- Color Plane Sequencer
- Control Synchronizer
- Deinterlacer
- Frame Buffer
- Frame Reader
- Gamma Corrector
- Interlacer
- Switch

Intel recommends that you use the upgraded versions of these IP cores.

Related Information

Intel Quartus Prime Design Suite Update Release Notes

1.1. Video and Image Processing Suite v18.1

Table 1. v18.1 September 2018

Description	Impact
Added new registers for the Deinterlacer II Intel FPGA IP. • Added new run-time control and status registers to improve deinterlacing quality for mid-range motion-adaptive configurations. • Added new registers to allow run-time switching between “bob”, ”weave” and “motion adaptive” modes.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Added new GUI parameters for the Mixer II Intel FPGA IP. • **Synchronize background to layer 0** • **InputN alpha channel** • **Reduced control register readback** • **Add extra register stages to data pipeline**	
Added new test pattern options for the Test Pattern II Intel FPGA IP.	

Related Information

- Introduction to Intel FPGA IP Cores
- Video and Image Processing Suite User Guide
- Errata for the Video and Image Processing Suite in the Knowledge Base

1.2. Video and Image Processing Suite v18.0

Table 2. v18.0 May 2018

Description	Impact
Support for 8 pixels in parallel are now available for the following IP cores: • 2D FIR Filter II • Avalon-ST Video Stream Cleaner • Chroma Resampler II • Clipper II • Clocked Video Input II • Clocked Video Output II • Color Space Converter II • Deinterlacer II • Frame Buffer II • Gamma Corrector II • Configurable Guard Bands • Interlacer II • Mixer II • Scaler II • Switch II • Test Pattern Generator II	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Clocked Video Output II IP core now supports Genlock.	
Added new GUI parameters for the Clocked Video Output II IP core: • **Generate Synchronization outputs** • **Accept Synchronization inputs** • **Set vco_clk_divider increment to pixels in parallel**	
Added Genlock signals for the Clocked Video Output II IP core: • `vid_vcoclk_div` • `vid_sof` • `vid_sof_locked` • `sof` • `sof_locked`	

Related Information

- Introduction to Intel FPGA IP Cores
- Video and Image Processing Suite User Guide
- Errata for the Video and Image Processing Suite in the Knowledge Base

1.3. Video and Image Processing Suite v17.1

Table 3. v17.1 November 2017

Description	Impact
Renamed Qsys to Platform Designer as per Intel rebranding.	–
All Video and Image Processing IP cores that support 4:2:2 feature require even frame widths when using 4:2:2 data; odd frame widths create unpredictable results or distorted images.	–
Added new parameters for Frame Buffer II IP core: • **Delay length (frames)** • **Drop/repeat user packets**	These changes are optional. If you do not upgrade your IP core, it does not have these new features.

Related Information

- Introduction to Intel FPGA IP Cores
- Video and Image Processing Suite User Guide
- Errata for the Video and Image Processing Suite in the Knowledge Base

1.4. Video and Image Processing Suite v17.0

Table 4. v17.0 May 2017

Description	Impact
Added a new IP core: Configurable Guard Bands IP core. This IP core supports pixels in parallel and run-time control.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Added device support for Intel Cyclone 10 LP and Cyclone 10 GX devices.	
Removed the following IP cores. These IP cores are no longer supported in Quartus Prime versions 17.0 and later. • 2D FIR Filter • Alpha Blending Mixer • Chroma Resampler • Color Space Converter • Color Plane Sequencer • Deinterlacer • Frame Buffer • Frame Reader • Gamma Corrector • Interlacer • Switch	
Added new parameters for the Chroma Resampler II IP core: • **Enable vertical luma adaptive resampling** • **Vertical chroma siting** • **Variable 3 color interface** • **Enable 4:2:0 input** • **Enable 4:2:0 output**	
Removed these parameters for the Deinterlacer II IP core:	

continued...

Description	Impact
• **How user packets are handled: Pass all user packets through to the output** (packets will always pass through) • **Enable embedded chroma resamplers**	
Changed `Cadence Detect On` register to `Cadence Detect and advanced tuning registers On` register for the Deinterlacer II IP core. This updated register enables the cadence detection feature and (if configured) the video over film feature together with all the motion and cadence/VOF tuning registers.	
Removed edge sharpening feature for the Scaler II IP core.	

Related Information

- Introduction to Intel FPGA IP Cores
- Video and Image Processing Suite User Guide
- Errata for the Video and Image Processing Suite in the Knowledge Base

1.5. Video and Image Processing Suite v16.1

Table 5. v16.1 October 2016

Description	Impact
Added the following new IP cores for 16.1 release: • 2D FIR Filter II • Chroma Resampler II • Color Plane Sequencer II • Gamma Corrector II • Interlacer II All these IP cores support pixels in parallel and run-time control.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Removed the Broadcast Deinterlacer IP core and merged the features into the Deinterlacer II IP core. If you were using the Broadcast Deinterlacer IP core versions 15.1 or 16.0, Qsys will automatically upgrade your design to the Deinterlacer II version 16.1 with the same configuration.	
Mixer II IP core • Updated alpha stream information for Mixer II IP core. • When you enable alpha stream, the LSB is in Alpha value and the control packets are composed of all symbols including Alpha.	
Clocked Video Interface IP core • Added new parameters for Clocked Video Input II IP core: — **Enable matching data packet to control by clipping**: Turning on this parameter clips the input video frame to match the resolution sent in control packet. — **Enable matching data packet to control by padding**: Turning on this parameter pads the incoming frame if it is smaller and/or shorter than the resolution specified in the control packet. — **Overflow handling**: Turning on this parameter ends the current frame (with dummy pixel data) based on the resolution specified in the control packet if overflow happens. • Added new signals Clocked Video Input II IP core: `Clipping` and `Padding`. • Updated information about the `Status` register Clocked Video Input II IP core to include bits to support clipping and padding features. • Added new parameter for Clocked Video Output II IP core: — **Low latency mode**: Setting this parameter to 1 enables the IP core to start timing for a new frame immediately.	

Related Information

- Introduction to Intel FPGA IP Cores
- Video and Image Processing Suite User Guide
- Errata for the Video and Image Processing Suite in the Knowledge Base

1.6. Video and Image Processing Suite v16.0

Table 6. v16.0 May 2016

Description	Impact
Avalon-ST Video Stream Cleaner IP core • Added a new IP core. The Avalon-ST Video Stream Cleaner IP Core removes and repairs non-ideal sequences and error cases present in the incoming data stream to produce a compliant output stream.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Frame Buffer II IP core • Added new Frame Buffer II IP core parameters: — **Enable use of fixed inter-buffer offset** — **Inter-buffer offset** — **Module is Frame Reader only** — **Module is Frame Writer only**	
Mixer II IP core • Added new or updated the following Mixer II IP core parameters: — **Number of inputs** — **Alpha Blending Enable** — **Layer Position Enable** — **Register Avalon-ST ready signals** — **Uniform values** — **Number of pixels transmitted in 1 clock cycle** — **Alpha Input Stream Enable** — **4:2:2 support** — **How user packets are handled** • Removed these Mixer II IP core parameters: — **Number of color planes** — **Run-time control** — **Output format**	
Clocked Video Interface IP core	

continued...

Description	Impact
• Added new or updated these Clocked Video Input II IP core signals: — `dout_empty` — `vid_locked` (updated) — `vid_datavalid` (updated) — `vid_color_encoding` — `vid_bit_width` — `vid_total_sample_count` — `vid_total_line_count` • Added a new register, `Color Pattern`, for the Clocked Video Input II IP core. • Removed the **Accept synchronization outputs** parameter and the related signals from the Clocked Video Output II IP core. — `vcoclk_div` — `sof` — `sof_locked` — `vid_sof` — `vid_sof_locked`	
Switch II IP core • Added a new register: `Din Consume Mode Enable`.	

Related Information

- Introduction to Intel FPGA IP Cores
- Video and Image Processing Suite User Guide
- Errata for the Video and Image Processing Suite in the Knowledge Base

1.7. Video and Image Processing Suite v15.1

Table 7. v15.1 November 2015

Description	Impact
Removed Clipper and Test Pattern Generator IP cores. Use Clipper II and Test Pattern Generators II IP cores instead.	If you are using the obsoleted IP cores, you will not get any support from Altera.
Supports Quartus Prime Standard edition only.	–

Related Information

- Introduction to Altera IP Cores
- Video and Image Processing Suite User Guide
- Errata for the Video and Image Processing Suite in the Knowledge Base

1.8. Video and Image Processing Suite v15.0

Table 8. v15.0 May 2015

Description	Impact
Updated the `Input (0-3) Enable` registers for the Mixer II IP core. The 1-bit registers are changed to 2-bit registers: • Set to bit 0 of the registers to display input 0. • Set to bit 1 of the registers to enable consume mode.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Updated the parameter settings for the Mixer II IP core. • Added a new parameter **Pattern** which enables you to select the pattern for the background layer. • Removed **Color planes transmitted in parallel** . This feature is now default and internally handled through the hardware TCL file.	
Updated the parameter settings for the Frame Buffer II IP core. • Added support for the following parameters (these were not supported in the previous version): **Maximum ancillary packets per frame**, **Interlace support**, **Locked rate support**, **Run-time writer control**, and**Run-time reader control** • Removed **Ready latency** and **Delay length (frames)**. These features are fixed to 1 and internally handled through the hardware TCL file.	
Updated the parameter settings for the Avalon-ST Video Monitor IP core. • Added new parameters: **Color planes transmitted in parallel** and **Pixels in parallel**. • Removed **Number of color planes in sequence**. You can specify whether to transmit the planes in parallel or in series using the **Color planes transmitted in parallel** parameter.	

Related Information

- Introduction to Altera IP Cores
- Video and Image Processing Suite User Guide
- Errata for the Video and Image Processing Suite in the Knowledge Base

1.9. Video and Image Processing Suite v14.1

Table 9. v14.1 December 2014

Description	Impact
Updated the parameters for Clocked Video Input II and Clocked Video Output II IP cores. • Edited the function of the **Use control port** parameter. The control ports will now only appear when you turn on this parameter. • Removed the **Generate Display Port output** parameter.	-

Related Information

- Introduction to Altera IP Cores
- Video and Image Processing Suite User Guide
- Errata for the Video and Image Processing Suite in the Knowledge Base

1.10. Video and Image Processing Suite v14.0 Arria 10 Edition

Table 10. v14.0 Arria 10 Edition August 2014

Description	Impact
Added support for Arria 10 devices only in the following IP cores: • Avalon-ST Video Monitor • Broadcast Deinterlacer • Clipper II • Clocked Video Input II • Clocked Video Output II • Color Space Converter II • Deinterlacer II • Frame Buffer II • Mixer II • Scaler II • Switch II • Test Pattern Generator II	-

Related Information

- Introduction to Altera IP Cores
- Video and Image Processing Suite User Guide
- Errata for the Video and Image Processing Suite in the Knowledge Base