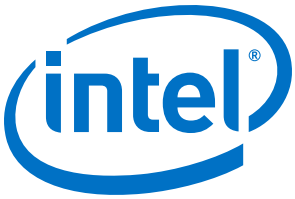

Triple-Speed Ethernet Intel® FPGA IP Release Notes

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1. Triple-Speed Ethernet Intel® FPGA IP Release Notes

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the *Intel® Quartus® Prime Design Suite Update Release Notes*.

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

The IP versioning scheme (X.Y.Z) number changes from one software version to another. A change in:

- X indicates a major revision of the IP. If you update your Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Related Information

- Intel Quartus Prime Design Suite Update Release Notes
- Triple-Speed Ethernet Intel FPGA IP User Guide Archives
- Errata for the Triple-Speed Ethernet Intel FPGA IP in the Knowledge Base

1.1. Triple-Speed Ethernet Intel FPGA IP v19.4.0

Table 1. v19.4.0 2019.12.16

Intel Quartus Prime	Description	Impact
19.4	Added support for the Intel Agilex™ device family.	—

1.2. Triple-Speed Ethernet Intel FPGA IP v19.2.0

Table 2. v19.2.0 2019.07.01

Intel Quartus Prime	Description	Impact
19.2	Added support for two new core variants for Intel Stratix® 10 E-tile devices: • 10/100/1000-Mbps Ethernet MAC with 1000BASE-X/SGMII 2XTBI PCS • 1000BASE-X/SGMII 2XTBI PCS	—

1.3. Triple-Speed Ethernet Intel FPGA IP v19.1

Table 3. v19.1 April 2019

Description	Impact
Renamed the **Enable Intel FPGA Debug Master Endpoint** parameter to **Enable Native PHY Debug Master Endpoint (NPDME)** as per Intel rebranding in the Intel Quartus Prime Pro Edition software. The Intel Quartus Prime Standard Edition software still uses **Enable Intel FPGA Debug Master Endpoint**.	—

1.4. Triple-Speed Ethernet Intel FPGA IP v18.0

Table 4. v18.0 May 2018

Description	Impact
Renamed Triple-Speed Ethernet IP core to Triple-Speed Ethernet Intel FPGA IP as per Intel rebranding.	—

Related Information

- Intel FPGA Triple Speed Ethernet IP User Guide
- Errata for Intel FPGA Triple Speed Ethernet IP core in the Knowledge Base

1.5. Intel FPGA Triple Speed Ethernet IP Core v17.1

Table 5. v17.1 November 2017

Description	Impact
Added support for the Intel Stratix 10, Intel Cyclone® 10 GX, and Intel Cyclone 10 LP device families.	These devices are only available in Intel Quartus Prime Pro Edition software version 17.1 onwards.
In versions 17.0.2 and earlier of the Triple-Speed Ethernet IP core, the Triple-Speed Ethernet IP variant with LVDS I/O for PMA implementation in Intel Arria® 10 devices may experience performance risk. This issue is fixed in the Intel Quartus Prime software version 17.1.	To upgrade designs from previous versions of the Intel Quartus Prime software to version 17.1, you must regenerate the Triple-Speed Ethernet IP core and recompile the design in the Intel Quartus Prime software version 17.1. Refer to the KDB page for more information.
The number of ports supported for Triple-Speed Ethernet design with LVDS I/O targeting Intel Stratix 10, Intel Arria 10, and Intel Cyclone 10 GX is 8 per instance. You must not promote the reference clock to global clock manually. Assign the number of ports supported and its reference clock to the same I/O bank as inter-bank clock sharing is not allowed.	—
RGMII interface is not supported in Intel Stratix 10, Intel Arria 10, and Intel Cyclone 10 GX devices.	—

Related Information

- Intel FPGA Triple Speed Ethernet IP Core User Guide
- Errata for Intel FPGA Triple Speed Ethernet IP core in the Knowledge Base

- KDB Link: Performance Risk Running Triple Speed Ethernet LVDS in Arria 10 Devices

1.6. Triple Speed Ethernet IP Core v15.1

Table 6. v15.1 November 2015

Description	Impact
Updated the ToD Clock module: • Added a new parameter—**PERIOD_CLOCK_FREQUENCY**.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Updated the ToD Synchronizer module: • Added a new parameter—**SAMPLE SIZE**. • Changed the parameter value of **SYNC_MODE** to "Between 0 to 15". • Changed the frequency range to 390.625 MHz.	

Related Information

- Triple Speed Ethernet IP Core User Guide
- Errata for Triple Speed Ethernet IP core in the Knowledge Base

1.7. Triple Speed Ethernet IP Core v15.0

Table 7. v15.0 May 2015

Description	Impact
You may observe hold time violation in designs targeting the Stratix V, Arria V, Cyclone V, and Arria 10 (10AS066ES) devices in this release.	Refer to the following errata for more information and the workaround: Hold Time Violation in Triple Speed Ethernet IP Core.

Related Information

- Introduction to Altera IP Cores
- Triple Speed Ethernet MegaCore Function User Guide
- Errata for Triple Speed Ethernet IP core in the Knowledge Base

1.8. Triple Speed Ethernet IP Core v14.0 Arria 10 Edition

Table 8. v14.0 Arria 10 Edition August 2014

Description	Impact
Verified in the Quartus II software v14.0 Arria 10 Edition. (Added support for Arria 10 devices).	If you upgrade your IP core to the Quartus II software v14.0 Arria 10 Edition , all of the changes require that you regenerate the IP core manually and reconnect it in your design.

Related Information

- Introduction to Altera IP Cores
- Triple Speed Ethernet MegaCore Function User Guide

- Errata for Triple Speed Ethernet IP core in the Knowledge Base

1.9. Triple Speed Ethernet IP Core v14.0

Table 9. v14.0 June 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-
Added ECC support for M20K blocks.	Optional changes. If you do not upgrade your IP core, it does not have these new features:
Added 1588v2 support for LVDS variant.	

Related Information

- Introduction to Altera IP Cores
- Triple Speed Ethernet MegaCore Function User Guide
- Errata for Triple Speed Ethernet IP core in the Knowledge Base

1.10. Triple Speed Ethernet IP Core v13.1 Arria 10 Edition

Table 10. v13.1 Arria 10 Edition December 2014

Description	impact
Added support for Arria 10 devices.	-

Related Information

- Introduction to Altera IP Cores
- Triple Speed Ethernet MegaCore Function User Guide
- Errata for Triple Speed Ethernet IP core in the Knowledge Base

1.11. Triple Speed Ethernet IP Core v13.1

Table 11. v13.1 November 2013

Description	Impact
Removed support for the following devices: • Arria GX • Cyclone II • HardCopy II, HardCopy III, and HardCopy IV • Stratix II and Stratix II GX	-
Added 1588v2 support for Arria V, Arria V SoC, Cyclone V, Cyclone V SoC and Stratix V devices.	-
Added 1588v2 support for MAC-only variants	-
Added ATX and CMU Tx PLL options for variations that include the PCS block targeting Arria V GZ and Stratix V devices.	-
Added SyncE support by separating Tx PLL and Rx PLL reference clock.	-
The period in nanosecond for csr registers: `tx_period`, `rx_period`, `Period`, and `AdjustPeriod`, was changed from bit 16 to 19 to bit 16 to 24.	-

Related Information

- Introduction to Altera IP Cores
- Triple Speed Ethernet MegaCore Function User Guide
- Errata for Triple Speed Ethernet IP core in the Knowledge Base

1.12. Triple-Speed Ethernet Intel FPGA IP User Guide Archives

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

If an IP core version is not listed, the user guide for the previous IP core version applies.

IP Core Version	User Guide
19.3.0	Triple-Speed Ethernet Intel FPGA IP User Guide
19.2.0	Triple-Speed Ethernet Intel FPGA IP User Guide
17.1	Triple-Speed Ethernet Intel FPGA IP User Guide
16.0	Triple-Speed Ethernet MegaCore Function User Guide
15.1	Triple-Speed Ethernet MegaCore Function User Guide
15.0	Triple-Speed Ethernet MegaCore Function User Guide