Stratix 10 SoC Virtual Platform Release Notes

These release notes cover versions 1.0 through 1.3 of the Intel® Stratix® 10 SoC Virtual Platform.

Related Links
Stratix 10 SoC Virtual Platform User Guide
For more information about the Stratix 10 SoC Virtual Platform, refer to this document.

Stratix 10 SoC Virtual Platform Version 1.3 Release Notes

This section describes any enhancements, known issues and advisories for the 1.3 version of the Stratix 10 SoC Virtual Platform.

Enhancements to the Stratix 10 SoC Virtual Platform Version 1.3

The following enhancements are included in the 1.3 version of the Stratix 10 SoC Virtual Platform:
- Improved processor modeling for use with hypervisor
- Support for proper reset handling

The following changes are included in the Linux version for the 1.3 version of the Stratix 10 SoC Virtual Platform:
- Kernel upgraded from 4.3 to 4.5
- Watchdog support

Known Issues in the Stratix 10 SoC Virtual Platform Version 1.3

Table 1. Known Issues

<table>
<thead>
<tr>
<th>Issue</th>
<th>Workaround</th>
</tr>
</thead>
<tbody>
<tr>
<td>Because Stratix 10 SoC Virtual platform is not a real-time platform, modeled real-time processes, such as wall clock timers, drift under sufficient execution load.</td>
<td>None</td>
</tr>
<tr>
<td>Intermittently, The hypervisor guest O/S console does not appear.</td>
<td>Enable only one CPU and leave the remaining three CPUs in reset. To implement this configuration, edit the parameters.txt file as shown below:</td>
</tr>
<tr>
<td></td>
<td>Startix10_top.rst_mux.use_rstmgr = 0</td>
</tr>
<tr>
<td></td>
<td>Startix10_top.rst_mux.ss_n_reset_1 = 0</td>
</tr>
<tr>
<td></td>
<td>Startix10_top.rst_mux.ss_n_reset_2 = 0</td>
</tr>
<tr>
<td></td>
<td>Startix10_top.rst_mux.ss_n_reset_3 = 0</td>
</tr>
</tbody>
</table>

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Advisory for the Stratix 10 SoC Virtual Platform Version 1.3

For large application compilations, use a chroot, Docker or a similar cross-compile environment and move the resultant files to the platform with secure copy (SCP).
Stratix 10 SoC Virtual Platform Version 1.2 Release Notes

This section describes any enhancements and notifications for the 1.2 version of the Stratix 10 SoC Virtual Platform.

Enhancements to the Stratix 10 SoC Virtual Platform Version 1.2

The following functional models are tested and verified in the 1.2 version of the Stratix 10 SoC Virtual Platform:

- On-chip RAM (OCRAM)

The following feature has been added to the 1.2 version of the Stratix 10 SoC Virtual Platform:

- Hypervisor support

Notifications for the Stratix 10 SoC Virtual Platform Version 1.2

- A patch to the Linux 4.6 kernel is not compatible with the Cortex®-A53 MPCore™ model used in the 1.2 version of the Stratix 10 SoC Virtual Platform. The preferred Linux kernel to use with this release is 4.5.

- In this release, instructions for how to create an SD card image for the Stratix 10 SoC Virtual Platform are not included in the user guide. For directions on how to create an SD card image for this release, please contact your local field sales representative.
Stratix 10 SoC Virtual Platform Version 1.1 Release Notes

This section describes any enhancements and known issues found in the 1.1 version of the Stratix 10 SoC Virtual Platform.

Enhancements to the Stratix 10 SoC Virtual Platform Version 1.1

The following functional models are available and have been tested in the 1.1 version of the Stratix 10 SoC Virtual Platform:

- SD/MMC
- Clock Manager
- Reset Manager
- System Manager
- Hard Processor System I/O Pin Multiplexing
Stratix 10 SoC Virtual Platform Version 1.0 Release Notes

This release note describes enhancements and known issues found in the 1.0 version of the Stratix 10 SoC Virtual Platform.

Enhancements to the Stratix 10 SoC Virtual Platform Version 1.0

The following functional models are available and have been tested in the 1.0 version of the Stratix 10 SoC Virtual Platform:

- Ethernet controller modules EMAC1 and EMAC2 (EMAC0 was available in 0.9)
- Universal serial bus controllers USB1 (USB0 was available in 0.9)
- UART1 (UART0 was available in 0.9)
- General interrupt controller

The following functional models are available but have not been fully tested in the 1.0 version of the Stratix 10 SoC Virtual Platform:

- Inter-Integrated Circuit (I²C) serial communication buses I2C0, I2C1, I2C2, I2C3 and I2C4
- General-purpose timers TMR_SYS0, TMR_SYS1, SPTIMER0 and SPTIMER1
- General-Purpose I/O modules GPIO0 and GPIO1
- Watchdog timers WDT0, WDT1, WDT2 and WDT3
- Non-secure DMA
- Serial Peripheral Interfaces SPI0, SPI1, SPI2, and SPI3

The following functionality is now available in the 1.0 version of the Stratix 10 Virtual Platform:

- Linux Symmetric Multiprocessing (SMP)
## Revision History of the Stratix 10 SoC Virtual Platform Release Notes

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
</tr>
</thead>
</table>
| January 2017 | 2017.01.20 | • Added section: "Known Issues in the Stratix 10 SoC Virtual Platform Version 1.3"  
  • Added section: "Advisory for the Stratix 10 SoC Virtual Platform Version 1.3"  |
| October 2016 | 2016.10.07 | Version 1.3 Release Notes                                              |
| July 2016   | 2016.07.15 | Version 1.2 Release Notes                                              |
| April 2016  | 2016.04.29 | Version 1.1 Release Notes                                              |
| March 2016  | 2016.03.04 | Version 1.0 Release Notes                                              |