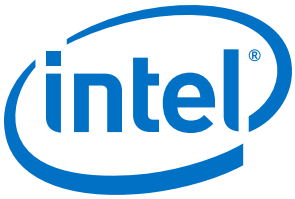

# Intel® Stratix® 10 Hard IP for PCI Express* IP Core Release Notes

Updated for Intel® Quartus® Prime Design Suite: **19.1**

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# Contents

# 1. Intel® Stratix® 10 Hard IP for PCI Express* IP Core Release Notes

## 1.1. Intel® Stratix® 10 Hard IP for PCI Express* IP Core v19.1

### Table 1. 19.1 March 2019

| Description | Impact |
|---|---|
| Added a chapter on the programming model for Root Ports to the Intel® Stratix® 10 Avalon®-MM Interface for PCI Express* Solutions User Guide. | Added the programming model for Root Ports to help users enable Root Ports. The model:<br>• Explains the Avalon-MM CRA interface registers.<br>• Explains sending and receiving TLPs through the CRA interface.<br>• Shows an example of BAR0 initialization. |
| Removed the note stating that Root Port mode is not recommended from the Intel Stratix 10 Avalon-MM and Intel Stratix 10 Avalon-ST for PCI Express Solutions User Guides. | Root Port mode is fully supported in this release for both Avalon-MM and Avalon-ST IPs. |
| Removed the *BIOS Enumeration Issue* section from the *Troubleshooting* chapter of all Intel Stratix 10 PCI Express User Guides. | Since Intel Stratix 10 devices support the autonomous Hard IP feature, they can be recognized by the OS/BIOS during enumeration without having to be fully programmed. |
| Added the note stating that the `bam_response_i[1:0]` inputs should be driven to 0 to the Intel Stratix 10 Avalon-MM Hard IP+ for PCI Express User Guide. | Clarified that these inputs are reserved; hence, they should be driven to 0. |

## 1.2. Intel Stratix 10 Hard IP for PCI Express IP Core v18.1.1

### Table 2. 18.1.1 December 2018

| Description | Impact |
|---|---|
| Added the Link Inspector Avalon-MM Interface to the Avalon-ST, Avalon-MM and Avalon-MM Hard IP+ for PCI Express IPs. | This interface allows you to access low-level link status information from the PCIe Hard IP, XCVR or PLL blocks via the Link Inspector without using the System Console. |
| Added the completion timeout checking feature to the Avalon-MM Hard IP+ for PCI Express IP. | This new option in the GUI (under the **Avalon-MM Settings** tab) allows you to receive a completion timeout error indicator on either the `rddm_tx_data_o[15]` port (if the Read Data Mover issued a Read operation to the host) or the `bas_response_o[1:0]` ports (if the Bursting Avalon Slave forwarded a Read operation to the host). |
| Added the feature to trigger MSI interrupts via the `rxm_irq_i` ports to the Avalon-MM for PCI Express IP. | This feature allows the IP core to convert a rising edge on one of the `rxm_irq_i` ports to an MSI interrupt and send it to the Root Port.<br>*Note:* the `rxm_irq_i` ports are not available when the IP core is operating in DMA mode. |

## 1.3. Intel Stratix 10 Hard IP for PCI Express IP Core v18.0

### Table 3. 18.0 May 2018

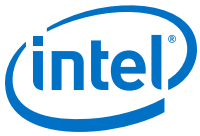
| Description | Impact |
|---|---|
| Initial release of the Avalon-MM Intel Stratix 10 Hard IP+ for PCI Express. | Added a new IP component to enable Avalon-MM support for Gen3 x16 mode. This IP core supports up to four functions. The support level is Advance. |
| Added support for 64-bit Avalon-MM application interface width. | In addition to the native 256-bit interface available, support for a 64-bit Avalon-MM interface (without DMA) is added. |
| VHDL compilation and simulation are not supported in the 18.0 release. | You can only simulate and compile in Verilog in the 18.0 release. |
| Single Root I/O Virtualization (SR-IOV) support for H-Tile variants. | Dynamic example design generation, compilation, simulation, and hardware support for SR-IOV have been added for Avalon-ST mode only. |
| First-level Signal Tap file. | Support to generate a Signal Tap file through a pre-compiled script has been enabled. |
| Software application for the Avalon-MM IP (with or without DMA). | Linux kernel driver, API, and an example command-line application using the API are available to enable testing of the Avalon-MM example designs (with or without DMA). The example application can also give rough estimates on the performance of the example design within the system. This application supports all link widths and speeds. |
| Intel Stratix 10 timing failures in example designs (Gen3 x16 Avalon-ST and Gen3 x16 Avalon-ST with SR-IOV). | Small hold violations (i.e: < 5 ps slack).<br>Setup violations can be observed on ES devices. |

## 1.4. Intel Stratix 10 Hard IP for PCI Express IP Core v17.1

### Table 4. 17.1 November 2017

| Description | Impact |
|---|---|
| Initial release. | N/A |
| VHDL compilation and simulation are not supported in the current release. | You can only simulate in Verilog in the current release. |
| The automatically generated simple DMA design example has timing issues.<br>This timing problem does not affect DMA designs that use the internal descriptor controller or DMA designs that use an external DMA controller to drive the internal Read and Write Data Movers. These designs close timing and function correctly in hardware. | You can simulate the simple DMA design and successfully and generate an SRAM Object file (`*.sof`). However, if you download the `*.sof` to hardware, the hardware will fail. |
| Single Root I/O Virtualization (SR-IOV) support for H-Tile variants is preliminary in the 17.1 release. | You can enable SR-IOV using the parameter editor. SR-IOV supports basic simulation and compilation. However, SR-IOV is not fully verified. You may find functional problems in the current release. |

*continued...*



<table>
<tr><th>Description</th><th>Impact</th></tr>
<tr><td>The Root Port is preliminary in the 17.1 release.</td><td>You can enable the Root Port using the parameter editor. The Root Port supports basic simulation and compilation. However, the Root Port is not fully verified. You may find functional problems in the current release.</td></tr>
<tr><td>The Avalon Memory-Mapped (Avalon-MM) DMA functionality is preliminary in the 17.1 release.</td><td>You can use the Avalon-MM DMA functionality in the current release. Avalon-MM supports simulation and compilation. However, this functionality has not been fully verified. You may find functional problems.</td></tr>
<tr><td>Upon reboot, the Intel Stratix 10 Hard IP for PCI Express IP Core might be unable to exit BIOS enumeration.</td><td>This problem affects L-Tile ES1 and ES2 and H-Tile ES1 devices. It will be fixed in a future release.</td></tr>
<tr><td>The link acknowledge logic in the Intel Stratix 10 H-Tile ES2 devices has a encoding error. This encoding error results in the following incorrect link widths:
<table>
<tr><th>Actual Link Width</th><th>Link Acknowledge</th></tr>
<tr><td>x1</td><td>x16</td></tr>
<tr><td>x2</td><td>x1</td></tr>
<tr><td>x4</td><td>x2</td></tr>
<tr><td>x8</td><td>x4</td></tr>
<tr><td>x16</td><td>x8</td></tr>
</table>
</td><td>This problem will be fixed in a future release.</td></tr>
</table>

## Related Information

Errata for the Stratix 10 Hard IP for PCI Express IP Core in the Knowledge Base