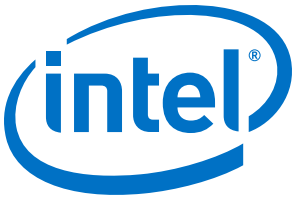

External Memory Interfaces Intel® Stratix® 10 FPGA IP Core Release Notes

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Contents

1. External Memory Interfaces Intel® Stratix® 10 FPGA IP Core Release Notes

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the *Intel® Quartus® Prime Design Suite Update Release Notes*.

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

The IP versioning scheme (X.Y.Z) number changes from one software version to another. A change in:

- X indicates a major revision of the IP. If you update your Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

1.1. External Memory Interfaces Intel Stratix® 10 FPGA IP v19.1.0

Table 1. v19.1.0 2019.07.01

Intel Quartus Prime Version	Description	Impact
19.2	Verified in the Intel Quartus Prime software v19.2.	—

1.2. External Memory Interfaces Intel Stratix® 10 FPGA IP 19.1

Table 2. v19.1 April 2019

Description	Impact
Verified in the Intel Quartus Prime software v19.1.	—

Related Information

- External Memory Interfaces Intel Stratix 10 FPGA IP User Guide
- External Memory Interfaces Intel Stratix 10 FPGA IP Design Example User Guide
- Intel Quartus Prime Design Suite Release Notes

1.3. External Memory Interfaces Intel Stratix® 10 FPGA IP 18.1.1

Table 3. v18.1.1 December 2018

Description	Impact
Added support for DDR4 clamshell layout.	—

Related Information

- External Memory Interfaces Intel Stratix 10 FPGA IP User Guide
- External Memory Interfaces Intel Stratix 10 FPGA IP Design Example User Guide
- Intel Quartus Prime Design Suite Release Notes

1.4. External Memory Interfaces Intel Stratix® 10 FPGA IP 18.1

Table 4. v18.1 September 2018

Description	Impact
Verified in the Intel Quartus Prime software v18.1.	Provides external memory interface IP for DDR3, DDR4, QDR II/II+/II+ Xtreme, QDR-IV, and RLDRAM 3 protocols for Intel Stratix® 10 devices. The tables below summarize speed and feature support.

Table 5. DDR4 EMIF IP Speed and Support Levels for Intel Stratix 10 GX, SX, MX, and TX Devices

Memory Format	Maximum Rate (Mbps/MHz)			EMIF IP Support Level by Intel Stratix 10 Device Grades			
	-1	-2	-3	GX	SX	MX	TX
UDIMM	2666/1333 (1R)	2400/1200 (1R)	1866/933 (1R)	S C T H	S C T H	S C T H	S C T H
	2400/1200 (2R)	2133/1066 (2R)	1600/800 (2R)	S C T H	S C T H	S C T H	S C T H
	2133/1066 (4R)	1866/933 (4R)	1333/667 (4R)	S C T H	S C T H	S C T H	S C T H
	1866/933 (2R +2R)	1600/800 (2R +2R)	1333/667 (2R+2R)	S C T H	S C T H	S C T H	S C T H
SODIMM	2666/1333 (1R)	2400/1200 (1R)	1866/933 (1R)	S C T H	S C T H	S C T H	S C T H
	2400/1200 (2R)	2133/1066 (2R)	1600/800 (2R)	S C T H	S C T H	S C T H	S C T H
	2133/1066 (4R)	1866/933 (4R)	1333/667 (4R)	S C T H	S C T H	S C T H	S C T H
	1866/933 (2R +2R)	1600/800 (2R +2R)	1333/667 (2R+2R)	S C T H	S C T H	S C T H	S C T H
RDIMM	2666/1333 (1R)	2400/1200 (1R)	1866/933 (1R)	S C T H	S C T H	S C T H	S C T H
	2400/1200 (2R)	2133/1066 (2R)	1600/800 (2R)	S C T H	S C T H	S C T H	S C T H
	2133/1066 (4R)	1866/933 (4R)	1333/667 (4R)	S C T H	S C T H	S C T H	S C T H
	1866/933 (2R +2R)	1600/800 (2R +2R)	1333/667 (2R+2R)	S C T H	S C T H	S C T H	S C T H

continued...

Memory Format	Maximum Rate (Mbps/MHz)			EMIF IP Support Level by Intel Stratix 10 Device Grades			
	-1	-2	-3	GX	SX	MX	TX
LRDIMM	2666/1333 (1R)	2400/1200 (1R)	1866/933 (1R)	S C T H	S C T H	S C T H	S C T H
	2666 / 1333 (2R)	2400/1200 (2R)	1866/933 (2R)	S C T H	S C T H	S C T H	S C T H
	2666 / 1333 (4R)	2400/1200 (4R)	1866/933 (4R)	S C T H	S C T H	S C T H	S C T H
	(2R+2R) - 2D4R configuration is supported for Intel Stratix 10 EMIF IP DDR4 LRDIMM						
Component	2666/1333	2400/1200	1866/933	S C T H	S C T H	S C T H	S C T H

Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support

Table 6. DDR4 EMIF IP Feature Support for Intel Stratix 10 GX, SX, MX, and TX Devices

Feature Category	Sub-Category	Supported?	EMIF IP Feature Support Level by Intel Stratix 10 Device Grades			
			GX	SX	MX	TX
Interface Width	<=72 with DIMM	Yes	S C T H	S C T H	S C T H	S C T H
	<=72 component	Yes	S C T H	S C T H	S C T H	S C T H
Controller	Hard controller	Yes	S C T H	S C T H	S C T H	S C T H
PHY	Hard PHY	Yes	S C T H	S C T H	S C T H	S C T H
	PHY Only	Yes	S C T H	S C T H	S C T H	S C T H
Ping Pong		Yes	S C T H	S C T H	S C T H	S C T H
Periodic OCT	Periodic OCT	No	–	–	–	–
3DS		Yes	S C T H	S C T H	S C T H	S C T H
Design Example		Yes	S C T H	S C T H	S C T H	S C T H
Rate (core)	Quarter	Yes	S C T H	S C T H	S C T H	S C T H
DBI	Read DBI	Yes	S C T H	S C T H	S C T H	S C T H
	Write DBI	Yes	S C T H	S C T H	S C T H	S C T H
Mirroring	Address Mirroring for odd ranks for multi rank DIMM	Yes	S C T H	S C T H	S C T H	S C T H
DM	DM pins	Yes	S C T H	S C T H	S C T H	S C T H
Preamble	Read Preamble settings	2	S C T H	S C T H	S C T H	S C T H
	Write Preamble settings	1	S C T H	S C T H	S C T H	S C T H
Refresh	Temperature-controlled	No	–	–	–	–
	Fine Granularity	No	–	–	–	–
	Auto self-refresh	No	–	–	–	–

continued...

Feature Category	Sub-Category	Supported?	EMIF IP Feature Support Level by Intel Stratix 10 Device Grades			
			GX	SX	MX	TX
	Self-refresh abort	No	–	–	–	–
ODT	Input buffer during power-down mode	No	–	–	–	–
Controller Features	ECC	Yes	S C T H	S C T H	S C T H	S C T H
	Reordering	Yes	S C T H	S C T H	S C T H	S C T H
	Auto Power Down	Yes	S C T H	S C T H	S C T H	S C T H
	User Refresh	Yes	S C T H	S C T H	S C T H	S C T H
	Auto Precharge	Yes	S C T H	S C T H	S C T H	S C T H
Calibration	Address/Command calibration	Yes	S C T H	S C T H	S C T H	S C T H
	Multi-rank calibration	Yes	S C T H	S C T H	S C T H	S C T H
Debug	EMIF Toolkit	Yes	C T H	C T H	C T H	C T H

Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support

Table 7. DDR3 EMIF IP Speed and Support Levels for Intel Stratix 10 GX, SX, MX, and TX Devices

Memory Format	Maximum Rate (Mbps/MHz)			EMIF IP Support Level by Intel Stratix 10 Device Grades			
	-1	-2	-3	GX	SX	MX	TX
UDIMM	2133/1066 (1R)	2133/1066 (1R)	1866/933 (1R)	S C T H	S C T H	S C T H	S C T H
	1866/933 (2R)	1866/933 (2R)	1600/800 (2R)	S C T H	S C T H	S C T H	S C T H
	1600/800 (4R)	1600/800 (4R)	1334/667 (4R)	S C T H	S C T H	S C T H	S C T H
	1334/667 (2R +2R)	1334/667 (2R +2R)	1334/667 (2R+2R)	S C T H	S C T H	S C T H	S C T H
SODIMM	2133/1066 (1R)	2133/1066 (1R)	1866/933 (1R)	S C T H	S C T H	S C T H	S C T H
	1866/933 (2R)	1866/933 (2R)	1600/800 (2R)	S C T H	S C T H	S C T H	S C T H
	1600/800 (4R)	1600/800 (4R)	1334/667 (4R)	S C T H	S C T H	S C T H	S C T H
	1334/667 (2R +2R)	1334/667 (2R +2R)	1334/667 (2R+2R)	S C T H	S C T H	S C T H	S C T H
RDIMM	2133/1066 (1R)	2133/1066 (1R)	1866/933 (1R)	S C T H	S C T H	S C T H	S C T H
	1866/933 (2R)	1866/933 (2R)	1600/800 (2R)	S C T H	S C T H	S C T H	S C T H
	1600/800 (4R)	1600/800 (4R)	1334/667 (4R)	S C T H	S C T H	S C T H	S C T H
	1334/667 (2R +2R)	1334/667 (2R +2R)	1334/667 (2R+2R)	S C T H	S C T H	S C T H	S C T H

continued...

Memory Format	Maximum Rate (Mbps/MHz)			EMIF IP Support Level by Intel Stratix 10 Device Grades			
	-1	-2	-3	GX	SX	MX	TX
LRDIMM	LRDIMM memory format is not supported for Intel Stratix 10 FPGA EMIF IP DDR3						
Component	2133/1066	2133/1066	1866/933	–	–	–	–

Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support

Table 8. DDR3 EMIF IP Feature Support for Intel Stratix 10 GX, SX, MX, and TX Devices

Feature Category	Sub-Category	Supported?	EMIF IP Feature Support Level by Intel Stratix 10 Device Grades			
			GX	SX	MX	TX
Interface Width	<=72 with DIMM	Yes	S C T H	S C T H	S C T H	S C T H
	<=72 component	Yes	S C T H	S C T H	S C T H	S C T H
Controller	Hard controller	Yes	S C T H	S C T H	S C T H	S C T H
PHY	Hard PHY	Yes	S C T H	S C T H	S C T H	S C T H
	PHY Only	Yes	S C T H	S C T H	S C T H	S C T H
Ping Pong		Yes	S C T H	S C T H	S C T H	S C T H
Design Example		Yes	S C T H	S C T H	S C T H	S C T H
Rate (core)	Quarter	Yes	S C T H	S C T H	S C T H	S C T H
	Half	Yes	S C T H	S C T H	S C T H	S C T H
Mirroring	Address Mirroring for odd ranks for multi rank DIMM	Yes	S C T H	S C T H	S C T H	S C T H
DM	DM pin	Yes	S C T H	S C T H	S C T H	S C T H
Controller Features	ECC	Yes	S C T H	S C T H	S C T H	S C T H
	Reordering	Yes	S C T H	S C T H	S C T H	S C T H
	Auto Power Down	Yes	S C T H	S C T H	S C T H	S C T H
	User Refresh	Yes	S C T H	S C T H	S C T H	S C T H
	Auto Precharge	Yes	S C T H	S C T H	S C T H	S C T H
	Command Priority	Yes	S C T H	S C T H	S C T H	S C T H
Calibration	Address/Command calibration	Yes	S C T H	S C T H	S C T H	S C T H
	Multirank calibration	Yes	S C T H	S C T H	S C T H	S C T H
Debug	EMIF Toolkit	Yes	C T H	C T H	C T H	C T H

Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support

Table 9. QDR-IV and QDR II/II+/Xtreme EMIF IP Speed and Support Levels for Intel Stratix 10 GX, SX, MX, and TX Devices

Protocol	Maximum Rate (Mbps/MHz)			EMIF IP Support Level by Intel Stratix 10 Device Grades			
	-1	-2	-3	GX	SX	MX	TX
QDR-IV	2133/1066	2133/1066	1866/933	S C T H	S C T H	S C T H	S C T H
QDR II+ Xtreme BL=4	1266/633	1100/550	1000/500	S C T H	S C T H	S C T H	S C T H
QDR II+ Xtreme BL=2	900/450	800/400	800/400	S C T H	S C T H	S C T H	S C T H
QDR II+ BL=4	1100/550	1000/500	900/450	S C T H	S C T H	S C T H	S C T H
QDR II+ BL=2	800/400	700/350	600/300	S C T H	S C T H	S C T H	S C T H
QDR II BL=4	700/350	700/350	700/350	S C T H	S C T H	S C T H	S C T H
QDR II BL=2	600/300	600/300	600/300	S C T H	S C T H	S C T H	S C T H

Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support

Table 10. QDR-IV EMIF IP Feature Support for Intel Stratix 10 GX, SX, MX, and TX Devices

Feature Category	Sub-Category	Supported?	EMIF IP Feature Support Level by Intel Stratix 10 Device Grades			
			GX	SX	MX	TX
Memory Format	Component	Yes	S C T H	S C T H	S C T H	S C T H
Memory Type	XP	Yes	S C T H	S C T H	S C T H	S C T H
Interface Width	<=72 with DIMM	Yes	S C T H	S C T H	S C T H	S C T H
Controller	Soft controller	Yes	S C T H	S C T H	S C T H	S C T H
PHY	Hard PHY	Yes	S C T H	S C T H	S C T H	S C T H
Design Example		Yes	S C T H	S C T H	S C T H	S C T H
Rate (core)	Quarter	Yes	S C T H	S C T H	S C T H	S C T H
Debug	EMIF Toolkit	Yes	C T H	C T H	C T H	C T H

Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support

Table 11. QDR II/II+/Xtreme EMIF IP Feature Support for Intel Stratix 10 GX, SX, MX, and TX Devices

Feature Category	Sub-Category	Supported?	EMIF IP Feature Support Level by Intel Stratix 10 Device Grades			
			GX	SX	MX	TX
Memory Format	Component	Yes	S C T H	S C T H	S C T H	S C T H
Interface Width	<=72 with DIMM	Yes	S C T H	S C T H	S C T H	S C T H
PHY	Hard PHY	Yes	S C T H	S C T H	S C T H	S C T H
Design Example		Yes	S C T H	S C T H	S C T H	S C T H
Rate (core)	Half	Yes	S C T H	S C T H	S C T H	S C T H
	Full	Yes	S C T H	S C T H	S C T H	S C T H
Debug	EMIF Toolkit	Yes	S C T H	S C T H	S C T H	S C T H

Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support

Table 12. RLDRAM 3 EMIF IP Speed and Support Levels for Intel Stratix 10 GX, SX, MX, and TX Devices

Format	Maximum Rate (Mbps/MHz)			EMIF IP Support Level by Intel Stratix 10 Device Grades			
	-1	-2	-3	GX	SX	MX	TX
Component	2400/1200	2133/1066	1866/933	S C T H	S C T H	S C T H	S C T H

Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support

Table 13. RLDRAM 3 EMIF IP Feature Support for Intel Stratix 10 GX, SX, MX, and TX Devices

Feature Category	Sub-Category	Supported?	EMIF IP Feature Support Level by Intel Stratix 10 Device Grades			
			GX	SX	MX	TX
Interface Width	<=72 with DIMM	Yes	S C T H	S C T H	S C T H	S C T H
Controller		No	–	–	–	–
PHY	Hard PHY only	Yes	S C T H	S C T H	S C T H	S C T H
Design Example		Yes	S C T H	S C T H	S C T H	S C T H
Rate (core)	Quarter	Yes	S C T H	S C T H	S C T H	S C T H
DM	DM pins	Yes	S C T H	S C T H	S C T H	S C T H
Debug	EMIF Toolkit	Yes	C T H	C T H	C T H	C T H

Support level key:

continued...

Feature Category	Sub-Category	Supported?	EMIF IP Feature Support Level by Intel Stratix 10 Device Grades			
			GX	SX	MX	TX
• S = simulation support • C = compilation support • T = timing support • H = hardware support						

Table 14. EMIF IP Debug Support

		Supported?
On-chip debug	On-chip debug (with soft Nios®)	Yes)
EMIF Debug Toolkit	Calibration margin	Yes
	Traffic Generator 2.0	No
	2D Eye	Yes
	Driver margining	Yes
	Efficiency monitor	Yes
	ODT Tuning	Yes
	RDBI + Driver margining	Yes
	Rank support	Yes

Related Information

- External Memory Interfaces Intel Stratix 10 FPGA IP User Guide
- External Memory Interfaces Intel Stratix 10 FPGA IP Design Example User Guide
- Intel Quartus Prime Design Suite Release Notes

1.5. External Memory Interfaces Intel Stratix 10 FPGA IP 18.0

Table 15. v18.0 May 2018

Description	Impact
Verified in the Intel Quartus Prime software v18.0.	Provides external memory interface IP for DDR3, DDR4, QDR II/II+/II+ Xtreme, QDR-IV, and RLDRAM 3 protocols for Intel Stratix 10 devices. The tables below summarize speed and feature support.

Table 16. DDR4 EMIF IP Speed and Support Levels for Intel Stratix 10 GX, SX, MX, and TX Devices

Memory Format	Maximum Rate (Mbps/MHz)			EMIF IP Support Level by Intel Stratix 10 Device Grades			
	-1	-2	-3	GX	SX	MX	TX
UDIMM	2666/1333 (1R)	2400/1200 (1R)	1866/933 (1R)	S C T H	S C T H	S C T H	S C T H
	2400/1200 (2R)	2133/1066 (2R)	1600/800 (2R)	S C T H	S C T H	S C T H	S C T H
	2133/1066 (4R)	1866/933 (4R)	1333/667 (4R)	S C T H	S C T H	S C T H	S C T H

continued...

Memory Format	Maximum Rate (Mbps/MHz)			EMIF IP Support Level by Intel Stratix 10 Device Grades			
	-1	-2	-3	GX	SX	MX	TX
	1866/933 (2R +2R)	1600/800 (2R +2R)	1333/667 (2R+2R)	S C T H	S C T H	S C T H	S C T H
SODIMM	2666/1333 (1R)	2400/1200 (1R)	1866/933 (1R)	S C T H	S C T H	S C T H	S C T H
	2400/1200 (2R)	2133/1066 (2R)	1600/800 (2R)	S C T H	S C T H	S C T H	S C T H
	2133/1066 (4R)	1866/933 (4R)	1333/667 (4R)	S C T H	S C T H	S C T H	S C T H
	1866/933 (2R +2R)	1600/800 (2R +2R)	1333/667 (2R+2R)	S C T H	S C T H	S C T H	S C T H
RDIMM	2666/1333 (1R)	2400/1200 (1R)	1866/933 (1R)	S C T H	S C T H	S C T H	S C T H
	2400/1200 (2R)	2133/1066 (2R)	1600/800 (2R)	S C T H	S C T H	S C T H	S C T H
	2133/1066 (4R)	1866/933 (4R)	1333/667 (4R)	S C T H	S C T H	S C T H	S C T H
	1866/933 (2R +2R)	1600/800 (2R +2R)	1333/667 (2R+2R)	S C T H	S C T H	S C T H	S C T H
LRDIMM	2666/1333 (1R)	2400/1200 (1R)	1866/933 (1R)	S C T H	S C T H	S C T H	S C T H
	2666 / 1333 (2R)	2400/1200 (2R)	1866/933 (2R)	S C T H	S C T H	S C T H	S C T H
	2666 / 1333 (4R)	2400/1200 (4R)	1866/933 (4R)	S C T H	S C T H	S C T H	S C T H
	(2R+2R) - 2D4R configuration is supported for Intel Stratix 10 EMIF IP DDR4 LRDIMM						
Component	2666/1333	2400/1200	1866/933	S C T H	S C T H	S C T H	S C T H

Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support

Table 17. DDR4 EMIF IP Feature Support for Intel Stratix 10 GX, SX, MX, and TX Devices

Feature Category	Sub-Category	Supported?	EMIF IP Feature Support Level by Intel Stratix 10 Device Grades			
			GX	SX	MX	TX
Interface Width	<=72 with DIMM	Yes	S C T H	S C T H	S C T H	S C T H
	<=72 component	Yes	S C T H	S C T H	S C T H	S C T H
Controller	Hard controller	Yes	S C T H	S C T H	S C T H	S C T H
PHY	Hard PHY	Yes	S C T H	S C T H	S C T H	S C T H
	PHY Only	Yes	S C T H	S C T H	S C T H	S C T H
Ping Pong		Yes	S C T H	S C T H	S C T H	S C T H
Periodic OCT	Periodic OCT	No	–	–	–	–
3DS		Yes	S C T H	S C T H	S C T H	S C T H
Design Example		Yes	S C T H	S C T H	S C T H	S C T H

continued...

Feature Category	Sub-Category	Supported?	EMIF IP Feature Support Level by Intel Stratix 10 Device Grades			
			GX	SX	MX	TX
Rate (core)	Quarter	Yes	S C T H	S C T H	S C T H	S C T H
DBI	Read DBI	Yes	S C T H	S C T H	S C T H	S C T H
	Write DBI	Yes	S C T H	S C T H	S C T H	S C T H
Mirroring	Address Mirroring for odd ranks for multi rank DIMM	Yes	S C T H	S C T H	S C T H	S C T H
DM	DM pins	Yes	S C T H	S C T H	S C T H	S C T H
Preamble	Read Preamble settings	2	S C T H	S C T H	S C T H	S C T H
	Write Preamble settings	1	S C T H	S C T H	S C T H	S C T H
Refresh	Temperature-controlled	No	–	–	–	–
	Fine Granularity	No	–	–	–	–
	Auto self-refresh	No	–	–	–	–
	Self-refresh abort	No	–	–	–	–
ODT	Input buffer during power-down mode	No	–	–	–	–
Controller Features	ECC	Yes	S C T H	S C T H	S C T H	S C T H
	Reordering	Yes	S C T H	S C T H	S C T H	S C T H
	Auto Power Down	Yes	S C T H	S C T H	S C T H	S C T H
	User Refresh	Yes	S C T H	S C T H	S C T H	S C T H
	Auto Precharge	Yes	S C T H	S C T H	S C T H	S C T H
	Command Priority	Yes	S C T H	S C T H	S C T H	S C T H
Calibration	Address/Command calibration	Yes	S C T H	S C T H	S C T H	S C T H
	Multi-rank calibration	Yes	S C T H	S C T H	S C T H	S C T H
Debug	EMIF Toolkit	Yes	C T H	C T H	C T H	C T H

Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support

Table 18. DDR3 EMIF IP Speed and Support Levels for Intel Stratix 10 GX, SX, MX, and TX Devices

Memory Format	Maximum Rate (Mbps/MHz)			EMIF IP Support Level by Intel Stratix 10 Device Grades			
	-1	-2	-3	GX	SX	MX	TX
UDIMM	2133/1066 (1R)	2133/1066 (1R)	1866/933 (1R)	S C T H	S C T H	S C T H	S C T H
	1866/933 (2R)	1866/933 (2R)	1600/800 (2R)	S C T H	S C T H	S C T H	S C T H
	1600/800 (4R)	1600/800 (4R)	1334/667 (4R)	S C T H	S C T H	S C T H	S C T H
	1334/667 (2R +2R)	1334/667 (2R +2R)	1334/667 (2R+2R)	S C T H	S C T H	S C T H	S C T H

continued...

Memory Format	Maximum Rate (Mbps/MHz)			EMIF IP Support Level by Intel Stratix 10 Device Grades			
	-1	-2	-3	GX	SX	MX	TX
SODIMM	2133/1066 (1R)	2133/1066 (1R)	1866/933 (1R)	S C T H	S C T H	S C T H	S C T H
	1866/933 (2R)	1866/933 (2R)	1600/800 (2R)	S C T H	S C T H	S C T H	S C T H
	1600/800 (4R)	1600/800 (4R)	1334/667 (4R)	S C T H	S C T H	S C T H	S C T H
	1334/667 (2R +2R)	1334/667 (2R +2R)	1334/667 (2R+2R)	S C T H	S C T H	S C T H	S C T H
RDIMM	2133/1066 (1R)	2133/1066 (1R)	1866/933 (1R)	S C T H	S C T H	S C T H	S C T H
	1866/933 (2R)	1866/933 (2R)	1600/800 (2R)	S C T H	S C T H	S C T H	S C T H
	1600/800 (4R)	1600/800 (4R)	1334/667 (4R)	S C T H	S C T H	S C T H	S C T H
	1334/667 (2R +2R)	1334/667 (2R +2R)	1334/667 (2R+2R)	S C T H	S C T H	S C T H	S C T H
LRDIMM	LRDIMM memory format is not supported for Intel Stratix 10 FPGA EMIF IP DDR3						
Component	2133/1066	2133/1066	1866/933	–	–	–	–

Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support

Table 19. DDR3 EMIF IP Feature Support for Intel Stratix 10 GX, SX, MX, and TX Devices

Feature Category	Sub-Category	Supported?	EMIF IP Feature Support Level by Intel Stratix 10 Device Grades			
			GX	SX	MX	TX
Interface Width	<=72 with DIMM	Yes	S C T H	S C T H	S C T H	S C T H
	<=72 component	Yes	S C T H	S C T H	S C T H	S C T H
Controller	Hard controller	Yes	S C T H	S C T H	S C T H	S C T H
PHY	Hard PHY	Yes	S C T H	S C T H	S C T H	S C T H
	PHY Only	Yes	S C T H	S C T H	S C T H	S C T H
Ping Pong		Yes	S C T H	S C T H	S C T H	S C T H
Design Example		Yes	S C T H	S C T H	S C T H	S C T H
Rate (core)	Quarter	Yes	S C T H	S C T H	S C T H	S C T H
	Half	Yes	S C T H	S C T H	S C T H	S C T H
	Full	Yes	S C T H	S C T H	S C T H	S C T H
Mirroring	Address Mirroring for odd ranks for multi rank DIMM	Yes	S C T H	S C T H	S C T H	S C T H
DM	DM pin	Yes	S C T H	S C T H	S C T H	S C T H
Controller Features	ECC	Yes	S C T H	S C T H	S C T H	S C T H
	Reordering	Yes	S C T H	S C T H	S C T H	S C T H

continued...

Feature Category	Sub-Category	Supported?	EMIF IP Feature Support Level by Intel Stratix 10 Device Grades			
			GX	SX	MX	TX
	Auto Power Down	Yes	S C T H	S C T H	S C T H	S C T H
	User Refresh	Yes	S C T H	S C T H	S C T H	S C T H
	Auto Precharge	Yes	S C T H	S C T H	S C T H	S C T H
	Command Priority	Yes	S C T H	S C T H	S C T H	S C T H
Calibration	Address/Command calibration	Yes	S C T H	S C T H	S C T H	S C T H
	Multirank calibration	Yes	S C T H	S C T H	S C T H	S C T H
Debug	EMIF Toolkit	Yes	C T H	C T H	C T H	C T H

Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support

Table 20. QDR-IV and QDR II/II+/Xtreme EMIF IP Speed and Support Levels for Intel Stratix 10 GX, SX, MX, and TX Devices

Protocol	Maximum Rate (Mbps/MHz)			EMIF IP Support Level by Intel Stratix 10 Device Grades			
	-1	-2	-3	GX	SX	MX	TX
QDR-IV	2133/1066	2133/1066	1866/933	S C T H	S C T H	S C T H	S C T H
QDR II+ Xtreme BL=4	1266/633	1100/550	1000/500	S C T H	S C T H	S C T H	S C T H
QDR II+ Xtreme BL=2	900/450	800/400	800/400	S C T H	S C T H	S C T H	S C T H
QDR II+ BL=4	1100/550	1000/500	900/450	S C T H	S C T H	S C T H	S C T H
QDR II+ BL=2	800/400	700/350	600/300	S C T H	S C T H	S C T H	S C T H
QDR II BL=4	700/350	700/350	700/350	S C T H	S C T H	S C T H	S C T H
QDR II BL=2	600/300	600/300	600/300	S C T H	S C T H	S C T H	S C T H

Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support

Table 21. QDR-IV EMIF IP Feature Support for Intel Stratix 10 GX, SX, MX, and TX Devices

Feature Category	Sub-Category	Supported?	EMIF IP Feature Support Level by Intel Stratix 10 Device Grades			
			GX	SX	MX	TX
Memory Format	Component	Yes	S C T H	S C T H	S C T H	S C T H
Memory Type	XP	Yes	S C T H	S C T H	S C T H	S C T H
Interface Width	<=72 with DIMM	Yes	S C T H	S C T H	S C T H	S C T H
Controller	Soft controller	Yes	S C T H	S C T H	S C T H	S C T H
PHY	Hard PHY	Yes	S C T H	S C T H	S C T H	S C T H
Design Example		Yes	S C T H	S C T H	S C T H	S C T H
Rate (core)	Quarter	Yes	S C T H	S C T H	S C T H	S C T H
Debug	EMIF Toolkit	Yes	C T H	C T H	C T H	C T H

Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support

Table 22. QDR II/II+/Xtreme EMIF IP Feature Support for Intel Stratix 10 GX, SX, MX, and TX Devices

Feature Category	Sub-Category	Supported?	EMIF IP Feature Support Level by Intel Stratix 10 Device Grades			
			GX	SX	MX	TX
Memory Format	Component	Yes	S C T H	S C T H	S C T H	S C T H
Interface Width	<=72 with DIMM	Yes	S C T H	S C T H	S C T H	S C T H
PHY	Hard PHY	Yes	S C T H	S C T H	S C T H	S C T H
Design Example		Yes	S C T H	S C T H	S C T H	S C T H
Rate (core)	Half	Yes	S C T H	S C T H	S C T H	S C T H
	Full	Yes	S C T H	S C T H	S C T H	S C T H
Debug	EMIF Toolkit	Yes	S C T H	S C T H	S C T H	S C T H

Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support

Table 23. RLDRAM 3 EMIF IP Speed and Support Levels for Intel Stratix 10 GX, SX, MX, and TX Devices

Format	Maximum Rate (Mbps/MHz)			EMIF IP Support Level by Intel Stratix 10 Device Grades			
	-1	-2	-3	GX	SX	MX	TX
Component	2400/1200	2133/1066	1866/933	S C T H	S C T H	S C T H	S C T H

Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support

Table 24. RLDRAM 3 EMIF IP Feature Support for Intel Stratix 10 GX, SX, MX, and TX Devices

Feature Category	Sub-Category	Supported?	EMIF IP Feature Support Level by Intel Stratix 10 Device Grades			
			GX	SX	MX	TX
Interface Width	<=72 with DIMM	Yes	S C T H	S C T H	S C T H	S C T H
Controller		No	–	–	–	–
PHY	Hard PHY only	Yes	S C T H	S C T H	S C T H	S C T H
Design Example		Yes	S C T H	S C T H	S C T H	S C T H
Rate (core)	Quarter	Yes	S C T H	S C T H	S C T H	S C T H
DM	DM pins	Yes	S C T H	S C T H	S C T H	S C T H
Debug	EMIF Toolkit	Yes	C T H	C T H	C T H	C T H

Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support

Table 25. EMIF IP Debug Support

		Supported?
On-chip debug	On-chip debug (with soft Nios)	Yes
EMIF Debug Toolkit	Calibration margin	Yes
	Traffic Generator 2.0	No
	2D Eye	No
	Driver margining	Yes
	Efficiency monitor	No
	ODT Tuning	Yes
	RDBI + Driver margining	Yes
	Rank support	Yes

Related Information

- External Memory Interfaces Intel Stratix 10 FPGA IP User Guide
- External Memory Interfaces Intel Stratix 10 FPGA IP Design Example User Guide
- Intel Quartus Prime Design Suite Release Notes

1.6. Intel Stratix 10 External Memory Interface IP 17.1

Table 26. v17.1 November 2017

Description	Impact
Initial release.	Provides external memory interface IP for DDR3, DDR4, QDR II/II+/II+ Xtreme, QDR-IV, and RLDRAM 3 protocols for Intel Stratix 10 devices.

Related Information

Intel Quartus Prime Design Suite Release Notes