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1. External Memory Interfaces Intel® Stratix® 10 FPGA IP Core Release Notes

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the Intel® Quartus® Prime Design Suite Update Release Notes.

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

The IP versioning scheme (X.Y.Z) number changes from one software version to another. A change in:

- X indicates a major revision of the IP. If you update your Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

1.1. External Memory Interfaces Intel Stratix® 10 FPGA IP v19.1.0

Table 1. v19.1.0 2019.07.01

<table>
<thead>
<tr>
<th>Intel Quartus Prime Version</th>
<th>Description</th>
<th>Impact</th>
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1.2. External Memory Interfaces Intel Stratix® 10 FPGA IP 19.1

Table 2. v19.1 April 2019

<table>
<thead>
<tr>
<th>Description</th>
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<td>Verified in the Intel Quartus Prime software v19.1.</td>
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Related Information

- External Memory Interfaces Intel Stratix 10 FPGA IP User Guide
- External Memory Interfaces Intel Stratix 10 FPGA IP Design Example User Guide
- Intel Quartus Prime Design Suite Release Notes
1.3. External Memory Interfaces Intel Stratix® 10 FPGA IP 18.1.1

Table 3. v18.1.1 December 2018

<table>
<thead>
<tr>
<th>Description</th>
<th>Impact</th>
</tr>
</thead>
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<tr>
<td>Added support for DDR4 clamshell layout.</td>
<td>—</td>
</tr>
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</table>

Related Information
- External Memory Interfaces Intel Stratix 10 FPGA IP User Guide
- External Memory Interfaces Intel Stratix 10 FPGA IP Design Example User Guide
- Intel Quartus Prime Design Suite Release Notes

1.4. External Memory Interfaces Intel Stratix® 10 FPGA IP 18.1

Table 4. v18.1 September 2018

<table>
<thead>
<tr>
<th>Description</th>
<th>Impact</th>
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Table 5. DDR4 EMIF IP Speed and Support Levels for Intel Stratix 10 GX, SX, MX, and TX Devices

<table>
<thead>
<tr>
<th>Memory Format</th>
<th>Maximum Rate (Mbps/MHz)</th>
<th>EMIF IP Support Level by Intel Stratix 10 Device Grades</th>
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<tbody>
<tr>
<td></td>
<td>-1</td>
<td>-2</td>
</tr>
<tr>
<td>UDIMM</td>
<td>2666/1333 (1R)</td>
<td>2400/1200 (1R)</td>
</tr>
<tr>
<td></td>
<td>2400/1200 (2R)</td>
<td>2133/1066 (2R)</td>
</tr>
<tr>
<td></td>
<td>2133/1066 (4R)</td>
<td>1866/933 (4R)</td>
</tr>
<tr>
<td></td>
<td>1866/933 (2R+2R)</td>
<td>1600/800 (2R+2R)</td>
</tr>
<tr>
<td>SODIMM</td>
<td>2666/1333 (1R)</td>
<td>2400/1200 (1R)</td>
</tr>
<tr>
<td></td>
<td>2400/1200 (2R)</td>
<td>2133/1066 (2R)</td>
</tr>
<tr>
<td></td>
<td>2133/1066 (4R)</td>
<td>1866/933 (4R)</td>
</tr>
<tr>
<td></td>
<td>1866/933 (2R+2R)</td>
<td>1600/800 (2R+2R)</td>
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<tr>
<td>RDIMM</td>
<td>2666/1333 (1R)</td>
<td>2400/1200 (1R)</td>
</tr>
<tr>
<td></td>
<td>2400/1200 (2R)</td>
<td>2133/1066 (2R)</td>
</tr>
<tr>
<td></td>
<td>2133/1066 (4R)</td>
<td>1866/933 (4R)</td>
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<tr>
<td></td>
<td>1866/933 (2R+2R)</td>
<td>1600/800 (2R+2R)</td>
</tr>
</tbody>
</table>

continued...
## Table 6. DDR4 EMIF IP Feature Support for Intel Stratix 10 GX, SX, MX, and TX Devices

<table>
<thead>
<tr>
<th>Feature Category</th>
<th>Sub-Category</th>
<th>Supported?</th>
<th>EMIF IP Feature Support Level by Intel Stratix 10 Device Grades</th>
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<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>GX</td>
</tr>
<tr>
<td>Interface Width</td>
<td>&lt;=72 with DIMM</td>
<td>Yes</td>
<td>S C T H</td>
</tr>
<tr>
<td></td>
<td>&lt;=72 component</td>
<td>Yes</td>
<td>S C T H</td>
</tr>
<tr>
<td>Controller</td>
<td>Hard controller</td>
<td>Yes</td>
<td>S C T H</td>
</tr>
<tr>
<td>PHY</td>
<td>Hard PHY</td>
<td>Yes</td>
<td>S C T H</td>
</tr>
<tr>
<td></td>
<td>PHY Only</td>
<td>Yes</td>
<td>S C T H</td>
</tr>
<tr>
<td>Ping Pong</td>
<td></td>
<td>Yes</td>
<td>S C T H</td>
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<td>Periodic OCT</td>
<td>Periodic OCT</td>
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<td>3DS</td>
<td></td>
<td>Yes</td>
<td>S C T H</td>
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<td>Design Example</td>
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<td>Yes</td>
<td>S C T H</td>
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<tr>
<td>Rate (core)</td>
<td>Quarter</td>
<td>Yes</td>
<td>S C T H</td>
</tr>
<tr>
<td>DBI</td>
<td>Read DBI</td>
<td>Yes</td>
<td>S C T H</td>
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<tr>
<td></td>
<td>Write DBI</td>
<td>Yes</td>
<td>S C T H</td>
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<tr>
<td>Mirroring</td>
<td>Address Mirroring for odd ranks for multi rank DIMM</td>
<td>Yes</td>
<td>S C T H</td>
</tr>
<tr>
<td>DM</td>
<td>DM pins</td>
<td>Yes</td>
<td>S C T H</td>
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<td>Preamble</td>
<td>Read Preamble settings</td>
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<td>S C T H</td>
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<td></td>
<td>Write Preamble settings</td>
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<td>S C T H</td>
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<td>Refresh</td>
<td>Temperature-controlled</td>
<td>No</td>
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</tr>
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<td></td>
<td>Fine Granularity</td>
<td>No</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>Auto self-refresh</td>
<td>No</td>
<td>–</td>
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<td>Feature Category</td>
<td>Sub-Category</td>
<td>Supported?</td>
<td>EMIF IP Feature Support Level by Intel Stratix 10 Device Grades</td>
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<tr>
<td>------------------</td>
<td>-------------</td>
<td>------------</td>
<td>---------------------------------------------------------------</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>GX</td>
</tr>
<tr>
<td>Self-refresh abort</td>
<td>No</td>
<td>–</td>
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<tr>
<td>ODT</td>
<td>Input buffer during power-down mode</td>
<td>No</td>
<td>–</td>
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<td>Controller Features</td>
<td>ECC</td>
<td>Yes</td>
<td>S T H</td>
</tr>
<tr>
<td></td>
<td>Reordering</td>
<td>Yes</td>
<td>S T H</td>
</tr>
<tr>
<td></td>
<td>Auto Power Down</td>
<td>Yes</td>
<td>S T H</td>
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<tr>
<td></td>
<td>User Refresh</td>
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<td>S T H</td>
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<td></td>
<td>Auto Precharge</td>
<td>Yes</td>
<td>S T H</td>
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<tr>
<td>Calibration</td>
<td>Address/Command calibration</td>
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<td>S T H</td>
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<td></td>
<td>Multi-rank calibration</td>
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<td>S T H</td>
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<tr>
<td>Debug</td>
<td>EMIF Toolkit</td>
<td>Yes</td>
<td>C T H</td>
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</table>

Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support

Table 7. DDR3 EMIF IP Speed and Support Levels for Intel Stratix 10 GX, SX, MX, and TX Devices

<table>
<thead>
<tr>
<th>Memory Format</th>
<th>Maximum Rate (Mbps/MHz)</th>
<th>EMIF IP Support Level by Intel Stratix 10 Device Grades</th>
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<tbody>
<tr>
<td></td>
<td>-1</td>
<td>-2</td>
</tr>
<tr>
<td>UDIMM</td>
<td>2133/1066 (1R)</td>
<td>2133/1066 (1R)</td>
</tr>
<tr>
<td></td>
<td>1866/933 (2R)</td>
<td>1866/933 (2R)</td>
</tr>
<tr>
<td></td>
<td>1600/800 (4R)</td>
<td>1600/800 (4R)</td>
</tr>
<tr>
<td></td>
<td>1334/667 (2R+2R)</td>
<td>1334/667 (2R+2R)</td>
</tr>
<tr>
<td>SODIMM</td>
<td>2133/1066 (1R)</td>
<td>2133/1066 (1R)</td>
</tr>
<tr>
<td></td>
<td>1866/933 (2R)</td>
<td>1866/933 (2R)</td>
</tr>
<tr>
<td></td>
<td>1600/800 (4R)</td>
<td>1600/800 (4R)</td>
</tr>
<tr>
<td></td>
<td>1334/667 (2R+2R)</td>
<td>1334/667 (2R+2R)</td>
</tr>
<tr>
<td>RDIMM</td>
<td>2133/1066 (1R)</td>
<td>2133/1066 (1R)</td>
</tr>
<tr>
<td></td>
<td>1866/933 (2R)</td>
<td>1866/933 (2R)</td>
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<tr>
<td></td>
<td>1600/800 (4R)</td>
<td>1600/800 (4R)</td>
</tr>
<tr>
<td></td>
<td>1334/667 (2R+2R)</td>
<td>1334/667 (2R+2R)</td>
</tr>
</tbody>
</table>

continued...
Table 8. DDR3 EMIF IP Feature Support for Intel Stratix 10 GX, SX, MX, and TX Devices

<table>
<thead>
<tr>
<th>Feature Category</th>
<th>Sub-Category</th>
<th>Supported?</th>
<th>EMIF IP Feature Support Level by Intel Stratix 10 Device Grades</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>GX</td>
</tr>
<tr>
<td>Interface Width</td>
<td>&lt;=72 with DIMM</td>
<td>Yes</td>
<td>S</td>
</tr>
<tr>
<td></td>
<td>&lt;=72 component</td>
<td>Yes</td>
<td>S</td>
</tr>
<tr>
<td>Controller</td>
<td>Hard controller</td>
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<td>S</td>
</tr>
<tr>
<td>PHY</td>
<td>Hard PHY</td>
<td>Yes</td>
<td>S</td>
</tr>
<tr>
<td>PHY</td>
<td>PHY Only</td>
<td>Yes</td>
<td>S</td>
</tr>
<tr>
<td>Ping Pong</td>
<td></td>
<td>Yes</td>
<td>S</td>
</tr>
<tr>
<td>Design Example</td>
<td></td>
<td>Yes</td>
<td>S</td>
</tr>
<tr>
<td>Rate (core)</td>
<td>Quarter</td>
<td>Yes</td>
<td>S</td>
</tr>
<tr>
<td></td>
<td>Half</td>
<td>Yes</td>
<td>S</td>
</tr>
<tr>
<td>Mirroring</td>
<td>Address Mirroring for odd ranks for multi rank DIMM</td>
<td>Yes</td>
<td>S</td>
</tr>
<tr>
<td>DM</td>
<td>DM pin</td>
<td>Yes</td>
<td>S</td>
</tr>
<tr>
<td>Controller Features</td>
<td>ECC</td>
<td>Yes</td>
<td>S</td>
</tr>
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<td></td>
<td>Reordering</td>
<td>Yes</td>
<td>S</td>
</tr>
<tr>
<td></td>
<td>Auto Power Down</td>
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<td>S</td>
</tr>
<tr>
<td></td>
<td>User Refresh</td>
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<td>S</td>
</tr>
<tr>
<td></td>
<td>Auto Precharge</td>
<td>Yes</td>
<td>S</td>
</tr>
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<td></td>
<td>Command Priority</td>
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<td>S</td>
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<tr>
<td>Calibration</td>
<td>Address/Command calibration</td>
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<td>S</td>
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<td></td>
<td>Multirank calibration</td>
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<td>S</td>
</tr>
<tr>
<td>Debug</td>
<td>EMIF Toolkit</td>
<td>Yes</td>
<td>C</td>
</tr>
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Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support
Table 9. **QDR-IV and QDR II/II+/Xtreme EMIF IP Speed and Support Levels for Intel Stratix 10 GX, SX, MX, and TX Devices**

<table>
<thead>
<tr>
<th>Protocol</th>
<th>Maximum Rate (Mbps/MHz)</th>
<th>EMIF IP Support Level by Intel Stratix 10 Device Grades</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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<td>-2</td>
</tr>
<tr>
<td>QDR-IV</td>
<td>2133/1066</td>
<td>2133/1066</td>
</tr>
<tr>
<td>QDR II+</td>
<td>1266/633</td>
<td>1100/550</td>
</tr>
<tr>
<td>QDR II+ Xtreme BL=4</td>
<td>900/450</td>
<td>800/400</td>
</tr>
<tr>
<td>QDR II+ BL=2</td>
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<td>700/350</td>
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<td>600/300</td>
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</table>

Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support

Table 10. **QDR-IV EMIF IP Feature Support for Intel Stratix 10 GX, SX, MX, and TX Devices**

<table>
<thead>
<tr>
<th>Feature Category</th>
<th>Sub-Category</th>
<th>Supported?</th>
<th>EMIF IP Feature Support Level by Intel Stratix 10 Device Grades</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory Format</td>
<td>Component</td>
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<td>S C T H</td>
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<tr>
<td>Memory Type</td>
<td>XP</td>
<td>Yes</td>
<td>S C T H</td>
</tr>
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<td>Interface Width</td>
<td>&lt;=72 with DIMM</td>
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<td>S C T H</td>
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<tr>
<td>Controller</td>
<td>Soft controller</td>
<td>Yes</td>
<td>S C T H</td>
</tr>
<tr>
<td>PHY</td>
<td>Hard PHY</td>
<td>Yes</td>
<td>S C T H</td>
</tr>
<tr>
<td>Design Example</td>
<td></td>
<td>Yes</td>
<td>S C T H</td>
</tr>
<tr>
<td>Rate (core)</td>
<td>Quarter</td>
<td>Yes</td>
<td>S C T H</td>
</tr>
<tr>
<td>Debug</td>
<td>EMIF Toolkit</td>
<td>Yes</td>
<td>C T H</td>
</tr>
</tbody>
</table>

Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support
### Table 11. QDR II/II+/Xtreme EMIF IP Feature Support for Intel Stratix 10 GX, SX, MX, and TX Devices

<table>
<thead>
<tr>
<th>Feature Category</th>
<th>Sub-Category</th>
<th>Supported?</th>
<th>EMIF IP Feature Support Level by Intel Stratix 10 Device Grades</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory Format</td>
<td>Component</td>
<td>Yes</td>
<td>S C T H S C T H S C T H S C T H</td>
</tr>
<tr>
<td>Interface Width</td>
<td>&lt;=72 with DIMM</td>
<td>Yes</td>
<td>S C T H S C T H S C T H S C T H</td>
</tr>
<tr>
<td>PHY</td>
<td>Hard PHY</td>
<td>Yes</td>
<td>S C T H S C T H S C T H S C T H</td>
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<tr>
<td>Design Example</td>
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<td>S C T H S C T H S C T H S C T H</td>
</tr>
<tr>
<td>Rate (core)</td>
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<tr>
<td></td>
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</tr>
<tr>
<td>Debug</td>
<td>EMIF Toolkit</td>
<td>Yes</td>
<td>S C T H S C T H S C T H S C T H</td>
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</table>

Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support

### Table 12. RLDRAM 3 EMIF IP Speed and Support Levels for Intel Stratix 10 GX, SX, MX, and TX Devices

<table>
<thead>
<tr>
<th>Format</th>
<th>Maximum Rate (Mbps/MHz)</th>
<th>EMIF IP Support Level by Intel Stratix 10 Device Grades</th>
</tr>
</thead>
<tbody>
<tr>
<td>Component</td>
<td></td>
<td>S C T H S C T H S C T H S C T H</td>
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<tr>
<td>-1</td>
<td>2400/1200</td>
<td></td>
</tr>
<tr>
<td>-2</td>
<td>2133/1066</td>
<td></td>
</tr>
<tr>
<td>-3</td>
<td>1866/933</td>
<td></td>
</tr>
<tr>
<td>TX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SX</td>
<td></td>
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</tr>
</tbody>
</table>

Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support

### Table 13. RLDRAM 3 EMIF IP Feature Support for Intel Stratix 10 GX, SX, MX, and TX Devices

<table>
<thead>
<tr>
<th>Feature Category</th>
<th>Sub-Category</th>
<th>Supported?</th>
<th>EMIF IP Feature Support Level by Intel Stratix 10 Device Grades</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interface Width</td>
<td>&lt;=72 with DIMM</td>
<td>Yes</td>
<td>S C T H S C T H S C T H S C T H</td>
</tr>
<tr>
<td>Controller</td>
<td></td>
<td>No</td>
<td>-- -- -- --</td>
</tr>
<tr>
<td>PHY</td>
<td>Hard PHY only</td>
<td>Yes</td>
<td>S C T H S C T H S C T H S C T H</td>
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<td>Design Example</td>
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<td>Yes</td>
<td>S C T H S C T H S C T H S C T H</td>
</tr>
<tr>
<td>Rate (core)</td>
<td>Quarter</td>
<td>Yes</td>
<td>S C T H S C T H S C T H S C T H</td>
</tr>
<tr>
<td>DM</td>
<td>DM pins</td>
<td>Yes</td>
<td>S C T H S C T H S C T H S C T H</td>
</tr>
<tr>
<td>Debug</td>
<td>EMIF Toolkit</td>
<td>Yes</td>
<td>C T H C T H C T H C T H</td>
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</table>

Support level key:
### Table 14. EMIF IP Debug Support

<table>
<thead>
<tr>
<th>Feature Category</th>
<th>Sub-Category</th>
<th>Supported?</th>
</tr>
</thead>
<tbody>
<tr>
<td>EMIF IP Debug Support</td>
<td>On-chip debug</td>
<td>Yes</td>
</tr>
<tr>
<td>EMIF Debug Toolkit</td>
<td>Calibration margin</td>
<td>Yes</td>
</tr>
<tr>
<td></td>
<td>Traffic Generator 2.0</td>
<td>No</td>
</tr>
<tr>
<td></td>
<td>2D Eye</td>
<td>Yes</td>
</tr>
<tr>
<td></td>
<td>Driver margining</td>
<td>Yes</td>
</tr>
<tr>
<td></td>
<td>Efficiency monitor</td>
<td>Yes</td>
</tr>
<tr>
<td></td>
<td>ODT Tuning</td>
<td>Yes</td>
</tr>
<tr>
<td></td>
<td>RDBI + Driver margining</td>
<td>Yes</td>
</tr>
<tr>
<td></td>
<td>Rank support</td>
<td>Yes</td>
</tr>
</tbody>
</table>

### Related Information
- External Memory Interfaces Intel Stratix 10 FPGA IP User Guide
- External Memory Interfaces Intel Stratix 10 FPGA IP Design Example User Guide
- Intel Quartus Prime Design Suite Release Notes

### 1.5. External Memory Interfaces Intel Stratix 10 FPGA IP 18.0

### Table 15. v18.0 May 2018

<table>
<thead>
<tr>
<th>Description</th>
<th>Impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>Verified in the Intel Quartus Prime software v18.0.</td>
<td>Provides external memory interface IP for DDR3, DDR4, QDR II/II+/II+ Xtreme, QDR-IV, and RLDRAM 3 protocols for Intel Stratix 10 devices. The tables below summarize speed and feature support.</td>
</tr>
</tbody>
</table>

### Table 16. DDR4 EMIF IP Speed and Support Levels for Intel Stratix 10 GX, SX, MX, and TX Devices

<table>
<thead>
<tr>
<th>Memory Format</th>
<th>Maximum Rate (Mbps/MHz)</th>
<th>EMIF IP Support Level by Intel Stratix 10 Device Grades</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>-1</td>
<td>-2</td>
</tr>
<tr>
<td>UDIMM</td>
<td>2666/1333 (1R)</td>
<td>2400/1200 (1R)</td>
</tr>
<tr>
<td></td>
<td>2400/1200 (2R)</td>
<td>2133/1066 (2R)</td>
</tr>
<tr>
<td></td>
<td>2133/1066 (4R)</td>
<td>1866/933 (4R)</td>
</tr>
</tbody>
</table>

**continued...**
## Memory Format

<table>
<thead>
<tr>
<th>Memory Format</th>
<th>Maximum Rate (Mbps/MHz)</th>
<th>EMIF IP Support Level by Intel Stratix 10 Device Grades</th>
</tr>
</thead>
<tbody>
<tr>
<td>-1</td>
<td>-2</td>
<td>-3</td>
</tr>
<tr>
<td>1866/933 (2R +2R)</td>
<td>1600/800 (2R +2R)</td>
<td>1333/667 (2R+2R)</td>
</tr>
<tr>
<td>SODIMM</td>
<td>2666/1333 (1R)</td>
<td>2400/1200 (1R)</td>
</tr>
<tr>
<td></td>
<td>2400/1200 (2R)</td>
<td>2133/1066 (2R)</td>
</tr>
<tr>
<td></td>
<td>2133/1066 (4R)</td>
<td>1866/933 (4R)</td>
</tr>
<tr>
<td></td>
<td>1866/933 (2R +2R)</td>
<td>1600/800 (2R +2R)</td>
</tr>
<tr>
<td>RDIMM</td>
<td>2666/1333 (1R)</td>
<td>2400/1200 (1R)</td>
</tr>
<tr>
<td></td>
<td>2400/1200 (2R)</td>
<td>2133/1066 (2R)</td>
</tr>
<tr>
<td></td>
<td>2133/1066 (4R)</td>
<td>1866/933 (4R)</td>
</tr>
<tr>
<td></td>
<td>1866/933 (2R +2R)</td>
<td>1600/800 (2R +2R)</td>
</tr>
<tr>
<td>LRDIMM</td>
<td>2666/1333 (1R)</td>
<td>2400/1200 (1R)</td>
</tr>
<tr>
<td></td>
<td>2666 / 1333 (2R)</td>
<td>2400/1200 (2R)</td>
</tr>
<tr>
<td></td>
<td>2666 / 1333 (4R)</td>
<td>2400/1200 (4R)</td>
</tr>
<tr>
<td>Component</td>
<td>2666/1333</td>
<td>2400/1200</td>
</tr>
</tbody>
</table>

Support level key:
- **S** = simulation support
- **C** = compilation support
- **T** = timing support
- **H** = hardware support

(2R+2R) - 2D4R configuration is supported for Intel Stratix 10 EMIF IP DDR4 LRDIMM

---

### Table 17. DDR4 EMIF IP Feature Support for Intel Stratix 10 GX, SX, MX, and TX Devices

<table>
<thead>
<tr>
<th>Feature Category</th>
<th>Sub-Category</th>
<th>Supported?</th>
<th>EMIF IP Feature Support Level by Intel Stratix 10 Device Grades</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>GX</td>
</tr>
<tr>
<td>Interface Width</td>
<td>&lt;=72 with DIMM</td>
<td>Yes</td>
<td>S C T H</td>
</tr>
<tr>
<td></td>
<td>&lt;=72 component</td>
<td>Yes</td>
<td>S C T H</td>
</tr>
<tr>
<td>Controller</td>
<td>Hard controller</td>
<td>Yes</td>
<td>S C T H</td>
</tr>
<tr>
<td>PHY</td>
<td>Hard PHY</td>
<td>Yes</td>
<td>S C T H</td>
</tr>
<tr>
<td></td>
<td>PHY Only</td>
<td>Yes</td>
<td>S C T H</td>
</tr>
<tr>
<td>Ping Pong</td>
<td></td>
<td>Yes</td>
<td>S C T H</td>
</tr>
<tr>
<td>Periodic OCT</td>
<td>Periodic OCT</td>
<td>No</td>
<td>–</td>
</tr>
<tr>
<td>3DS</td>
<td></td>
<td>Yes</td>
<td>S C T H</td>
</tr>
<tr>
<td>Design Example</td>
<td></td>
<td>Yes</td>
<td>S C T H</td>
</tr>
</tbody>
</table>

**continued...**

---

Send Feedback
<table>
<thead>
<tr>
<th>Feature Category</th>
<th>Sub-Category</th>
<th>Supported?</th>
<th>EMIF IP Feature Support Level by Intel Stratix 10 Device Grades</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rate (core)</td>
<td>Quarter</td>
<td>Yes</td>
<td><strong>S C T H</strong> <strong>S C T H</strong> <strong>S C T H</strong> <strong>S C T H</strong></td>
</tr>
<tr>
<td>DBI</td>
<td>Read DBI</td>
<td>Yes</td>
<td><strong>S C T H</strong> <strong>S C T H</strong> <strong>S C T H</strong> <strong>S C T H</strong></td>
</tr>
<tr>
<td></td>
<td>Write DBI</td>
<td>Yes</td>
<td><strong>S C T H</strong> <strong>S C T H</strong> <strong>S C T H</strong> <strong>S C T H</strong></td>
</tr>
<tr>
<td>Mirroring</td>
<td>Address Mirroring for odd ranks for multi rank DIMM</td>
<td>Yes</td>
<td><strong>S C T H</strong> <strong>S C T H</strong> <strong>S C T H</strong> <strong>S C T H</strong></td>
</tr>
<tr>
<td>DM</td>
<td>DM pins</td>
<td>Yes</td>
<td><strong>S C T H</strong> <strong>S C T H</strong> <strong>S C T H</strong> <strong>S C T H</strong></td>
</tr>
<tr>
<td>Preamble</td>
<td>Read Preamble settings</td>
<td>2</td>
<td><strong>S C T H</strong> <strong>S C T H</strong> <strong>S C T H</strong> <strong>S C T H</strong></td>
</tr>
<tr>
<td></td>
<td>Write Preamble settings</td>
<td>1</td>
<td><strong>S C T H</strong> <strong>S C T H</strong> <strong>S C T H</strong> <strong>S C T H</strong></td>
</tr>
<tr>
<td>Refresh</td>
<td>Temperature-controlled</td>
<td>No</td>
<td>– – – –</td>
</tr>
<tr>
<td></td>
<td>Fine Granularity</td>
<td>No</td>
<td>– – – –</td>
</tr>
<tr>
<td></td>
<td>Auto self-refresh</td>
<td>No</td>
<td>– – – –</td>
</tr>
<tr>
<td></td>
<td>Self-refresh abort</td>
<td>No</td>
<td>– – – –</td>
</tr>
<tr>
<td>ODT</td>
<td>Input buffer during power-down mode</td>
<td>No</td>
<td>– – – –</td>
</tr>
<tr>
<td>Controller Features</td>
<td>ECC</td>
<td>Yes</td>
<td><strong>S C T H</strong> <strong>S C T H</strong> <strong>S C T H</strong> <strong>S C T H</strong></td>
</tr>
<tr>
<td></td>
<td>Reordering</td>
<td>Yes</td>
<td><strong>S C T H</strong> <strong>S C T H</strong> <strong>S C T H</strong> <strong>S C T H</strong></td>
</tr>
<tr>
<td></td>
<td>Auto Power Down</td>
<td>Yes</td>
<td><strong>S C T H</strong> <strong>S C T H</strong> <strong>S C T H</strong> <strong>S C T H</strong></td>
</tr>
<tr>
<td></td>
<td>User Refresh</td>
<td>Yes</td>
<td><strong>S C T H</strong> <strong>S C T H</strong> <strong>S C T H</strong> <strong>S C T H</strong></td>
</tr>
<tr>
<td></td>
<td>Auto Precharge</td>
<td>Yes</td>
<td><strong>S C T H</strong> <strong>S C T H</strong> <strong>S C T H</strong> <strong>S C T H</strong></td>
</tr>
<tr>
<td></td>
<td>Command Priority</td>
<td>Yes</td>
<td><strong>S C T H</strong> <strong>S C T H</strong> <strong>S C T H</strong> <strong>S C T H</strong></td>
</tr>
<tr>
<td>Calibration</td>
<td>Address/Command calibration</td>
<td>Yes</td>
<td><strong>S C T H</strong> <strong>S C T H</strong> <strong>S C T H</strong> <strong>S C T H</strong></td>
</tr>
<tr>
<td></td>
<td>Multi-rank calibration</td>
<td>Yes</td>
<td><strong>S C T H</strong> <strong>S C T H</strong> <strong>S C T H</strong> <strong>S C T H</strong></td>
</tr>
<tr>
<td>Debug</td>
<td>EMIF Toolkit</td>
<td>Yes</td>
<td><strong>C T H</strong> <strong>C T H</strong> <strong>C T H</strong> <strong>C T H</strong></td>
</tr>
</tbody>
</table>

Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support

Table 18. DDR3 EMIF IP Speed and Support Levels for Intel Stratix 10 GX, SX, MX, and TX Devices

<table>
<thead>
<tr>
<th>Memory Format</th>
<th>Maximum Rate (Mbps/MHz)</th>
<th>EMIF IP Support Level by Intel Stratix 10 Device Grades</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>-1</td>
<td>-2</td>
</tr>
<tr>
<td>UDIMM</td>
<td>2133/1066 (1R)</td>
<td>1866/933 (1R)</td>
</tr>
<tr>
<td></td>
<td>1866/933 (2R)</td>
<td>1600/800 (2R)</td>
</tr>
<tr>
<td></td>
<td>1600/800 (4R)</td>
<td>1334/667 (4R)</td>
</tr>
<tr>
<td></td>
<td>1334/667 (2R+2R)</td>
<td>1334/667 (2R+2R)</td>
</tr>
</tbody>
</table>

continued...
### Table 19. DDR3 EMIF IP Feature Support for Intel Stratix 10 GX, SX, MX, and TX Devices

<table>
<thead>
<tr>
<th>Feature Category</th>
<th>Sub-Category</th>
<th>Supported?</th>
<th>EMIF IP Feature Support Level by Intel Stratix 10 Device Grades</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interface Width</td>
<td>&lt;=72 with DIMM</td>
<td>Yes</td>
<td>S C T H   S C T H   S C T H   S C T H</td>
</tr>
<tr>
<td></td>
<td>&lt;=72 component</td>
<td>Yes</td>
<td>S C T H   S C T H   S C T H   S C T H</td>
</tr>
<tr>
<td>Controller</td>
<td>Hard controller</td>
<td>Yes</td>
<td>S C T H   S C T H   S C T H   S C T H</td>
</tr>
<tr>
<td>PHY</td>
<td>Hard PHY</td>
<td>Yes</td>
<td>S C T H   S C T H   S C T H   S C T H</td>
</tr>
<tr>
<td></td>
<td>PHY Only</td>
<td>Yes</td>
<td>S C T H   S C T H   S C T H   S C T H</td>
</tr>
<tr>
<td>Ping Pong</td>
<td></td>
<td>Yes</td>
<td>S C T H   S C T H   S C T H   S C T H</td>
</tr>
<tr>
<td>Design Example</td>
<td></td>
<td>Yes</td>
<td>S C T H   S C T H   S C T H   S C T H</td>
</tr>
<tr>
<td>Rate (core)</td>
<td>Quarter</td>
<td>Yes</td>
<td>S C T H   S C T H   S C T H   S C T H</td>
</tr>
<tr>
<td></td>
<td>Half</td>
<td>Yes</td>
<td>S C T H   S C T H   S C T H   S C T H</td>
</tr>
<tr>
<td></td>
<td>Full</td>
<td>Yes</td>
<td>S C T H   S C T H   S C T H   S C T H</td>
</tr>
<tr>
<td>Mirroring</td>
<td>Address Mirroring for odd ranks for multi rank DIMM</td>
<td>Yes</td>
<td>S C T H   S C T H   S C T H   S C T H</td>
</tr>
<tr>
<td>DM</td>
<td>DM pin</td>
<td>Yes</td>
<td>S C T H   S C T H   S C T H   S C T H</td>
</tr>
<tr>
<td>Controller Features</td>
<td>ECC</td>
<td>Yes</td>
<td>S C T H   S C T H   S C T H   S C T H</td>
</tr>
<tr>
<td></td>
<td>Reordering</td>
<td>Yes</td>
<td>S C T H   S C T H   S C T H   S C T H</td>
</tr>
</tbody>
</table>

**Note:** LRDIMM memory format is not supported for Intel Stratix 10 FPGA EMIF IP DDR3.
<table>
<thead>
<tr>
<th>Feature Category</th>
<th>Sub-Category</th>
<th>Supported?</th>
<th>EMIF IP Feature Support Level by Intel Stratix 10 Device Grades</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>GX</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>S C T H</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>S C T H</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>S C T H</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>S C T H</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>C T H</td>
</tr>
</tbody>
</table>

Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support

### Table 20. QDR-IV and QDR II/II+/Xtreme EMIF IP Speed and Support Levels for Intel Stratix 10 GX, SX, MX, and TX Devices

<table>
<thead>
<tr>
<th>Protocol</th>
<th>Maximum Rate (Mbps/MHz)</th>
<th>EMIF IP Support Level by Intel Stratix 10 Device Grades</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>-1</td>
<td>-2</td>
</tr>
<tr>
<td>QDR-IV</td>
<td>2133/1066</td>
<td>2133/1066</td>
</tr>
<tr>
<td>QDR II+ Xtreme</td>
<td>1266/633</td>
<td>1100/550</td>
</tr>
<tr>
<td>BL=4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>QDR II+ Xtreme</td>
<td>900/450</td>
<td>800/400</td>
</tr>
<tr>
<td>BL=2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>QDR II+</td>
<td>1100/550</td>
<td>1000/500</td>
</tr>
<tr>
<td>BL=4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>QDR II+</td>
<td>800/400</td>
<td>700/350</td>
</tr>
<tr>
<td>BL=2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>QDR II</td>
<td>700/350</td>
<td>700/350</td>
</tr>
<tr>
<td>BL=4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>QDR II</td>
<td>600/300</td>
<td>600/300</td>
</tr>
<tr>
<td>BL=2</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support
Table 21. QDR-IV EMIF IP Feature Support for Intel Stratix 10 GX, SX, MX, and TX Devices

<table>
<thead>
<tr>
<th>Feature Category</th>
<th>Sub-Category</th>
<th>Supported?</th>
<th>EMIF IP Feature Support Level by Intel Stratix 10 Device Grades</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>GX</td>
</tr>
<tr>
<td>Memory Format</td>
<td>Component</td>
<td>Yes</td>
<td>S C T H</td>
</tr>
<tr>
<td>Memory Type</td>
<td>XP</td>
<td>Yes</td>
<td>S C T H</td>
</tr>
<tr>
<td>Interface Width</td>
<td>&lt;=72 with DIMM</td>
<td>Yes</td>
<td>S C T H</td>
</tr>
<tr>
<td>Controller</td>
<td>Soft controller</td>
<td>Yes</td>
<td>S C T H</td>
</tr>
<tr>
<td>PHY</td>
<td>Hard PHY</td>
<td>Yes</td>
<td>S C T H</td>
</tr>
<tr>
<td>Design Example</td>
<td></td>
<td>Yes</td>
<td>S C T H</td>
</tr>
<tr>
<td>Rate (core)</td>
<td>Quarter</td>
<td>Yes</td>
<td>S C T H</td>
</tr>
<tr>
<td>Debug</td>
<td>EMIF Toolkit</td>
<td>Yes</td>
<td>C T H</td>
</tr>
</tbody>
</table>

Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support

Table 22. QDR II/II+/Xtreme EMIF IP Feature Support for Intel Stratix 10 GX, SX, MX, and TX Devices

<table>
<thead>
<tr>
<th>Feature Category</th>
<th>Sub-Category</th>
<th>Supported?</th>
<th>EMIF IP Feature Support Level by Intel Stratix 10 Device Grades</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>GX</td>
</tr>
<tr>
<td>Memory Format</td>
<td>Component</td>
<td>Yes</td>
<td>S C T H</td>
</tr>
<tr>
<td>Interface Width</td>
<td>&lt;=72 with DIMM</td>
<td>Yes</td>
<td>S C T H</td>
</tr>
<tr>
<td>PHY</td>
<td>Hard PHY</td>
<td>Yes</td>
<td>S C T H</td>
</tr>
<tr>
<td>Design Example</td>
<td></td>
<td>Yes</td>
<td>S C T H</td>
</tr>
<tr>
<td>Rate (core)</td>
<td>Half</td>
<td>Yes</td>
<td>S C T H</td>
</tr>
<tr>
<td></td>
<td>Full</td>
<td>Yes</td>
<td>S C T H</td>
</tr>
<tr>
<td>Debug</td>
<td>EMIF Toolkit</td>
<td>Yes</td>
<td>S C T H</td>
</tr>
</tbody>
</table>

Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support
Table 23. **RLDRAM 3 EMIF IP Speed and Support Levels for Intel Stratix 10 GX, SX, MX, and TX Devices**

<table>
<thead>
<tr>
<th>Format</th>
<th>Maximum Rate (Mbps/MHz)</th>
<th>EMIF IP Support Level by Intel Stratix 10 Device Grades</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>-1</td>
<td>-2</td>
</tr>
<tr>
<td>Component</td>
<td>2400/1200</td>
<td>2133/1066</td>
</tr>
</tbody>
</table>

Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support

Table 24. **RLDRAM 3 EMIF IP Feature Support for Intel Stratix 10 GX, SX, MX, and TX Devices**

<table>
<thead>
<tr>
<th>Feature Category</th>
<th>Sub-Category</th>
<th>Supported?</th>
<th>EMIF IP Feature Support Level by Intel Stratix 10 Device Grades</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interface Width</td>
<td>&lt;=72 with DIMM</td>
<td>Yes</td>
<td>S C T H</td>
</tr>
<tr>
<td>Controller</td>
<td>No</td>
<td></td>
<td>–</td>
</tr>
<tr>
<td>PHY</td>
<td>Hard PHY only</td>
<td>Yes</td>
<td>S C T H</td>
</tr>
<tr>
<td>Design Example</td>
<td>Yes</td>
<td></td>
<td>S C T H</td>
</tr>
<tr>
<td>Rate (core)</td>
<td>Quarter</td>
<td>Yes</td>
<td>S C T H</td>
</tr>
<tr>
<td>DM</td>
<td>DM pins</td>
<td>Yes</td>
<td>S C T H</td>
</tr>
<tr>
<td>Debug</td>
<td>EMIF Toolkit</td>
<td>Yes</td>
<td>C T H</td>
</tr>
</tbody>
</table>

Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support

Table 25. **EMIF IP Debug Support**

<table>
<thead>
<tr>
<th>Feature</th>
<th>Supported?</th>
</tr>
</thead>
<tbody>
<tr>
<td>On-chip debug</td>
<td>Yes</td>
</tr>
<tr>
<td>On-chip debug (with soft Nios)</td>
<td>Yes</td>
</tr>
<tr>
<td>EMIF Debug Toolkit</td>
<td></td>
</tr>
<tr>
<td>Calibration margin</td>
<td>Yes</td>
</tr>
<tr>
<td>Traffic Generator 2.0</td>
<td>No</td>
</tr>
<tr>
<td>2D Eye</td>
<td>No</td>
</tr>
<tr>
<td>Driver margining</td>
<td>Yes</td>
</tr>
<tr>
<td>Efficiency monitor</td>
<td>No</td>
</tr>
<tr>
<td>ODT Tuning</td>
<td>Yes</td>
</tr>
<tr>
<td>RDBI + Driver margining</td>
<td>Yes</td>
</tr>
<tr>
<td>Rank support</td>
<td>Yes</td>
</tr>
</tbody>
</table>
**1.6. Intel Stratix 10 External Memory Interface IP 17.1**

**Table 26. v17.1 November 2017**

<table>
<thead>
<tr>
<th>Description</th>
<th>Impact</th>
</tr>
</thead>
</table>

**Related Information**

Intel Quartus Prime Design Suite Release Notes