Clock Control Intel Stratix 10 FPGA IP Core Release Notes .................................................. 3
Clock Control Intel Stratix 10 FPGA IP v18.0 ................................................................. 3
Stratix 10 Clock Control v17.1 ................................................................................... 3
Clock Control Intel Stratix 10 FPGA IP Core Release Notes

If a release note is not available for a specific IP core version, the IP core has no changes in that version. Information on the latest update releases is in the Intel Quartus Prime Design Suite Update Release Notes.

Related Information
Intel Quartus Prime Design Suite Update Release Notes

Clock Control Intel Stratix 10 FPGA IP v18.0

Table 1. v18.0 May 2018

<table>
<thead>
<tr>
<th>Description</th>
<th>Impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>Renamed Stratix 10 Clock Control IP core to Clock Control Intel Stratix 10 FPGA IP core as per Intel rebranding.</td>
<td>—</td>
</tr>
<tr>
<td>Renamed ‘falling edge’ mode to ‘negative latch’ mode.</td>
<td>—</td>
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</tbody>
</table>

Related Information
• Introduction to Intel FPGA IP Cores
• Intel® Stratix® 10 Clocking and PLL User Guide
• Errata for other IP cores in the Knowledge Base

Stratix 10 Clock Control v17.1

Table 2. v17.1 November 2017

<table>
<thead>
<tr>
<th>Description</th>
<th>Impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>Initial release for Intel Stratix 10 devices.</td>
<td>—</td>
</tr>
</tbody>
</table>

Related Information
• Introduction to Intel FPGA IP Cores
• Intel Stratix 10 Clocking and PLL User Guide
• Errata for other IP cores in the Knowledge Base