Temperature Sensor Intel® Stratix® 10 FPGA IP Release Notes........................................3
Temperature Sensor Intel® Stratix® 10 FPGA IP v18.0.................................................. 3
Intel FPGA S10 Temperature Sensor IP Core v17.1.......................................................... 3
Temperature Sensor Intel® Stratix® 10 FPGA IP Release Notes

If a release note is not available for a specific IP core version, the IP core has no changes in that version. Information on the latest update releases is in the Intel Quartus Prime Design Suite Update Release Notes.

Related Information
Intel Quartus Prime Design Suite Update Release Notes

Temperature Sensor Intel® Stratix® 10 FPGA IP v18.0

Table 1. v18.0 May 2018

<table>
<thead>
<tr>
<th>Description</th>
<th>Impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>Renamed the IP core from &quot;Intel® FPGA S10 Temperature Sensor&quot; to &quot;Temperature Sensor Intel Stratix® 10 FPGA IP&quot;.</td>
<td>—</td>
</tr>
<tr>
<td>Added support for sampling the internal temperature sensing diodes (TSDs) in the high-bandwidth DRAM memory (HBM2) stacks.</td>
<td>The <code>cmd_data</code> signal is now 9-bits width.</td>
</tr>
<tr>
<td>Added response value to the <code>rsp_data</code> signal to indicate invalid data.</td>
<td>0x80000000 indicates invalid data.</td>
</tr>
</tbody>
</table>

Related Information
- Introduction to Intel FPGA IP Cores
- Intel Stratix 10 Analog to Digital Converter User Guide
- Errata for other IP cores in the Knowledge Base

Intel FPGA S10 Temperature Sensor IP Core v17.1

Table 2. v17.1 November 2017

<table>
<thead>
<tr>
<th>Description</th>
<th>Impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>Initial release. This IP is available for Intel Stratix 10 devices only.</td>
<td>—</td>
</tr>
</tbody>
</table>

Related Information
- Introduction to Intel FPGA IP Cores
- Intel Stratix 10 Analog to Digital Converter User Guide
- Errata for other IP cores in the Knowledge Base

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