RapidIO II Intel® FPGA IP Release Notes

Attention: The RapidIO II Intel FPGA IP is part of a product obsolescence and support discontinuation schedule.

For the schedule, refer to the Product Discontinuation Notice PDN2025.

For new designs, Intel recommends that you use other IPs with equivalent functions. To see a list of available IPs, refer to the Intel® FPGA IP Portfolio web page.

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1. RapidIO II Intel® FPGA IP Release Notes

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the *Intel® Quartus® Prime Design Suite Update Release Notes*.

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

The IP version (X.Y.Z) number may change from one Intel Quartus Prime software version to another. A change in:

- X indicates a major revision of the IP. If you update your Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Related Information

- Intel Quartus Prime Design Suite Update Release Notes
- Introduction to Intel FPGA IP Cores
- RapidIO II Intel FPGA IP User Guide
- Errata for the RapidIO II Intel FPGA IP in the Knowledge Base

1.1. RapidIO II IP v19.2.0

Table 1. v19.2.0 2020.09.28

Intel Quartus Prime Version	Description	Impact
20.3	Discontinued support for RapidIO II Intel FPGA IP.	There is no further development or customer support for this IP starting from next Intel Quartus Prime software version.

1.2. RapidIO II Intel FPGA IP v18.0

Table 2. Version 18.0 May 2018

Description	Impact	Note
Renamed RapidIO II IP core to RapidIO II Intel FPGA IP as per Intel rebranding.	—	—
Intel Cyclone® 10 GX devices are now supported in the 18.0 Intel Quartus Prime Pro Edition software.	—	—
Added support for Cadence Xcelium* Parallel simulator.	—	—

Related Information

- RapidIO II Intel FPGA IP User Guide
- Errata for RapidIO II Intel FPGA IP in the Knowledge Base

1.3. RapidIO II IP Core v17.1

Table 3. Version 17.1 November 2017

Description	Impact	Note
Intel Stratix® 10 devices are now supported in the 17.1 Intel Quartus Prime software.	—	—
Added new parameter **Transceiver Tile**.	—	—
Added support for Cadence NCSim simulator.	—	—

Related Information

RapidIO II IP Core User Guide

1.4. RapidIO II IP Core v15.1

Table 4. Version 15.1 November 2015

Description	Impact	Note
The RapidIO II IP core no longer supports 6.25 Gbaud, Avalon-ST pass-through variations that target the Arria V family on any -5 speed grade device.	You must target a different Arria V device for these variations.	—
If you connect your RapidIO II IP core to an Altera Transceiver PHY Reset Controller, added the requirement to set the **RX_PER_CHANNEL** parameter of the reset controller to the value of 1.	—	—

Related Information

- RapidIO II MegaCore Function User Guide
- Errata for RapidIO II IP core in the Knowledge Base

1.5. RapidIO II IP Core v14.1

Table 5. Version 14.1 December 2014

Description	Impact	Note
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade, but does not clarify the reason.	You must ensure that you specify a device for your v14.0 Arria 10 Edition IP core variation and regenerate it in the Quartus II software v14.1.	—
Added `io_error_response_set` input port. The IP core sets the `IO_ERROR_RSP` field in bit [31] of the `Logical/Transport Layer Error Detect CSR` at offset 0x308 when this signal changes value from 0 to 1.	If you upgrade the RapidIO II IP core in your design to the IP core v14.1, you must reconnect the IP core in your design so the new input signal does not float.	—
Changed behavior of individual baud rate _ENABLE and _SUPPORT fields of Port 0 Control 2 CSR at offset 0x154. Instead of all being set to the value of 1, now the _SUPPORT fields for baud rates less than or equal to the value of the **Maximum baud rate** parameter have the value of 1, and the _SUPPORT fields for baud rates greater than the value of the **Maximum baud rate** parameter have the value of 0. Instead of all being set to the value of 1, now the _ENABLE field for the baud rate at which the IP core is operating has the value of 1, and the _ENABLE fields for all other baud rates have the value of 0.	If you upgrade the RapidIO II IP core in your design to the IP core v14.1, the Port 0 Control 2 CSR fields are set as expected to indicate the supported and enabled baud rates.	To modify the IP core to run at a different baud rate than the **Maximum baud rate** value, you must turn on **Enable transceiver dynamic reconfiguration** in the parameter editor, and user logic must reconfigure the transceiver to the new baud rate. As indicated by the values of the Port 0 Control 2 CSR fields, you can only reconfigure the IP core to a baud rate equal or slower than the **Maximum baud rate** value.
Made changes to `Port 0 Control CSR` at offset 0x15C: • Added new field `PORT_ERR_IRQ_EN` that controls whether an interrupt is generated when an error is flagged in the `Port 0 Error Detect` register at offset 0x340. The new field is in bit [6] of the `Port 0 Control CSR`. • Moved `DIS_DEST_ID_CHK` field from bit [7] to bit [8]. • Moved `LOG_TRANS_ERR_IRQ_EN` field from bit [6] to bit [7].	If you upgrade the RapidIO II IP core in your design to the IP core v14.1, your IP core implements the new behavior. You can use the new register field to force an interrupt in this case.	—

Related Information

- RapidIO II MegaCore Function User Guide
- Errata for RapidIO II IP core in the Knowledge Base

1.6. RapidIO II IP Core v14.0 Arria 10 Edition

Table 6. Version 14.0 Arria 10 Edition August 2014

Description	Impact	Note
Verified in the Quartus II software v14.0 Arria 10 Edition. (Added support for Arria 10 devices).	Upgrading your existing IP core from a previous release of the Quartus II software requires migrating it to the Arria 10 device family. To migrate your IP core to the Arria 10 device family, you must regenerate the IP core manually in the Quartus II v14.0 Arria 10 Edition software and reconnect it in your design.	
Arria 10 variations require that you instantiate and connect a TX transceiver PLL IP core in your design.	Upgrading your existing IP core from a previous release of the Quartus II software requires migrating it to the Arria 10 device family. To migrate your IP core to the Arria 10 device family, you must regenerate the IP core manually in the Quartus II v14.0 Arria 10 Edition software and reconnect it in your design.	The new interface signals are listed in the RapidIO II IP Core Signal Changes table.
Arria 10 variations do not require that you instantiate and connect a dynamic reconfiguration controller. Instead, if you turn on the new parameter **Enable transceiver dynamic reconfiguration**, these variations have an internal reconfiguration controller that the user accesses through an Avalon-MM interface.	Upgrading your existing IP core from a previous release of the Quartus II software requires migrating it to the Arria 10 device family. To migrate your IP core to the Arria 10 device family, you must regenerate the IP core manually in the Quartus II v14.0 Arria 10 Edition software and reconnect it in your design.	The new interface signals are listed in the RapidIO II IP Core Signal Changes table.

Table 7. RapidIO II IP Core Signal Changes

Signals added or modified in version 14.0 Arria 10 Edition.

Old Signal Name	New Signal Name	Notes
—	tx_bonded_clocks_ch<n>[5:0]	New interface to external TX PLL. Relevant for Arria 10 variations only. Individual transceiver channel clock signals. One signal (_ch<n>) for each RapidIO lane <n>.
—	reconfig_clk_ch<n>	New Arria 10 transceiver reconfiguration interface. This interface is available if you turn on **Enable transceiver dynamic reconfiguration** in the RapidIO II parameter editor. Relevant for Arria 10 variations only. One signal (_ch<n>) for each RapidIO lane <n>.
—	reconfig_reset_ch<n>	
—	reconfig_read_ch<n>	
—	reconfig_write_ch<n>	
—	reconfig_address_ch<n>[9:0]	
—	reconfig_readdata_ch<n>[31:0]	
—	reconfig_waitrequest_ch<n>	
—	reconfig_writedata_ch<n>[31:0]	
reconfig_to_xcvr	Not present in Arria 10 variations.	Transceiver reconfiguration interface signals for specific non-Arria 10 device families (as supported in past and future versions of the Quartus II software). These signals are not present in Arria 10 variations.
reconfig_from_xcvr	Not present in Arria 10 variations.	
pll_locked	Not present in Arria 10 variations.	
pll_powerdown	Not present in Arria 10 variations.	

Related Information

- RapidIO II MegaCore Function User Guide
- Errata for RapidIO II IP core in the Knowledge Base

1.7. RapidIO II IP Core v14.0

Table 8. Version 14.0 June 2014

Description	Impact	Note
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	This change is optional for v13.1 IP cores. However, IP upgrade is required for IP cores v13.0 and earlier.	
In case of MAINTENANCE Response with Error status, the ADDRESS field of the `Logical/Transport Layer Address Capture` CSR captures the `config_offset` value from the original request.	None. This change is optional. If you do not upgrade your IP core, it does not have this new feature.	
Added new allowed value IMPLEMENTATION SPECIFIC for `INFO_TYPE` field of `Port 0 Attributes Capture` CSR.	None. This change is optional. If you do not upgrade your IP core, it does not have this new feature.	

Related Information

- Introduction to Altera IP Cores
- RapidIO II MegaCore Function User Guide
- Errata for RapidIO II IP core in the Knowledge Base

1.8. RapidIO II IP Core v13.1

Table 9. Version 13.1 November 2013

Description	Impact	Note
Verified in the Quartus II software v13.1.		

Related Information

- RapidIO II MegaCore Function User Guide
- Errata for RapidIO II IP core in the Knowledge Base

1.9. RapidIO II IP Core v13.0

Table 10. Version 13.0 May 2013

Description	Impact	Note
Verified in the Quartus II software v13.0.		

Related Information

- RapidIO II MegaCore Function User Guide
- Errata for RapidIO II IP core in the Knowledge Base

1.10. RapidIO II IP Core User Guide Archives

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.
If an IP core version is not listed, the user guide for the previous IP core version applies.

IP Core Version	User Guide
18.0	RapidIO II Intel FPGA IP Core User Guide
17.1	RapidIO II IP Core User Guide
17.0	RapidIO II IP Core User Guide
16.1	RapidIO II IP Core User Guide 16.1
16.0	RapidIO II IP Core User Guide 16.0
15.0	RapidIO II MegaCore Function User Guide 15.0
14.0	RapidIO II MegaCore Function User Guide 14.0