P-Tile IP for PCI Express IP Core
Release Notes

Updated for Intel® Quartus® Prime Design Suite: 19.3
IP Version: 1.0.0
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1. P-Tile IP for PCI Express IP Core Release Notes

1.1. P-Tile IP for PCI Express IP Cores v19.3

Table 1. 19.3 September 2019

<table>
<thead>
<tr>
<th>Description</th>
<th>Impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>Initial release of the P-Tile Avalon®-MM IP for PCI Express. This IP supports both Intel® Stratix® 10 DX and Intel Agilex™ devices.</td>
<td>Added this new IP component to enable Avalon-MM support for P-Tile in the Gen3 x16 for Endpoint configuration. The support level is Advance. Other configurations may be supported in a future release of Intel Quartus® Prime.</td>
</tr>
<tr>
<td>The P-Tile Avalon-MM IP for PCI Express includes internal Read Data Mover and Write Data Mover to support DMA operations.</td>
<td>This IP includes Data Mover interfaces to communicate with an external DMA Controller. The Intel Quartus Prime 19.3 release includes a PCIe DMA design example, which provides a DMA Controller that can interface with the internal Data Movers of the P-Tile Avalon-MM IP for PCI Express to perform DMA operations. Alternatively, you can build your custom DMA Controller in your application logic.</td>
</tr>
<tr>
<td>Added support for the Debug Toolkit for both P-Tile Avalon-MM and P-Tile Avalon-ST IPs for PCI Express.</td>
<td>The P-Tile Debug Toolkit is a System Console-based tool that provides real-time control, monitoring and debugging of the PCIe links at the Physical Layer.</td>
</tr>
<tr>
<td>Clocking topologies with Separate Reference Clock architectures are supported in this release.</td>
<td>P-Tile IPs for PCI Express support the Separate Reference Clock with no Spread Spectrum Clocking (SRNS) architecture by default, and the Separate Reference Clock with Independent Spread Spectrum (SRIS) Clocking architecture, which can be enabled from the IP Parameter Editor.</td>
</tr>
<tr>
<td>The P-Tile Avalon-MM IP for PCI Express does not support the Interrupt Interface, Error Interface and Configuration Intercept Interface in this release.</td>
<td>The P-Tile Avalon-ST IP for PCI Express does support these interfaces. The P-Tile Avalon-MM IP for PCI Express may support these interfaces in a future release of Intel Quartus Prime.</td>
</tr>
<tr>
<td>The P-Tile Avalon-MM IP for PCI Express does not support example design simulation in this release.</td>
<td>The P-Tile Avalon-ST IP for PCI Express does support example design simulation. The P-Tile Avalon-MM IP for PCI Express may support example design simulation in a future release of Intel Quartus Prime. You can still simulate the P-Tile Avalon-MM IP for PCI Express by using a third-party Bus Functional Model (BFM).</td>
</tr>
</tbody>
</table>

Related Information

- P-Tile Avalon Streaming (ST) IP for PCI Express User Guide
  For the Avalon-ST Interface to the Application Layer.
- Errata for the Hard IP for PCI Express IP Core in the Knowledge Base
- Introduction to Intel FPGA IP Cores
  Provides general information about all Intel FPGA IP cores, including parameterizing, generating, upgrading, and simulating IP cores.
### 1.2. P-Tile IP for PCI Express IP Cores v19.2

#### Table 2. 19.2 June 2019

<table>
<thead>
<tr>
<th>Description</th>
<th>Impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>Initial release of the P-Tile Avalon-ST IP for PCI Express. This IP supports both Intel Stratix 10 DX and Intel Agilex devices.</td>
<td>Added this new IP component to enable Avalon-ST native support for P-Tile in the Gen3 x16/x8 for Endpoint, Gen4 x16/x8 for Endpoint, Gen3 x16/x4 for Root Port and Gen4 x16/x4 for Root Port configurations. The support level is Advance. Other configurations can be supported through link negotiations.</td>
</tr>
<tr>
<td>Support for Single-Root I/O Virtualization (SR-IOV) is available.</td>
<td>The P-Tile Avalon-ST IP for PCI Express supports up to 8 physical functions (PFs) and 2048 virtual functions (VFs) in SR-IOV mode.</td>
</tr>
<tr>
<td>Port bifurcation is supported.</td>
<td>This IP can support one x16 or two x8 interfaces in Endpoint mode, and four x4 interfaces in Root Port mode.</td>
</tr>
</tbody>
</table>
| TLP Bypass mode is supported.                                              | This IP supports a TLP Bypass mode for both upstream and downstream ports, thus allowing the implementation of advanced features such as:  
  • The upstream port or downstream port of a switch.  
  • A custom implementation of a Transaction Layer to meet specific user requirements. |

### 1.3. User Guide Archives

If an IP core version is not listed, the user guide for the previous IP core version applies.

<table>
<thead>
<tr>
<th>Quartus Version</th>
<th>User Guide</th>
</tr>
</thead>
<tbody>
<tr>
<td>19.2</td>
<td>P-Tile Avalon Streaming (Avalon-ST) IP for PCI Express User Guide</td>
</tr>
</tbody>
</table>