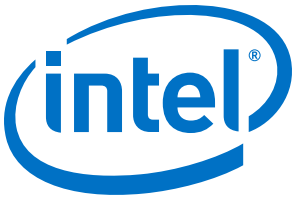

# Other IP Cores Release Notes

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# Contents

# 1. Other IP Cores Release Notes

## 1.1. Altera Arria 10 Unique Chip ID IP Core v16.0

### Table 1. v16.0 May 2016

| Description | Impact |
|---|---|
| Initial release. Only supports Arria 10 device family. | - |

#### Related Information

- Introduction to Altera IP Cores
- Altera Arria 10 Unique Chip ID IP Core User Guide
- Errata for other IP cores in the Knowledge Base

## 1.2. ASMI Parallel Intel FPGA IP Core v18.0

### Table 2. v18.0 May 2018

| Description | Impact |
|---|---|
| Renamed Altera ASMI Parallel IP core to ASMI Parallel Intel® FPGA IP core as per Intel rebranding. | — |

#### Related Information

- Introduction to Intel FPGA IP Cores
- ASMI Parallel Intel FPGA IP Core User Guide

## 1.3. Intel FPGA Advanced SEU Detection IP Core v17.1

### Table 3. v17.1 November 2017

| Description | Impact |
|---|---|
| Renamed Altera Advanced SEU Detection IP core to Intel FPGA Advanced SEU Detection IP core as per Intel rebranding. | — |
| Added support for Intel Cyclone® 10 GX devices. | — |

#### Related Information

- Introduction to Intel FPGA IP Cores
- Intel FPGA Advanced SEU Detection IP Core User Guide
- Errata for other IP cores in the Knowledge Base

## 1.4. Altera Advanced SEU Detection IP Core v14.1

### Table 4. v14.1 December 2014

| Description | Impact |
|---|---|
| Added support for double-adjacent SEU sensitivity processing. | Initiates an .smh lookup for correctable double-adjacent EDCRC errors instead of identifying such SEU as critical. |
| Added `critical_clear` signal to `errors` interface | - |
| Added `busy` signal to `errors` interface | For on-chip processing configuration only. |

#### Related Information

- Advanced SEU Detection IP Core User Guide
- Errata for other IP cores in the Knowledge Base

## 1.5. Altera Dual Configuration v14.0 Update 2

### Table 5. v14.0 Update 2 September 2014

| Description | Impact |
|---|---|
| Initial release. | - |

#### Related Information

- MAX 10 FPGA Configuration User Guide
- Errata for other IP cores in the Knowledge Base

## 1.6. Altera CRC Error Verify IP Core v16.0

### Table 6. v16.0 May 2016

| Description | Impact |
|---|---|
| Improved design to filter intermittent multiple leaky data line | - |

#### Related Information

- Introduction to Altera IP Cores
- Errata for other IP cores in the Knowledge Base

## 1.7. Altera Error Message Register Unloader IP Core v16.0

### Table 7. v16.0 May 2016

| Description | Impact |
|---|---|
| Major update for this IP core. This IP core is not backward compatible to Intel Quartus® Prime prior to version 16.0. | You are required to instantiate the IP core in Intel Quartus Prime version 16.0. |

### Related Information

- Introduction to Altera IP Cores
- Altera Error Message Register Unloader IP Core User Guide
- Errata for other IP cores in the Knowledge Base

## 1.8. Altera EMR Unloader IP Core v14.1

### Table 8. v14.1 December 2014

| Description | Impact |
|---|---|
| Fixed an issue with synchronization the of CRCERROR signal, which comes from the EDCRC circuitry that the internal oscillator drives. | - |

### Related Information

- Advanced SEU Detection IP Core User Guide
- Errata for other IP cores in the Knowledge Base

## 1.9. ALTERA_FP_FUNCTIONS v15.0

### Table 9. v15.0 May 2015

| Description | Impact |
|---|---|
| Added new functions: Multiply Add, Multiply Accumulate, Accumulate, and Scalar Product.. | - |
| Added support for range reduction option for appropriate trigonometric functions. | - |
| Added **Manually Specify DSP Registers** option on the **Performance** tab that shows a GUI and allows you to target specific registers on Arria 10 devices. applies to Add, Subtract, Multiply Add functions | - |
| Added target option on the **Performance** tab to allow you to constrain both latency and frequency | - |

### Related Information

- Floating-Point Megafunctions User Guide
- Errata for other IP cores in the Knowledge Base

## 1.10. ALTERA_FP_MATRIX_MULT v14.1

### Table 10. v14.1 December 2014

| Description | Impact |
|---|---|
| Added support for Arria 10 device hard floating-point blocks. | Only for new IP cores. |
| Changed reset port. It is no longer optional and is always present | |
| Removed option to add an enable port | |

*continued...*

| Description | Impact |
|---|---|
| Changed performance. Specify twice the number of memory blocks compared to previous version for the equivalent performance | |
| Changed the signals to use Avalon-ST interfaces. | Only for new IP cores. Any existing IP cores continue to have the same signals even when you edit and regenerate the IP core. |
| Changed `reset` to active low | |

### Related Information

- Floating-Point Megafunctions User Guide
- Errata for other IP cores in the Knowledge Base

## 1.11. GPIO Intel FPGA IP v18.0

### Table 11. v18.0 May 2018

| Description | Impact |
|---|---|
| Renamed the IP core from "Intel FPGA GPIO" to "GPIO Intel FPGA IP". | — |

### Related Information

- Introduction to Intel FPGA IP Cores
- Intel Stratix® 10 General Purpose I/O User Guide
- GPIO Intel FPGA IP User Guide
- Errata for other IP cores in the Knowledge Base

## 1.12. Intel FPGA GPIO IP Core v17.1

### Table 12. v17.1 November 2017

| Description | Impact |
|---|---|
| Added support for Intel Stratix® 10 devices. | — |
| Renamed Altera GPIO IP core to Intel FPGA GPIO IP core as per Intel rebranding. | — |

### Related Information

- Introduction to Altera IP Cores
- Intel Stratix 10 General Purpose I/O User Guide
- Intel FPGA GPIO IP Core User Guide
- Errata for other IP cores in the Knowledge Base

## 1.13. Altera GPIO IP Core v14.0 Arria 10 Edition

### Table 13. v14.0 Arria 10 Edition August 2014

| Description | Impact |
|---|---|
| Changed signal names | - |

### Table 14. Signal Name Changes

| Old Name | New Name | Notes |
|---|---|---|
| core_ck_fr_in_export | ck_fr_in | |
| core_ck_fr_out_export | ch_fr_out | |
| core_ck_hr_in_export | ch_hr_in | |
| core_ck_hr_out_export | ch_hr_out | |
| core_dout_export | dout | |
| core_din_export | din | |
| core_oe_export | oe | |
| core_pad_io_export | pad_io | |
| core_pad_io_b_export | pad_io_b | |
| core_aclr_export | aclr | |
| core_sclr_export | sclr | |
| core_cke_export | cke | |
| core_ck_export | ck | |
| core_ck_in_export | ck_in | |
| core_ck_out_export | ck_out | |
| core_ck_fr_export | ck_fr | |
| core_ck_hr_export | ck_hr | |
| core_pad_in_export | pad_in | |
| core_pad_in_b_export | pad_in_b | |
| core_pad_out_export | pad_out | |
| core_pad_out_b_export | pad_out_b | |
| core_aset_export | aset | |
| core_sset_export | sset | |

#### Related Information

- Altera GPIO Megafunction User Guide
- Errata for other IP cores in the Knowledge Base

## 1.14. Altera GPIO Lite IP Core v14.0 Update 2

### Table 15. v14.0 Update 2 September 2014

| Description | Impact |
|---|---|
| Initial release. | |

#### Related Information

- MAX 10 General Purpose I/O User Guide

- Errata for other IP cores in the Knowledge Base

## 1.15. LVDS SERDES Intel FPGA IP v18.0

### Table 16. v18.0 May 2018

| Description | Impact |
|---|---|
| Renamed the IP core from "Intel FPGA LVDS SERDES" to "LVDS SERDES Intel FPGA IP". | - |

### Related Information

- Introduction to Intel FPGA IP Cores
- Intel Stratix 10 High-Speed LVDS I/O User Guide
- LVDS SERDES Intel FPGA IP User Guide
- Errata for other IP cores in the Knowledge Base

## 1.16. Intel FPGA LVDS SERDES IP Core v17.1

### Table 17. v17.1 November 2017

| Description | Impact |
|---|---|
| Added support for Intel Stratix 10 devices:<br>• Duplex feature to allow transmitter and receiver channels in the same I/O bank<br>• Clock phase alignment (CPA) block for improved timing closure between the periphery and the core | — |
| Renamed Altera LVDS SERDES IP core to Intel FPGA LVDS SERDES IP core as per Intel rebranding. | — |

### Related Information

- Introduction to Altera IP Cores
- Intel Stratix 10 High-Speed LVDS I/O User Guide
- Intel FPGA LVDS SERDES IP Core User Guide
- Errata for other IP cores in the Knowledge Base

## 1.17. Altera LVDS SERDES IP Core v17.0

### Table 18. v17.0 May 2017

| Description | Impact |
|---|---|
| Added support for Intel Cyclone 10 GX devices. | - |

### Related Information

- Introduction to Altera IP Cores
- Altera LVDS SERDES IP Core User Guide
- Errata for other IP cores in the Knowledge Base

## 1.18. Altera LVDS SERDES IP Core v14.1

### Table 19. v14.1 December 2014

| Description | Impact |
|---|---|
| Added internal PLL additional clock export parameter | - |

#### Related Information

- Altera LVDS SERDES Megafunction User Guide
- Errata for other IP cores in the Knowledge Base

## 1.19. Altera LVDS SERDES IP Core v14.0 Arria 10 Edition

### Table 20. v14.0 Arria 10 Edition August 2014

| Description | Impact |
|---|---|
| Added feature that creates `.sdc` file for generated designs (previously only for example designs) | - |
| Added support for external PLL mode | - |
| Added option to clock TX core registers using reference clock | - |

#### Related Information

- Altera LVDS SERDES Megafunction User Guide
- Errata for other IP cores in the Knowledge Base

## 1.20. Clock Control Block (ALTCLKCTRL) IP Core v17.0

### Table 21. v17.0 May 2017

| Description | Impact |
|---|---|
| Added support for Intel Cyclone 10 LP and Intel Cyclone 10 GX devices. | — |

#### Related Information

- Introduction to Intel FPGA IP Cores
- Clock Control Block (ALTCLKCTRL) IP Core User Guide
- Errata for other IP cores in the Knowledge Base

## 1.21. ALTDDIO_IN, ALTDDIO_OUT, and ALTDDIO_BIDIR IP Cores v17.0

### Table 22. v17.0 May 2017

| Description | Impact |
|---|---|
| Added support for Intel Cyclone 10 LP devices. | — |

#### Related Information

- Introduction to Intel FPGA IP Cores

- Double Data Rate I/O (ALTDDIO_IN, ALTDDIO_OUT, and ALTDDIO_BIDIR) IP Cores User Guide
- Errata for other IP cores in the Knowledge Base

## 1.22. ALTIOBUF IP Core v17.0

### Table 23. v17.0 May 2017

| Description | Impact |
|---|---|
| Added support for Intel Cyclone 10 LP devices. | — |

### Related Information

- Introduction to Intel FPGA IP Cores
- I/O Buffer (ALTIOBUF) IP Core User Guide
- Errata for other IP cores in the Knowledge Base

## 1.23. ALTMULT_ACCUM IP Core v17.0

### Table 24. v17.0 May 2017

| Description | Impact |
|---|---|
| Added support for Intel Cyclone 10 LP and Intel Cyclone 10 GX devices. | — |

### Related Information

- Introduction to Intel FPGA IP Cores
- Integer Arithmetic IP Cores User Guide
- Errata for other IP cores in the Knowledge Base

## 1.24. ALTMULT_COMPLEX Intel FPGA IP Core v18.0

### Table 25. v18.0 May 2018

| Description | Impact |
|---|---|
| Renamed ALTMULT_COMPLEX IP core to ALTMULT_COMPLEX Intel FPGA IP core as per Intel rebranding. | — |

### Related Information

- Introduction to Altera IP Cores
- Intel Stratix 10 Variable Precision DSP Blocks User Guide
- Integer Arithmetic IP Cores User Guide
- Errata for other IP cores in the Knowledge Base

## 1.25. ALTMULT_COMPLEX IP Core v17.1

### Table 26. v17.1 November 2017

| Description | Impact |
|---|---|
| Added support for Intel Stratix 10 and Intel Cyclone 10 GX devices. | — |

#### Related Information

- Introduction to Altera IP Cores
- Integer Arithmetic IP Cores User Guide
- Intel Stratix 10 Variable Precision DSP Blocks User Guide
- Errata for other IP cores in the Knowledge Base

## 1.26. ALTMULT_COMPLEX IP Core v17.0

### Table 27. v17.0 May 2017

| Description | Impact |
|---|---|
| Added support for Intel Cyclone 10 LP and Intel Cyclone 10 GX devices. | — |

#### Related Information

- Introduction to Intel FPGA IP Cores
- Integer Arithmetic IP Cores User Guide
- Errata for other IP cores in the Knowledge Base

## 1.27. ALTMULT_COMPLEX IP Core v16.0

### Table 28. v16.0 May 2016

| Description | Impact |
|---|---|
| • Added synchronous clear signal support for output pipeline register for Arria 10 devices.<br>• Replaced **Create an asynchronous Clear input** check box with **Clear Signal Type** drop down box with the values of **NONE**, **ACLR**, and **SCLR** in the IP parameter editor for users selection. This change is only applicable to Arria 10 devices. | — |

#### Related Information

- Introduction to Altera IP Cores
- Integer Arithmetic IP Cores User Guide
- Errata for other IP cores in the Knowledge Base

## 1.28. ALTPLL IP Core v17.0

### Table 29. v17.0 May 2017

| Description | Impact |
|---|---|
| Added support for Intel Cyclone 10 LP devices. | — |

### Related Information

- Introduction to Intel FPGA IP Cores
- ALTPLL (Phase-Locked Loop) IP Core User Guide
- Errata for other IP cores in the Knowledge Base

## 1.29. ALTSQRT IP Core v17.0

### Table 30. v17.0 May 2017

| Description | Impact |
|---|---|
| Added support for Intel Cyclone 10 LP and Intel Cyclone 10 GX devices. | — |

### Related Information

- Introduction to Intel FPGA IP Cores
- Integer Arithmetic IP Cores User Guide
- Errata for other IP cores in the Knowledge Base

## 1.30. Multiply Adder Intel FPGA IP Core v18.0

### Table 31. v18.0 May 2018

| Description | Impact |
|---|---|
| Renamed Intel FPGA Multiply Adder IP core to Multiply Adder Intel FPGA IP core as per Intel rebranding. | — |

### Related Information

- Introduction to Intel FPGA IP Cores
- Intel Stratix 10 Variable Precision DSP Blocks User Guide
- Integer Arithmetic IP Cores User Guide
- Errata for other IP cores in the Knowledge Base

## 1.31. Intel FPGA Multiply Adder v17.1

### Table 32. v17.1 November 2017

| Description | Impact |
|---|---|
| Added support for Intel Stratix 10 and Intel Cyclone 10 GX devices. | — |
| Renamed ALTERA_MULT_ADD IP core to Intel FPGA Multiply Adder IP core as per Intel rebranding. | — |

### Related Information

- Introduction to Intel FPGA IP Cores
- Intel Stratix 10 Variable Precision DSP Blocks User Guide
- Errata for other IP cores in the Knowledge Base

## 1.32. ALTMULT_ADD IP Core v17.0

### Table 33. v17.0 May 2017

| Description | Impact |
|---|---|
| Added support for Intel Cyclone 10 LP and Intel Cyclone 10 GX devices. | — |

### Related Information

- Introduction to Intel FPGA IP Cores
- Integer Arithmetic IP Cores User Guide
- Errata for other IP cores in the Knowledge Base

## 1.33. ALTERA_MULT_ADD IP Core v16.0

### Table 34. v16.0 May 2016

| Description | Impact |
|---|---|
| • Added synchronous clear signal support.<br>• Added **What is the source for synchronous clear input?** selection for the following registers in the GUI:<br>— Output register of the adder unit<br>— Register for `addnsub1` input signal<br>— Register for `addnsub3` input signal<br>— Register for `dataa` input signal<br>— Register for `datab` input signal<br>— Register for `scainouta` output signal<br>— Register for `datac` input signal<br>— Register for `signa` input signal<br>— Register for `signb` input signal<br>— Register for `coefsel[0..3]` input signals<br>— Register for `accum_sload` and `sload_accum` input signals<br>— Register for `negate` input signal<br>— Second register for `signa` and `signb` input signals<br>— Register for systolic delay input signals | — |

### Related Information

- Introduction to Altera IP Cores
- Integer Arithmetic IP Cores User Guide
- Errata for other IP cores in the Knowledge Base

## 1.34. Altera Modular ADC IP Core v14.0 Update 2

### Table 35. v14.0 Update 2 September 2014

| Description | Impact |
|---|---|
| Initial release. | - |

### Related Information

- MAX 10 Analog to Digital Converter User Guide

- Errata for other IP cores in the Knowledge Base

## 1.35. Altera On-Chip Flash IP Core v15.1

### Table 36. v15.1 November 2015

| Description | Impact |
|---|---|
| Added parallel data interface support for 10M02 devices; the maximum frequency is 7.25 MHz. | – |

### Related Information

- Introduction to Altera IP Cores
- MAX 10 User Flash Memory User Guide
- Errata for other IP cores in the Knowledge Base

## 1.36. Altera On-Chip Flash IP Core v14.0 Update 2

### Table 37. v14.0 Update 2 September 2014

| Description | Impact |
|---|---|
| Initial release. | - |

### Related Information

- MAX 10 User Flash Memory User Guide
- Errata for other IP cores in the Knowledge Base

## 1.37. Altera On-Chip Flash IP Core v14.1

### Table 38. v14.1 December 2014

| Description | Impact |
|---|---|
| Added new parameters:<br>• **Data interface** parameter.<br>• **Read burst count** parameter. Adjusts the maximum burst count for Incrementing read mode. Also autoadjusts `burstcount` bus width.<br>• **Serial** data interfaces<br>• **Flash Memory**. Indicates the address mapping for each sector and adjusts the **Access Mode** for each sector individually | - |
| Replaced **Dual Images** parameter with **Configuration Scheme** and **Configuration Mode** parameters which includes all supported configuration modes. Use CFM as UFM during single image configuration mode without memory initialization. | |
| Fixed a bug, which allows you to adjust the **Read burst count** from 1 to 2 or 4 while using **WrappingRead burst mode**. | |

### Related Information

- MAX 10 User Flash Memory User Guide
- Errata for other IP cores in the Knowledge Base

## 1.38. Altera Parallel Flash Loader IP Core v17.0

### Table 39. v17.0 May 2017

| Description | Impact |
|---|---|
| Added support for Intel Cyclone 10 LP and Intel Cyclone 10 GX devices. | — |

#### Related Information

- Introduction to Intel FPGA IP Cores
- Intel FPGA Parallel Flash Loader IP Core User Guide
- Errata for other IP cores in the Knowledge Base

## 1.39. Altera Soft LVDS IP Core v14.0 Update 2

### Table 40. v14.0 Update 2 September 2014

| Description | Impact |
|---|---|
| Initial release. | - |

#### Related Information

- MAX 10 High-Speed LVDS I/O User Guide
- Errata for other IP cores in the Knowledge Base

## 1.40. OCT Intel FPGA IP v18.0

### Table 41. v18.0 May 2018

| Description | Impact |
|---|---|
| Renamed the IP core from "Intel FPGA OCT" to "OCT Intel FPGA IP". | — |

#### Related Information

- Introduction to Intel FPGA IP Cores
- Intel FPGA OCT IP Core User Guide
- Errata for other IP cores in the Knowledge Base

## 1.41. Intel FPGA OCT IP Core v17.1

### Table 42. v17.1 November 2017

| Description | Impact |
|---|---|
| Added support for Intel Stratix 10 devices. | — |
| Renamed Altera OCT IP core to Intel FPGA OCT IP core as per Intel rebranding. | — |

#### Related Information

- Introduction to Intel FPGA IP Cores
- Intel FPGA OCT IP Core User Guide
- Errata for other IP cores in the Knowledge Base

## 1.42. Altera OCT IP Core v14.0 Arria 10 Edition

### Table 43. v14.0 Arria 10 Edition August 2014

| Description | Impact |
|---|---|
| • Changed signal names<br>• Added user mode OCT | |

### Table 44. Signal Name Changes

| Old Name | New Name | Notes |
|---|---|---|
| `core_rzqin_export` | `rzqin` | - |
| `core_series_termination_control_expor r` | `oct_#_series_termination_control` | - |
| `core_parallel_termination_control_ex port` | `oct_#_parallel_termination_control` | - |

#### Related Information

- Altera OCT Megafunction User Guide
- Errata for other IP cores in the Knowledge Base

## 1.43. Altera Remote Update IP Core v17.0

### Table 45. v17.0 May 2017

| Description | Impact |
|---|---|
| Added support for Intel Cyclone 10 LP and Intel Cyclone 10 GX devices. | — |

#### Related Information

- Introduction to Intel FPGA IP Cores
- Altera Remote Update IP Core User Guide
- Errata for other IP cores in the Knowledge Base

## 1.44. Altera Serial Flash Loader IP Core v17.0

### Table 46. v17.0 May 2017

| Description | Impact |
|---|---|
| Added support for Intel Cyclone 10 LP and Intel Cyclone 10 GX devices. | — |

#### Related Information

- Introduction to Intel FPGA IP Cores
- AN 370: Using the Serial Flash Loader with the Intel Quartus Prime Software
- Errata for other IP cores in the Knowledge Base

## 1.45. Intel FPGA Voltage Sensor IP Core v17.1

### Table 47. v17.1 November 2017

| Description | Impact |
|---|---|
| Added support for Intel Cyclone 10 GX devices. | The Intel Cyclone 10 GX devices are only available in the Intel Quartus Prime Pro Edition software. |
| Renamed Altera Voltage Sensor IP core to Intel FPGA Voltage Sensor IP core as per Intel rebranding. | — |

#### Related Information

- Introduction to Intel FPGA IP Cores
- Altera Voltage Sensor IP Core User Guide
- Errata for other IP cores in the Knowledge Base

## 1.46. Altera Voltage Sensor IP Core v15.0

### Table 48. v15.0 May 2015

| Description | Impact |
|---|---|
| Initial release. | - |

#### Related Information

- Altera Voltage Sensor IP Core User Guide
- Errata for other IP cores in the Knowledge Base

## 1.47. FIFO IP Core v17.1

### Table 49. v17.1 November 2017

| Description | Impact |
|---|---|
| Added support for Intel Stratix 10, Intel Cyclone 10 LP, and Intel Cyclone 10 GX devices. | — |

#### Related Information

- Introduction to Altera IP Cores
- SCFIFO and DCFIFO IP Cores User Guide
- Errata for other IP cores in the Knowledge Base

## 1.48. FIFO IP Core v16.0

### Table 50. v16.0 May 2016

| Description | Impact |
|---|---|
| Added ECC support for variable data width for Arria 10 devices. | — |

### Related Information

- Introduction to Altera IP Cores
- SCFIFO and DCFIFO IP Cores User Guide
- Errata for other IP cores in the Knowledge Base

## 1.49. FIFO2 IP Core v17.1

### Table 51. v17.1 November 2017

| Description | Impact |
|---|---|
| Initial release. This IP core is available only in Intel Stratix 10 devices. | — |

### Related Information

- Introduction to Intel FPGA IP Cores
- Intel Stratix 10 Embedded Memory User Guide
- Errata for other IP cores in the Knowledge Base

## 1.50. Intel FPGA Fault Injection IP Core v17.1

### Table 52. v17.1 November 2017

| Description | Impact |
|---|---|
| Renamed Altera Fault Injection IP core to Intel FPGA Fault Injection IP core as per Intel rebranding. | — |
| Added support for Intel Cyclone 10 GX devices. | — |

### Related Information

- Introduction to Intel FPGA IP Cores
- Intel FPGA Fault Injection IP Core User Guide
- Errata for other IP cores in the Knowledge Base

## 1.51. Phase-Locked Loop Reconfiguration (ATLPLL_RECONFIG) IP Core v17.0

### Table 53. v17.0 May 2017

| Description | Impact |
|---|---|
| Added support for Intel Cyclone 10 LP devices. | — |

### Related Information

- Introduction to Intel FPGA IP Cores
- AN 728: I/O PLL Reconfiguration and Dynamic Phase Shift for Intel Arria® 10 Devices
- Errata for other IP cores in the Knowledge Base

## 1.52. Intel FPGA PLL Reconfig v17.1

### Table 54. v17.1 November 2017

| Description | Impact |
|---|---|
| Added support for Intel Cyclone 10 GX devices. | — |

#### Related Information

- Introduction to Intel FPGA IP Cores
- AN 728: I/O PLL Reconfiguration and Dynamic Phase Shift for Intel Arria® 10 Devices
- Errata for other IP cores in the Knowledge Base

## 1.53. Intel FPGA S10 Configuration Clock v17.1

### Table 55. v17.1 November 2017

| Description | Impact |
|---|---|
| Initial release. This IP is available only in Intel Stratix 10 devices. | — |

#### Related Information

- Introduction to Intel FPGA IP Cores
- AN 496: Using the Internal Oscillator IP Core
- Errata for other IP cores in the Knowledge Base

## 1.54. Intel FPGA Temperature Sensor IP Core v17.1

### Table 56. v17.1 November 2017

| Description | Impact |
|---|---|
| Added support for Intel Cyclone 10 GX devices. | The Intel Cyclone 10 GX devices are only available in the Intel Quartus Prime Pro Edition software. |
| Renamed Altera Temperature Sensor IP core to Intel FPGA Temperature Sensor IP core as per Intel rebranding. | — |

#### Related Information

- Introduction to Intel FPGA IP Cores
- Intel FPGA Temperature Sensor IP Core User Guide
- Errata for other IP cores in the Knowledge Base

## 1.55. Internal Oscillator v17.1

### Table 57. v17.1 November 2017

| Description | Impact |
|---|---|
| Added support Intel Cyclone 10 LP and Intel Cyclone 10 GX devices. | — |

### Related Information

- Introduction to Intel FPGA IP Cores
- AN 496: Using the Internal Oscillator IP Core
- Errata for other IP cores in the Knowledge Base

## 1.56. Internal Oscillator IP Core v14.0 Update 2

**Table 58. v14.0 Update 2 September 2014**

| Description | Impact |
|---|---|
| Initial release. | - |

### Related Information

- MAX 10 Clocking and PLL User Guide
- Errata for other IP cores in the Knowledge Base

## 1.57. LPM_ADD_SUB IP Core v17.0

**Table 59. v17.0 May 2017**

| Description | Impact |
|---|---|
| Added support for Intel Cyclone 10 LP devices. | — |

### Related Information

- Introduction to Intel FPGA IP Cores
- Integer Arithmetic IP Cores User Guide
- Errata for other IP cores in the Knowledge Base

## 1.58. LPM_COMPARE IP Core v17.0

**Table 60. v17.0 May 2017**

| Description | Impact |
|---|---|
| Added support for Intel Cyclone 10 LP devices. | — |

### Related Information

- Introduction to Intel FPGA IP Cores
- Integer Arithmetic IP Cores User Guide
- Errata for other IP cores in the Knowledge Base

## 1.59. LPM_COUNTER IP Core v17.0

**Table 61. v17.0 May 2017**

| Description | Impact |
|---|---|
| Added support for Intel Cyclone 10 LP devices. | — |

### Related Information

- Introduction to Intel FPGA IP Cores
- Integer Arithmetic IP Cores User Guide
- Errata for other IP cores in the Knowledge Base

## 1.60. LPM_DIVIDE IP Core v17.0

### Table 62. v17.0 May 2017

| Description | Impact |
|---|---|
| Added support for Intel Cyclone 10 LP devices. | — |

### Related Information

- Introduction to Intel FPGA IP Cores
- Integer Arithmetic IP Cores User Guide
- Errata for other IP cores in the Knowledge Base

## 1.61. LPM_MULT Intel FPGA IP Core v18.0

### Table 63. v18.0 May 2018

| Description | Impact |
|---|---|
| Renamed LPM_MULT IP core to LPM_MULT Intel FPGA IP core as per Intel rebranding. | — |

### Related Information

- Introduction to Intel FPGA IP Cores
- Intel Stratix 10 Variable Precision DSP Blocks User Guide
- Integer Arithmetic IP Cores User Guide
- Errata for other IP cores in the Knowledge Base

## 1.62. LPM_MULT IP Core v17.1

### Table 64. v17.1 November 2017

| Description | Impact |
|---|---|
| Added support for Intel Stratix 10 and Intel Cyclone 10 GX devices. | — |

### Related Information

- Introduction to Intel FPGA IP Cores
- Intel Stratix 10 Variable Precision DSP Blocks User Guide
- Integer Arithmetic IP Cores User Guide
- Errata for other IP cores in the Knowledge Base

## 1.63. LPM_MULT IP Core v17.0

### Table 65. v17.0 May 2017

| Description | Impact |
|---|---|
| Added support for Intel Cyclone 10 LP devices. | — |

#### Related Information

- Introduction to Intel FPGA IP Cores
- Integer Arithmetic IP Cores User Guide
- Errata for other IP cores in the Knowledge Base

## 1.64. LPM_MULT IP Core v16.0

### Table 66. v16.0 May 2016

| Description | Impact |
|---|---|
| • Added synchronous clear signal support for output pipeline register for Arria 10 devices.<br>• Replaced **Create an asynchronous Clear input** checkbox with **Clear Signal Type** drop down box with the values of **NONE**, **ACLR**, and **SCLR** in the IP parameter editor for users selection. This change is only applicable to Arria 10 devices. | — |

#### Related Information

- Introduction to Altera IP Cores
- Integer Arithmetic IP Cores User Guide
- Errata for other IP cores in the Knowledge Base

## 1.65. LPM_SHIFTREG IP Core v17.0

### Table 67. v17.0 May 2017

| Description | Impact |
|---|---|
| Added support for Intel Cyclone 10 LP devices. | — |

#### Related Information

- Introduction to Intel FPGA IP Cores
- LPM_SHIFTREG Megafunction User Guide
- Errata for other IP cores in the Knowledge Base

## 1.66. LVDS SERDES Transmitter/Receiver IP Cores v17.0

### Table 68. v17.0 May 2017

| Description | Impact |
|---|---|
| For the `pll_phasedone` signal, the asynchronous clear has been changed to synchronous clear to avoid hardware glitch. | — |
| Added support for Intel Cyclone 10 LP devices. | — |

### Related Information

- Introduction to Intel FPGA IP Cores
- LVDS SERDES Transmitter/Receiver IP Cores User Guide
- Errata for other IP cores in the Knowledge Base

## 1.67. PARALLEL_ADD IP Core v17.0

### Table 69. v17.0 May 2017

| Description | Impact |
|---|---|
| Added support for Intel Cyclone 10 LP devices. | — |

### Related Information

- Introduction to Intel FPGA IP Cores
- Integer Arithmetic IP Cores User Guide
- Errata for other IP cores in the Knowledge Base

## 1.68. RAM: 2-Port IP Core v17.1

### Table 70. v17.1 November 2017

| Description | Impact |
|---|---|
| Added support for Intel Stratix 10 devices.<br>• Added ECC Parity Flip feature for memory blocks error correction code support. This feature dynamically flip the parity value generated in the encoder of M20K blocks to observe the ECC behavior through simulation.<br>• Added True Dual Ports Dual Clock Emulator feature to emulates a TDP dual clock mode using single clock mode. This feature provides backward compatibility with Intel Arria® 10 devices. | — |

### Related Information

- Introduction to Intel FPGA IP Cores
- Intel Stratix 10 Embedded Memory User Guide
- Errata for other IP cores in the Knowledge Base

## 1.69. RAM: 1-port, RAM: 2-port, ROM: 1-port, and ROM: 2-port IP Cores v17.0

### Table 71. v17.0 May 2017

| Description | Impact |
|---|---|
| Added the **Implement clock-enable circuitry for use in a partial reconfiguration region** parameter for RAM: 1-port and RAM: 2-port IP cores. Turning on this parameter implements the clock-enable circuitry for use in a partial reconfiguration region. | This change is optional. If you do not upgrade your IP core, it does not have this new feature. |
| Added support for Intel Cyclone 10 LP devices. | — |

### Related Information

- Internal Memory (ROM and RAM) User Guide

- Errata for other IP cores in the Knowledge Base

## 1.70. RAM: 2-port v16.0 Arria 10 Edition

### Table 72. v16.0 Arria 10 Edition May 2016

| Description | Impact |
|---|---|
| Added ECC support for variable data width. | - |

### Related Information

- Embedded Memory (RAM and ROM) IP Core User Guide
- Errata for other IP cores in the Knowledge Base

## 1.71. RAM: 1-port and RAM: 2-port v14.0 Arria 10 Edition

### Table 73. v14.0 Arria 10 Edition August 2014

| Description | Impact |
|---|---|
| Changed GUI. When upgrading, you lose any value in **Memory Initial Mode ➤ File name**. For the work around, refer to the Knowledge Base. | - |

### Related Information

- Internal Memory (ROM and RAM) User Guide
- Errata for other IP cores in the Knowledge Base

## 1.72. SCFIFO and DCFIFO IP Cores v15.1

### Table 74. v15.1 November 2015

| Description | Impact |
|---|---|
| Added a new GUI parameter, **enable_ecc**, for Arria 10 devices. The **enable_ecc** parameter specifies whether to enable the error correction code (ECC) feature that corrects single-bit errors and double-adjacent bit errors, and detects triple-adjacent bit errors at the output of the memory. | This change is optional. If you do not upgrade your IP core, it does not have this new feature. |
| Added a new signal, `eccstatus` that indicates the ECC status of the data. | |

### Related Information

- Introduction to Altera IP Cores
- SCFIFO and DCFIFO IP Cores User Guide
- Errata for other IP cores in the Knowledge Base

## 1.73. SLD Hub Controller System v14.1

### Table 75. v14.1 December 2014

| Description | Impact |
|---|---|
| Enhanced the register map | The pre-v14.1 and v14.1 register maps are similar. Pre v14.1 register maps work unchanged with v14.1 hardware. |

#### Related Information

Errata for other IP cores in the Knowledge Base

## 1.74. Time-of-day Clock IP Core v16.0

### Table 76. v16.0 May 2016

| Description | Impact |
|---|---|
| Added offset, jitter, and wander functionalities, and new parameters to support them. | — |

#### Related Information

- Introduction to Altera IP Cores
- Ethernet Design Example Components User Guide
- Errata for other IP cores in the Knowledge Base