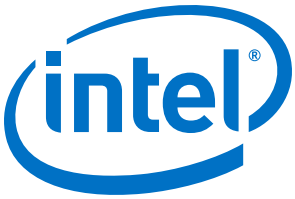

# Low Latency Ethernet 10G MAC Intel® FPGA IP Release Notes

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# Contents

# Low Latency Ethernet 10G MAC Intel® FPGA IP Release Notes

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the *Intel® Quartus® Prime Design Suite Update Release Notes*.

### Related Information

- Intel Quartus Prime Design Suite Update Release Notes
- Low Latency Ethernet 10G MAC Intel FPGA IP User Guide Archives
- Low Latency Ethernet 10G MAC Intel Stratix® 10 Design Example User Guide Archives
- Low Latency Ethernet 10G MAC Intel Arria® 10 Design Example User Guide Archives
- Low Latency Ethernet 10G MAC Intel Cyclone® 10 GX Design Example User Guide Archives
- Errata for the Low Latency Ethernet 10G MAC Intel FPGA IP in the Knowledge Base

## Low Latency Ethernet 10G MAC Intel FPGA IP v19.1

### Table 1. v19.1 April 2019

| Description | Impact |
|---|---|
| Renamed the **Enable Altera Debug Master Endpoint** parameter to **Enable Native PHY Debug Master Endpoint** as per Intel rebranding in the Intel Quartus Prime Pro Edition software. The Intel Quartus Prime Standard Edition software still uses **Enable Altera Debug Master Endpoint**. | — |

## Low Latency Ethernet 10G MAC Intel FPGA IP v18.1

### Table 2. v18.1 September 2018

| Description | Impact |
|---|---|
| Added support for the following operation mode for Intel Cyclone® 10 GX devices:<br>• 10M/100M/1G/2.5G/5G/10G (USXGMII) | — |
| Design Example for Low Latency 10G Ethernet MAC Intel FPGA IP:<br>• Added the following design example for Intel Cyclone 10 GX devices:<br>— 10M/100M/1G/2.5G/5G/10G (USXGMII) Ethernet | — |

### Related Information

- Introduction to Intel FPGA IP Cores

- Intel FPGA Low Latency Ethernet 10G MAC Intel FPGA IP User Guide
- Intel FPGA Low Latency Ethernet 10G MAC Intel Cyclone 10 GX FPGA IP Design Example User Guide
- Errata for Low Latency Ethernet 10G MAC Intel FPGA IP in the Knowledge Base

## Low Latency Ethernet 10G MAC Intel FPGA IP v18.0

### Table 3. v18.0 May 2018

| Description | Impact |
|---|---|
| Renamed Low Latency Ethernet 10G MAC IP core to Low Latency Ethernet 10G MAC Intel FPGA IP core as per Intel rebranding. | — |
| Added support for the following operation modes for Intel Stratix® 10 devices:<br>• 10M/100M/1G/2.5G/5G/10G (USXGMII)<br>• 10M/100M/1G/2.5G/5G/10G (USXGMII) with IEEE 1588v2 feature | — |
| Added support for the following operation mode for Intel Arria® 10 devices:<br>• 10M/100M/1G/2.5G/5G/10G (USXGMII) | — |
| Added new parameter for LL Ethernet 10G MAC Intel FPGA IP:<br>• **TX and RX datapath Reset/Default to Enable**:<br>Turning on this parameter disables TX and RX datapath during startup or CSR reset. | — |
| Design Examples for Low Latency 10G Ethernet MAC Intel FPGA IP:<br>• Added the following design example for Intel Stratix 10 devices:<br>— 10M/100M/1G/2.5G/5G/10G (USXGMII) Ethernet<br>— 10M/100M/1G/2.5G/5G/10G (USXGMII) Ethernet with IEEE 1588v2 feature<br>• Added the following design example for Intel Arria 10 devices:<br>— 10M/100M/1G/2.5G/5G/10G (USXGMII) Ethernet<br>• Added the following design example for Intel Cyclone 10 GX devices:<br>— 10GBASE-R Ethernet | — |

#### Related Information

- Introduction to Intel FPGA IP Cores
- Intel FPGA Low Latency Ethernet 10G MAC Intel FPGA IP User Guide
- Intel FPGA Low Latency Ethernet 10G MAC Intel Stratix 10 FPGA IP Design Example User Guide
- Intel FPGA Low Latency Ethernet 10G MAC Intel Arria 10 FPGA IP Design Example User Guide
- Intel FPGA Low Latency Ethernet 10G MAC Intel Cyclone 10 GX FPGA IP Design Example User Guide
- Errata for Low Latency Ethernet 10G MAC Intel FPGA IP in the Knowledge Base

## Intel FPGA Low Latency Ethernet 10G MAC IP Core v17.1 Update 1

### Table 4. v17.1 Update 1 December 2017

| Description | Impact |
|---|---|
| 10GBASE-R register mode is now supported in Intel Stratix 10 devices. | — |

### Related Information

- Introduction to Intel FPGA IP Cores
- Intel FPGA Low Latency Ethernet 10G MAC User Guide
- Intel FPGA Low Latency Ethernet 10G MAC Design Example User Guide for Intel Stratix 10 Devices
- Intel FPGA Low Latency Ethernet 10G MAC Design Example User Guide for Intel Arria 10 Devices
- Errata for Low Latency Ethernet 10G MAC IP core in the Knowledge Base

## Intel FPGA Low Latency Ethernet 10G MAC IP Core v17.1

### Table 5. v17.1 November 2017

| Description | Impact |
|---|---|
| Added support for the Intel Cyclone 10 GX device family. | This device is only available in Intel Quartus Prime software version 17.1 onwards. |
| Added support for the following operation modes for Intel Stratix 10 devices:<br>• 10/100M/1G/2.5G<br>• 10M/100M/1G/2.5G/10G | — |
| Added a new feature—Peer-to-Peer:<br>• Added a new parameter—**Enable peer-to-peer support**.<br>• Added new timestamp registers:<br>— Added new IEEE 1588v2 Egress TX signals—`tx_egress_p2p_update` and `tx_egress_p2p_val[]`.<br>— Added new IEEE 1588v2 Ingress RX signals—`rx_ingress_p2p_val[]` and `rx_ingress_p2p_val_valid`. | These changes are optional. If you do not upgrade your IP core, it does not have these new features. |
| You cannot turn on the **Enable ECC on memory blocks** parameter with the **Enable time stamping** parameter. | The IP core may not exhibit the expected behavior when both parameters are turned on at the same time. This is applicable in Intel Quartus Prime Pro Edition and Intel Quartus Prime Standard Edition version 17.0 and earlier. |
| Design Examples for Low Latency 10G Ethernet MAC:<br>• Added the following design examples for Intel Stratix 10 devices:<br>— 10M/100M/1G/2.5G/10G Ethernet<br>— 1G/2.5G Ethernet with IEEE 1588v2<br>— 1G/2.5G/10G Ethernet with IEEE 1588v2<br>— 10G USXGMII Ethernet | — |
| In previous versions of the Low Latency Ethernet 10G MAC design example for Intel Arria 10 devices, the IOPLL and transceiver PLL output may experience additional jitter. The additional jitter occurs if you source the reference clock from a cascaded PLL output, global clock, or core clock. To compensate for the jitter, the designs require additional constraints. This issue has been fixed in Intel Quartus Prime version 17.1. | If you are upgrading designs that have these additional constraints from the previous versions of Intel Quartus Prime to version 17.1, you must revise the constraints. Refer to the KDB page for more information. |
| 10GBASE-R register mode is not supported in Intel Stratix 10 devices. | — |

### Related Information

- Introduction to Intel FPGA IP Cores
- Intel FPGA Low Latency Ethernet 10G MAC User Guide
- Intel FPGA Low Latency Ethernet 10G MAC Design Example User Guide for Intel Stratix 10 Devices
- Intel FPGA Low Latency Ethernet 10G MAC Design Example User Guide for Intel Arria 10 Devices
- Errata for Low Latency Ethernet 10G MAC IP core in the Knowledge Base
- KDB Link: Compensating for the jitter of PLL cascading or non-dedicated clock path for Intel Arria 10 PLL reference clock

## Low Latency Ethernet 10G MAC IP Core v17.0

### Table 6. v17.0 May 2017

| Description | Impact |
|---|---|
| Stratix 10 supports for the following operation modes:<br>• 1G/2.5G/10G MAC with 1G/2.5G/10G Multi-rate Ethernet PHY<br>• 1G/2.5G/10G MAC with 1G/2.5G/10G Multi-rate Ethernet PHY and IEEE 1588v2<br>• 1G/2.5G MAC with 1G/2.5G Multi-rate Ethernet PHY<br>• 1G/2.5G MAC with 2.5G Multi-rate Ethernet PHY<br>• 10M/100M/1G/10G MAC with IEEE 1588v2<br>• 1G/10G MAC with Backplane Ethernet 10GBASE-KR PHY | — |
| Design Examples for Low Latency 10G Ethernet MAC:<br>• Added the following design examples for Stratix 10:<br>— 1G/2.5G Ethernet Design Example with IEEE 1588v2 Feature<br>— 1G/2.5G/10G Ethernet Design Example | |

### Related Information

- Introduction to Altera IP Cores
- Low Latency Ethernet 10G MAC User Guide
- Errata for Low Latency Ethernet 10G MAC IP core in the Knowledge Base

## Low Latency Ethernet 10G MAC IP Core v16.1

### Table 7. v16.1 October 2016

| Description | Impact |
|---|---|
| Added support for Stratix 10 devices. | — |
| Added new parameter for LL Ethernet 10G MAC IP Core:<br>• **Asymmetry support**:<br>Turning on this parameter enables asymmetry support on TX datapath. | |

### Related Information

- Introduction to Altera IP Cores
- Low Latency Ethernet 10G MAC MegaCore Function User Guide
- Errata for Low Latency Ethernet 10G MAC IP core in the Knowledge Base

# Low Latency Ethernet 10G MAC IP Core v16.0

## Table 8. v16.0 May 2016

| Description | Impact |
|---|---|
| • Support for 1G/2.5G/5G/10G (USXGMII) operating modes.<br>• Design Examples for Low Latency 10G Ethernet MAC:<br>— Added the following design examples:<br>• 10G USXGMII Ethernet<br>• 10GBase-R<br>• 1G/2.5G Ethernet<br>• 1G/2.5G Ethernet with 1588<br>• 1G/2.5G/10G Ethernet<br>— Added support for custom development board.<br>— Enhanced reset scheme for the following design examples, where the MAC reset is decoupled from the PHY reset:<br>• 10M/100M/1G/10G Ethernet<br>• 10M/100M/1G/10G Ethernet with 1588<br>• 1G/10G Ethernet<br>• 1G/10G Ethernet with 1588<br>— Added a SignalTap file (`.stp`) for the following designs:<br>• 10GBase-R Register Mode<br>• 10M/100M/1G/10G Ethernet<br>• 10M/100M/1G/10G Ethernet with 1588<br>• 1G/10G Ethernet<br>• 1G/10G Ethernet with 1588 | — |

### Related Information

- Introduction to Altera IP Cores
- Low Latency Ethernet 10G MAC MegaCore Function User Guide
- Errata for Low Latency Ethernet 10G MAC IP core in the Knowledge Base

# Low Latency Ethernet 10G MAC IP Core v15.1

## Table 9. v15.1 November 2015

| Description | Impact |
|---|---|
| • Support for 1G/2.5 and 1G/2.5G/10G operating modes.<br>• Generation of the following design examples:<br>— 10GBase-R Register Mode<br>— 1G/10G Ethernet<br>— 1G/10G Ethernet with 1588<br>— 10M/100M/1G/10G Ethernet<br>— 10M/100M/1G/10G Ethernet with 1588<br>• Enhanced unidirectional feature to support user-triggered remote fault notification through the register bit. | — |

### Related Information

- Introduction to Altera IP Cores
- Low Latency Ethernet 10G MAC MegaCore Function User Guide
- Errata for Low Latency Ethernet 10G MAC IP core in the Knowledge Base

# Low Latency Ethernet 10G MAC IP Core v15.0

## Table 10. v15.0 May 2015

| Description | Impact |
|---|---|
| Added new registers:<br>• Software reset register for TX and RX datapaths.<br>• Transfer status registers for TX and RX datapaths.<br>• VLAN and stacked VLAN detection disable.<br>• Programmable IPG registers for 10G and 10M/100M/1G operating speeds. | If you do not upgrade your IP core, it does not have this new feature. |

### Related Information

- Introduction to Altera IP Cores
- Low Latency Ethernet 10G MAC MegaCore Function User Guide
- Errata for Low Latency Ethernet 10G MAC IP core in the Knowledge Base

# Low Latency Ethernet 10G MAC IP Core v14.1

## Table 11. v14.1 December 2014

| Description | Impact |
|---|---|
| Added new parameter options:<br>• Enable 10GBASE-R register mode<br>• Time of Day Format. | If you do not upgrade your IP core, it does not have this new feature. |
| Added new signals to support 10GBASE-R register mode:<br>• `tx_xcvr_clk`<br>• `rx_xcvr_clk`<br>• `xgmii_tx_valid`<br>• `xgmii_rx_valid` | |

### Related Information

- Introduction to Altera IP Cores
- Low Latency Ethernet 10G MAC MegaCore Function User Guide
- Errata for Low Latency Ethernet 10G MAC IP core in the Knowledge Base

# Low Latency Ethernet 10G MAC IP Core v14.0 Arria 10 Edition

## Table 12. v14.0 Arria 10 Edition August 2014

| Description | Impact |
|---|---|
| Verified in the Quartus II software v14.0 Arria 10 Edition. (Added support for Arria 10 devices). | If you upgrade your IP core to the Quartus II software v14.0 Arria 10 Edition, all of the changes require that you regenerate the IP core manually and reconnect it in your design. |

### Related Information

- Introduction to Altera IP Cores

- Low Latency Ethernet 10G MAC MegaCore Function User Guide
- Errata for Low Latency Ethernet 10G MAC IP core in the Knowledge Base

## Low Latency Ethernet 10G MAC IP Core v14.0

### Table 13. v14.0 June 2014

| Description | Impact |
|---|---|
| Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*. | - |
| Added support for unidirectional feature. | The following changes are optional. If you do not upgrade your IP core, it does not have these new features. |
| Modified the reset behavior—TX and RX reset signals changed from asynchronous reset to synchronous reset. | |
| Resource improvement with no impact to performance. | |

#### Related Information

- Introduction to Altera IP Cores
- Low Latency Ethernet 10G MAC MegaCore Function User Guide
- Errata for Low Latency Ethernet 10G MAC IP core in the Knowledge Base

## Low Latency Ethernet 10G MAC IP Core v13.1 Arria 10 Edition

### Table 14. v13.1 Arria 10 Edition December 2013

| Description | Impact |
|---|---|
| Added support for Arria 10 devices. | - |

#### Related Information

- Introduction to Altera IP Cores
- Low Latency Ethernet 10G MAC MegaCore Function User Guide
- Errata for Low Latency Ethernet 10G MAC IP core in the Knowledge Base

## Low Latency Ethernet 10G MAC IP Core v13.1

### Table 15. v13.1 November 2013

| Description | Impact |
|---|---|
| Initial release.<br>• Lowest latency 10-Gbps Ethernet MAC with 32-bit user interface mode.<br>• Final support for Arria V GZ and Stratix V devices. | - |

#### Related Information

- Introduction to Altera IP Cores
- Low Latency Ethernet 10G MAC MegaCore Function User Guide
- Errata for Low Latency Ethernet 10G MAC IP core in the Knowledge Base