



# Low Latency 40-Gbps Ethernet IP Core Release Notes

***RN-1142***  
***2017.07.07***

 [Subscribe](#)

 [Send Feedback](#)



## Contents

---

<b>1 Low Latency 40-Gbps Ethernet IP Core Release Notes.....</b>	<b>3</b>
1.1 Low Latency 40-Gbps Ethernet IP Core v16.1.....	3



## 1 Low Latency 40-Gbps Ethernet IP Core Release Notes

Prior to the software release v16.0, the Low Latency 40-Gbps Ethernet and Low Latency 100-Gbps Ethernet IP cores were not available separately in the IP Catalog. For release notes for the Low Latency 40-Gbps Ethernet IP core for software releases v16.0 and earlier, refer to the *Low Latency 40- and 100-Gbps Ethernet MAC and PHY IP Core Release Notes*.

If a release note is not available for a specific IP core version, the IP core has no changes in that version. Information on the latest update releases is in the *Intel Quartus Prime Design Suite Update Release Notes*.

### Related Links

- [Low Latency 40- and 100-Gbps Ethernet MAC and PHY IP Core Release Notes](#)
- [Intel Quartus Prime Design Suite Update Release Notes](#)

### 1.1 Low Latency 40-Gbps Ethernet IP Core v16.1

**Table 1. Version 16.1 October 2016**

Description	Impact	Notes
Enhanced malformed packet handling. The IP core now ignores standard flow control pause packets if they are runt packets or have FCS errors. This change does not affect the IP core's handling of priority-based flow control packets.	The IP core potentially exhibits a behavior change. If you turn on standard flow control, the IP core might not process some incoming pause packets that it would previously have processed. The IP core continues to forward or drop these packets according to the setting in the <code>RX_PAUSE_FWD</code> register at offset 0x706.	Change required for UNH compliance.
Added new option for strict SFD checking. The IP provides a new parameter <b>Enable strict SFD checking</b> . If you turn on this parameter, the IP core checks the SFD and preamble bytes in all incoming packets for the following values: <ul style="list-style-type: none"> <li>• SFD = 0xD5</li> <li>• Preamble = 0x555555555555</li> </ul> Whether you turn on this parameter or not, the IP core checks for a correct Start byte (Start = 0xFB).	The IP core potentially exhibits a behavior change. If you turn on the new parameter, the IP core might reject some incoming packets that it would previously have processed.	Change required for UNH compliance.

### Related Links

- [Low Latency 40- and 100-Gbps Ethernet MAC and PHY MegaCore Function User Guide](#)  
With this software release, the Low Latency 40-Gbps Ethernet IP core is still documented in the joint IP core user guide.
- [Errata for Low Latency 40- and 100-Gbps Ethernet MAC and PHY IP core in the Knowledge Base](#)

Intel Corporation. All rights reserved. Intel, the Intel logo, Altera, Arria, Cyclone, Enpirion, MAX, Nios, Quartus and Stratix words and logos are trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.

\*Other names and brands may be claimed as the property of others.

ISO  
9001:2008  
Registered



Older errata for the combined LL 40-100GbE IP core

- [Errata for Low Latency 40-Gbps Ethernet IP core in the Knowledge Base](#)  
Newer errata for the LL 40GbE IP core only