Low Latency 40- and 100-Gbps Ethernet MAC and PHY IP Core Release Notes

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In the software version 16.1 and later, these two IP cores are separated in the IP Catalog and have their own IP Release Notes documents, the *Low Latency 40-Gbps Ethernet IP Core Release Notes* and the *Low Latency 100-Gbps Ethernet IP Core Release Notes*.

If a release note is not available for a specific IP core version, the IP core has no changes in that version. Information on the latest update releases is in the Software and Device Support Release Notes.

Related Information

- Low Latency 40-Gbps Ethernet IP Core Release Notes
- Low Latency 100-Gbps Ethernet IP Core Release Notes
- Intel Quartus Prime Pro Edition Software and Device Support Release Notes Archives
- Intel Quartus Prime Standard Edition Software and Device Support Release Notes Archives

Low Latency 40- and 100-Gbps Ethernet MAC and PHY IP Core v15.1

Table 1: Version 15.1 November 2015

Arria 10 support for this IP core is available in the Altera MegaCore IP Library. Stratix V support is available only through the Self-Service Licensing center.

Description	Impact	Notes
In Arria 10 variations. added new parameters **Enable Altera Debug Master Endpoint** and **Enable ODI acceleration logic**.	Upgrading the IP core to incorporate these features is optional. This change does not affect the top-level signals of the IP core.	These parameters expose control of transceiver configuration features.
Made comprehensive changes to 1588 PTP interfaces.	Upgrading the IP core to incorporate this feature is optional. In variations that include the 1588 PTP support feature, the interface changes modify and add top-level output signals to the IP core. Therefore, to utilize the 1588 PTP support feature after you upgrade, you must reconnect the IP core in your design.	Refer to LL 40-100GbE IP Core Signal Changes v15.1 table.

Description	Impact	Notes
Added new 1588 PTP parameters **Enable 96b Time of Day Format**, **Enable 64b Time of Day Format**, and **Timestamp fingerprint width**.	Upgrading the IP core to incorporate this feature is optional. These parameters are available only if you turn on the **Enable 1588 PTP** parameter.	
Removed `TX_PTP_STATUS` register.	Upgrading the IP core to incorporate this feature is optional. If you upgrade your IP core to the v15.1 version, you must be aware of this change in variations that include the 1588 PTP support feature.	
Added new 1588 PTP registers `TX_PTP_ASYM_DELAY`, `TX_PTP_PMA_LATENCY`, and `RX_PTP_PMA_LATENCY`.	Upgrading the IP core to incorporate this feature is optional. If you upgrade your IP core to the v15.1 version, you must be aware of these changes in variations that include the 1588 PTP support feature.	
Added dedicated **Example Design** tab in parameter editor for Arria 10 variations.	Upgrading the IP core to incorporate this feature is optional. If you upgrade your IP core, you should use the **Example Design** tab to generate a testbench and design example that work correctly with the upgraded IP core.	
Added hardware test you can run on the hardware design example.	Upgrading the IP core and regenerating the example design to incorporate this feature is optional. If you upgrade the IP core but do not regenerate the example design, this feature is not available.	
Minor changes to LL 40GBASE-KR4 feature register default values.	If you upgrade your IP core to the v15.1 version, you must be aware of these changes in LL 40GBASE-KR4 variations.	

Table 2: LL 40-100GbE IP Core Signal Changes v15.1

All signal changes are associated with the PTP module. Signals added or modified in version 15.1 are due to a comprehensive change in the 1588 PTP interface. All correspondences between old and new signal names are approximate: many of the new signals indicate a combination of old signal values or incorporate information previously available in the `TX_PTP_STATUS` register. Other signals are added for the new 64-bit timestamp option.

Notes specify the expected usage of the new signal. In most cases the output signals are in fact available in the other processing modes and your design can use them in other processing modes. For full information about the sets of mutually exclusive input signals, refer to the LL 40-100GbE IP core user guide.

Old Signal Name	New Signal Name	Notes
`tod_rxmac_in[95:0]`	`rx_time_of_day_96b_data[95:0]`	RX PTP interface to TOD module: Two distinct signals to support the **Enable 96b Time of Day Format** and **Enable 64b Time of Day Format** parameters.
	`rx_time_of_day_64b_data[63:0]`	
`tod_txmac_in[95:0]`	`tx_time_of_day_96b_data[95:0]`	TX PTP interface to TOD module: Two distinct signals to support the **Enable 96b Time of Day Format** and **Enable 64b Time of Day Format** parameters.
	`tx_time_of_day_64b_data[63:0]`	
`rx_tod[95:0]`	`rx_ingress_timestamp_96b_data[95:0]`	RX PTP interface to TOD module: Two distinct signals to support the **Enable 96b Time of Day Format** and **Enable 64b Time of Day Format** parameters.
	`rx_ingress_timestamp_64b_data[63:0]`	
—	`rx_ingress_timestamp_96b_valid`	RX PTP interface: Valid signal for `rx_ingress_timestamp_96b_data`.
—	`rx_ingress_timestamp_64b_valid`	RX PTP interface: Valid signal for `rx_ingress_timestamp_64b_data`.
`tx_in_ptp`	`tx_egress_timestamp_request_valid`	Incorporates functionality of old `tx_in_ptp` signal (tells the IP core the current incoming packet on the TX client interface is a PTP packet) and also tells the IP core to process this packet in two-step processing mode.
	`tx_etstamp_ins_ctrl_timestamp_insert`	Incorporates functionality of old `tx_in_ptp` signal (tells the IP core the current incoming packet on the TX client interface is a PTP packet) and also tells the IP core to process this packet in one-step processing insertion mode.
	`tx_etstamp_ins_ctrl_residence_time_update`	Incorporates functionality of old `tx_in_ptp` signal (tells the IP core the current incoming packet on the TX client interface is a PTP packet) and also tells the IP core to process this packet in tone-step processing correction mode.

Old Signal Name	New Signal Name	Notes
tod_tx_clk_st2[95:0]	tx_egress_timestamp_96b_data[95:0]	TX PTP two-step processing: Two distinct signals to support the **Enable 96b Time of Day Format** and **Enable 64b Time of Day Format** parameters.
	tx_egress_timestamp_64b_data[63:0]	
ptp_pkt_out	tx_egress_timestamp_96b_valid	TX PTP two-step processing: Two distinct signals to support the **Enable 96b Time of Day Format** and **Enable 64b Time of Day Format** parameters.
	tx_egress_timestamp_64b_valid	
—	tx_egress_timestamp_request_fingerprint	TX PTP fingerprint: Fingerprint in.
—	tx_egress_timestamp_96b_fingerprint	TX PTP fingerprint: Fingerprint out (96-bit timestamp interface).
—	tx_egress_timestamp_64b_fingerprint	TX PTP fingerprint: Fingerprint out (64-bit timestamp interface).
tx_in_ptp_overwrite[1:0]	—	
—	tx_etstamp_ins_ctrl_timestamp_format	TX PTP one-step processing insertion mode: timestamp format (96-bit or 64-bit).
—	tx_etstamp_ins_ctrl_residence_time_calc_format	TX PTP one-step processing correction mode: latency format (96-bit or 64-bit).
tx_in_ptp_offset[15:0]	tx_etstamp_ins_ctrl_offset_timestamp[15:0]	TX PTP one-step processing insertion mode: timestamp offset.
	tx_etstamp_ins_ctrl_offset_correction_field[15:0]	TX PTP one-step processing correction mode: correction field offset. Also the location for two bytes of inserted 96-bit timestamp (in insertion mode).
—	tx_etstamp_ins_ctrl_ingress_timestamp_96b[95:0]	TX PTP one-step processing: 96-bit entry timestamp.

Old Signal Name	New Signal Name	Notes
—	tx_etstamp_ins_ctrl_ingress_timestamp_64b[63:0]	TX PTP one-step processing: 64-bit entry timestamp.
tx_in_zero_tcp	tx_etstamp_ins_ctrl_checksum_zero	TX PTP one-step processing: Set checksum to the value of zero.
	tx_etstamp_ins_ctrl_checksum_correct	TX PTP one-step processing: Update the checksum following the timestamp update.
tx_in_tcp_offset[15:0]	tx_etstamp_ins_ctrl_offset_checksum_field[15:0]	TX PTP one-step processing, offset to zero the checksum (required if you assert tx_etstamp_ins_ctrl_checksum_zero).
	tx_etstamp_ins_ctrl_offset_checksum_correction[15:0]	TX PTP one-step processing, offset to update (correct) the checksum (required if you assert tx_etstamp_ins_ctrl_checksum_correct).
—	tx_egress_asymmetry_update	Tells the IP core to use the value in the new TX_PTP_ASYM_DELAY register.

Related Information

- **Low Latency 40- and 100-Gbps Ethernet MAC and PHY MegaCore Function User Guide**
- **Low Latency 40-Gbps Ethernet IP Core User Guide**
- **Low Latency 100-Gbps Ethernet IP Core User Guide**

Low Latency 40- and 100-Gbps Ethernet MAC and PHY IP Core v15.0

Table 3: Version 15.0 May 2015

Arria 10 support for this IP core is available in the Altera MegaCore IP Library. Stratix V support is available only through the Self-Service Licensing center.

Description	Impact	Notes
If you upgrade the LL 40-100GbE IP core to the IP core v15.0, the example design no longer functions correctly. You must regenerate the example design after you upgrade.	After you upgrade your IP core, you must regenerate the example design.	

Description	Impact	Notes
Added optional Synchronous Ethernet support for Arria 10 variations. Turning on the new **Enable SyncE** parameter adds a new RX recovered clock output signal.	Upgrading the IP core to incorporate this feature is optional. This feature does not affect the top-level signals of the IP core unless you turn on the **Enable SyncE** parameter. If you upgrade, turn on this parameter, and intend to implement a Synchronous Ethernet system, you must reconnect the IP core in your design.	Refer to LL 40-100GbE IP Core Signal Changes v15.0 table.
Changed handling of received malformed packets: • The IP core asserts the `l<n>_rx_error[0]` or `rx_error[0]` signal in the case of an unexpected control character that is not an Error character. • Both the LL 40GbE IP core and the LL 100GbE IP core handle received malformed packets the same way.	If you upgrade your IP core to the v15.0 version, you must be aware of this behavior change.	
New output signals explain the control frames that the IP core passes to the RX client interface. The output flags indicate whether the control frame is a standard flow-control frame, a priority-based flow-control frame, or a non-flow control frame.	Upgrading the IP core to incorporate this feature is optional. This feature adds top-level output signals to the IP core. Therefore, to utilize this feature after you upgrade, you must reconnect the IP core in your design.	Refer to LL 40-100GbE IP Core Signal Changes v15.0 table.
Priority-based flow control is now available for both LL 40GbE IP core variations and LL 100GbE IP core variations. Previously it was available only in LL 100GbE variations.	Upgrading the IP core to incorporate this feature is optional. This feature does not affect the top-level signals of the IP core.	
New output status flag indicates when TX lanes are fully aligned and ready to transmit data.	Upgrading the IP core to incorporate this feature is optional. This feature adds top-level output signals to the IP core. Therefore, to utilize this feature after you upgrade, you must reconnect the IP core in your design.	Refer to LL 40-100GbE IP Core Signal Changes v15.0 table.
New option to direct the IP core to insert an error in a transmitted Ethernet frame.	Upgrading the IP core to incorporate this feature is optional. This feature adds top-level input signals to the IP core. Therefore, if you upgrade, you must reconnect the IP core in your design.	Refer to LL 40-100GbE IP Core Signal Changes v15.0 table.

Description	Impact	Notes
The IP core now generates an example project that you can configure on a device, for most variations. The older type of example projects, which you cannot configure on a device, are also generated.	Upgrading the IP core to incorporate this feature is optional.	
Minor changes to LL 40GBASE-KR4 feature parameters and registers: • Changed default value of link training **INITPOSTVAL** parameter from 22 to 13. • Changed `rx_ctle_mode` LL 40GBASE-KR4 register field. The IP core uses only the two least significant bits of the 10GBASE-KR register field.	If you upgrade your IP core to the v15.0 version, you must be aware of these changes, and set the parameter and access the register accordingly, in LL 40GBASE-KR4 variations..	

Table 4: LL 40-100GbE IP Core Signal Changes v15.0

Signals added or modified in version 15.0.

Old Signal Name	New Signal Name	Notes
—	`clk_rx_recover`	Output RX recovered clock intended to drive the input reference clock of another Ethernet component in a Synchronous Ethernet design. This signal is available if you turn on **Enable SyncE** in the LL 40-100GbE parameter editor.
—	`l<n>_rx_status[2:0]` (Avalon-ST client interface)	New three-bit control frame type flag.
—	`rx_status[2:0]` (custom client interface)	
—	`tx_lanes_stable`	New output status flag.
—	`l<n>_tx_error` (Avalon-ST client interface)	New TX error insertion signal. User logic asserts a bit to direct the IP core to insert an error in the corresponding frame on the Ethernet link.
—	`tx_error[1:0]` or `tx_error[3:0]` (custom client interface)	

Related Information

- Low Latency 40- and 100-Gbps Ethernet MAC and PHY MegaCore Function User Guide
- Low Latency 40-Gbps Ethernet IP Core User Guide
- Low Latency 100-Gbps Ethernet IP Core User Guide

Low Latency 40- and 100-Gbps Ethernet MAC and PHY IP Core v14.1

Table 5: Version 14.1 December 2014

Arria 10 support for this IP core is available in the Altera MegaCore IP Library. Stratix V support is available only through the Self-Service Licensing center.

Description	Impact	Notes
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade, but does not clarify the reason.	You must ensure that you specify a device for your v14.0 Arria 10 Edition IP core variation and regenerate it in the Quartus II software v14.1.	
Added optional 40GBASE-KR4 support in LL 40GbE IP core variations. Turning on the **Enable KR4** parameter makes many additional 40GBASE-KR4 specific parameters available. 40GBASE-KR4 variations have many additional registers but no additional signals.	Upgrading the IP core to incorporate this feature is optional. This feature does not affect the top-level signals of the IP core.	
All statistics increment vectors are now available and functional whether or not you include the relevant statistics counters in your IP core variations. Previously, the statistics increment vectors were functional only in IP core variations that included the relevant statistics module.	Upgrading the IP core to incorporate this feature is optional. This feature does not affect the top-level signals of the IP core.	
Added option to move the TX MAC PLL outside the IP core. Turning on the **Use external TX MAC PLL** parameter adds an input clock that drives the `clk_txmac` internal clock. This option adds no additional registers or register fields.	Upgrading the IP core to incorporate this feature is optional. This feature does not affect the top-level signals of the IP core unless you turn on the **Use external TX MAC PLL** parameter.	Refer to LL 40-100GbE IP Core Signal Changes table.

Description	Impact	Notes
Added two new 64-bit statistics counters RXOctets_OK at offset 0x960 and TXOctets_OK at offset 0x860 to count the payload bytes (octets) in received and transmitted frames with no FCS errors, undersized, oversized, or payload length errors. The two registers each have two associated new signals.	Upgrading the IP core to incorporate this feature is optional. If you upgrade the IP core to the v14.1 version, this feature adds top-level signals and therefore requires that you reconnect the IP core in your design.	Refer to LL 40-100GbE IP Core Signal Changes table.
Added new `CFG_PLEN_CHECK` register at offset 0x50A to support bit[4] of the new six-bit RX error signal.	If you upgrade your IP core to the v14.1 version and wish to use the new length checking status flag, you must ensure that user logic turns on the enable bit in this new register. In addition, the register supports a new RX error status flag signal that requires that you reconnect the IP core in your design.	
Changed handling of received malformed packet. If the IP core detects an incoming unexpected control character, it generates an EOP for the packet. Previously the IP core did not terminate (generate an EOP for) an incoming packet if it received an unexpected control character. In addition the IP core signals an error on the new six-bit RX error status signal when appropriate.	If you upgrade your IP core to the v14.1 version, you must be aware of this behavior change.	
Newly generated IP cores do not have top-level signals that interface to modules that the IP core does not include. This change applies to the TX MAC input clock, link fault signals, pause signals, and PTP signals.	Because of the backward compatibility feature described in the Notes column, if you upgrade your IP core to the v14.1 version, this feature has no effect on the top-level signals and does not require any additional actions. Note that this feature applies only to IP core variations that do not instantiate the relevant module or modules.	For backward compatibility, if you upgrade an IP core variation, link fault signals, pause top-level signals, and PTP signals in the earlier release of the IP core variation remain available in the 14.1 version after upgrade.
Updated PTP module behavior and modified parameter name. If you turn on **Enable 1588 PTP**, the PTP module has the following new features and requirements:	Upgrading the IP core to incorporate this feature is optional. If you upgrade the IP core to the v14.1 version, and the PTP module is included in your original IP core variation, this feature adds top-level	

Description	Impact	Notes
• You must instantiate a time-of-day (TOD) module and connect it to the IP core. • Added new PTP signals to receive the timestamps the TOD module generates in the two clock domains. Refer to LL 40-100GbE IP Core Signal Changes table. • Removed TX PTP module TOD calculation registers at offsets 0xB06 through 0xB08. The TOD module now provides the functionality the registers supported in previous versions of the IP core. • Added support for resetting the TCP checksum to zero of the application does not recalculate it. Added two new signals with which the application communicates such a request to the IP core. Refer to LL 40-100GbE IP Core Signal Changes table.	signals and therefore requires that you reconnect the IP core in your design.	
Improved RX skew tolerance to 1900 bits for LL 40GbE IP core variations and to 1000 bits for LL 100GbE IP core variations. Altera LL 40-100GbE IP cores exceed the IEEE 802.3-2012 Ethernet Standard Clause 82.2.12 requirements of 1856 bits skew tolerance for 40GbE IP cores and 928 bits skew tolerance for 100GbE IP cores.		

Table 6: LL 40-100GbE IP Core Signal Changes

Signals added or modified in version 14.1.

Old Signal Name	New Signal Name	Notes
—	`clk_txmac_in`	Input clock to drive the `clk_txmac` internal clock. This signal is available if you turn on **Use external TX MAC PLL** in the LL 40-100GbE parameter editor.

Old Signal Name	New Signal Name	Notes
l<n>_rx_error (1 bit)	l<n>_rx_error[5:0] (Avalon-ST client interface)	New six-bit RX error status signal.
—	rx_error[5:0] (custom client interface)	
—	unidirectional_en	Signals that provide status from the LINK_FAULT_CONFIG register.
—	link_fault_gen_en	
—	tx_inc_octetsOK[15:0]	Signals that provide per-frame information associated with the new RxOctets_OK and TXOctets_OK registers. These signals are present and functional whether or not you turn on **Enable TX statistics** or **Enable RX statistics** in the parameter editor.
—	tx_inc_octetsOK_valid	
—	rx_inc_octetsOK[15:0]	
—	rx_inc_octetsOK_valid	
—	tx_in_zero_tcp	Signals for application to direct the IP core to reset the TCP checksum field.
—	tx_in_tcp_offset[15:0]	
—	tod_txmac_in[95:0]	Signals to receive TOD values from new external TOD module.
—	tod_rxmac_in[95:0]	
Link fault signals are present in new IP core variations you generate in the Quartus II v14.1 IP Catalog only if you turn on **Enable link fault generation** in the parameter editor. For backward compatibility, the signals remain if you upgrade from a pre-14.1 IP core variation that has those signals.		
Pause signals are present in new IP core variations that you generate in the Quartus II v14.1 IP Catalog only if you set **Flow control mode** to standard flow control or priority-based flow control in the parameter editor. For backward compatibility, the signals remain if you upgrade from a pre-14.1 IP core variation that has those signals.		
PTP interface signals are present in new IP core variations that you generate in the Quartus II v14.1 IP Catalog only if you turn on **Enable 1588 PTP** in the parameter editor. For backward compatibility, the signals remain if you upgrade from a pre-14.1 IP core variation that has those signals.		

Related Information

- **Low Latency 40- and 100-Gbps Ethernet MAC and PHY MegaCore Function User Guide**
- **Low Latency 40-Gbps Ethernet IP Core User Guide**
- **Low Latency 100-Gbps Ethernet IP Core User Guide**

Low Latency 40- and 100-Gbps Ethernet MAC and PHY IP Core v14.0 Arria 10 Edition

Table 7: Version 14.0 Arria 10 Edition August 2014

Description	Impact	Notes
Initial release in the Intel FPGA IP Library.		

Related Information

- Low Latency 40- and 100-Gbps Ethernet MAC and PHY MegaCore Function User Guide
- Low Latency 40-Gbps Ethernet IP Core User Guide
- Low Latency 100-Gbps Ethernet IP Core User Guide