JESD204B Intel FPGA IP Release Notes

2019.04.01

RN-1125 Subscribe Send Feedback

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the *Intel® Quartus® Prime Design Suite Update Release Notes*.

Related Information

- **Intel Quartus Prime Design Suite Update Release Notes**
- **JESD204B Intel FPGA IP User Guide**
  Refer to the JESD204B Intel FPGA IP User Guide Archives section for previous versions.
- **JESD204B Intel Stratix® 10 FPGA IP Design Example User Guide**
  Refer to the JESD204B Intel Stratix 10 FPGA IP Design Example User Guide Archives section for previous versions.
- **JESD204B Intel Arria® 10 FPGA IP Design Example User Guide**
  Refer to the JESD204B Intel Arria 10 FPGA IP Design Example User Guide Archives section for previous versions.
- **JESD204B Intel Cyclone® 10 GX FPGA IP Design Example User Guide**
  Refer to the JESD204B Intel Cyclone 10 GX FPGA IP Design Example User Guide Archives section for previous versions.
- **Errata for JESD204B FPGA IP in the Knowledge Base**

JESD204B Intel FPGA IP v19.1

Table 1: v19.1 April 2019

Description	Impact
Added support for Intel Stratix® 10 E-tile devices. Merging of simplex TX and RX channels is not supported.	These changes are optional. If you do not manually upgrade your IP core and select E-tile for **Transceiver Tile**, it does not have these new features.
Added the **Transceiver Tile** parameter. This parameter is available when you target an Intel Stratix 10 device that supports both H-tile and E-tile. You can choose the tile that you want to use for your design.	
Added the following signals that are applicable only for Intel Stratix 10 E-tile devices. • `phy_tx_ready` • `phy_rx_ready` • `phy_tx_pma_ready` • `phy_rx_pma_ready` • `phy_tx_rst_n` • `phy_rx_rst_n` • `tx_serial_data_n` • `rx_serial_data_n`	
Renamed the **Enable Altera Debug Master Endpoint** parameter to **Enable Native PHY Debug Master Endpoint** as per Intel rebranding in the Intel Quartus Prime Pro Edition software. The Intel Quartus Prime Standard Edition software still uses **Enable Altera Debug Master Endpoint**.	—

JESD204B Intel FPGA IP v18.1

Table 2: v18.1 September 2018

Description	Impact
Added support for F=3 configurations for Intel Stratix 10 devices.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Revised the data rate support for Intel Stratix 10 soft PCS mode for FPGA fabric speed grades 2 and 3. • For PMA speed grade 1, 2, or 3 with FPGA fabric speed grade 2, the maximum supported data rate is 14.0 Gbps. • For PMA speed grade 3 with FPGA fabric speed grade 3, the maximum supported data rate is 13.0 Gbps..	

Related Information

- JESD204B Intel FPGA IP User Guide
- JESD204B Intel Stratix 10 FPGA Design Example User Guide
- JESD204B Intel Arria® 10 FPGA Design Example User Guide
- JESD204B Intel Cyclone® 10 FPGA Design Example User Guide
- Errata for JESD204B FPGA IP in the Knowledge Base

JESD204B Intel FPGA IP v18.0

Table 3: v18.0 May 2018

Description	Impact
Added support for Intel Cyclone® 10 GX FPGA devices and new design example tab for Intel Cyclone 10 GX in the parameter editor.	Intel Cyclone 10 GX devices are now supported in the 18.0 Intel Quartus Prime Pro Edition software.
Added back the **Target Development Kit** option for the Intel Stratix 10 design example. This parameter was not available in the JESD204B Intel FPGA IP version 17.1 Update 1. The target development board for the design example is FPGA development board.	Intel Stratix 10 design example is only available in the Intel Quartus Prime Pro Edition software.
Added support for Cadence Xcelium* Parallel simulator.	–

Related Information

- JESD204B Intel FPGA IP User Guide
- JESD204B Intel Stratix 10 FPGA Design Example User Guide
- JESD204B Intel Arria® 10 FPGA Design Example User Guide
- JESD204B Intel Cyclone 10 FPGA Design Example User Guide
- Errata for JESD204B FPGA IP in the Knowledge Base

JESD204B IP Core v17.1

Table 4: v17.1 November 2017

Description	Impact
Added support for Intel Stratix 10 FPGA devices.	Intel Stratix 10 devices are now supported in the 17.1 Intel Quartus Prime Pro Edition.
Added a new parameter—**Provide Separate Reconfiguration Interface for Each Channel**.	Available in Intel Quartus Prime Pro Edition only.

Description	Impact
Supports up to 12.5Gbps characterized to JESD204B specification. Supports up to 16Gbps not characterized to the JESD204B specification.	—
In previous versions of the JESD204B IP core design example for Intel Arria® 10 devices, the IOPLL and transceiver PLL output may experience additional jitter. The additional jitter occurs if you source the reference clock from a cascaded PLL output, global clock, or core clock. To compensate for the jitter, the designs require additional constraints. This issue has been fixed in Intel Quartus Prime version 17.1.	This issue affects designs that use Intel Arria 10 devices. If you are upgrading designs that have these additional constraints from the previous versions of Intel Quartus Prime to version 17.1, you must revise the constraints. Refer to the **KDB page** for more information.

Related Information

- **JESD204B IP Core User Guide**
- **Intel FPGA JESD204B Design Example User Guide for Intel Stratix 10 Devices**
- **Intel FPGA JESD204B Design Example User Guide for Intel Arria 10 Devices**
- **Errata for JESD204B IP core in the Knowledge Base**

JESD204B IP Core v17.0

Table 5: v17.0 May 2017

Description	Impact
Added support for Intel Stratix 10 FPGA devices.	Intel Stratix 10 devices are not supported in the Intel Quartus Prime Pro Edition. For more information, **contact Intel**.
Added `somf[]` for transmitter signal.	—
Updated data path preset value to simplex TX and simplex RX..	—
• Added a new parameter—**Share Reconfiguration Interface**.	This feature is available only for Intel Arria 10 and Intel Stratix 10 device family.

Related Information

- **JESD204B IP Core User Guide**
- **Errata for JESD204B IP core in the Knowledge Base**

JESD204B IP Core v16.1

Table 6: v16.1 October 2016

Description	Impact
Added status registers: • rx_status0, rx_status1, rx_status2, rx_status3 • tx_status0, tx_status1, tx_status2, tx_status3	—

Related Information

- **JESD204B IP Core User Guide**
- **Errata for JESD204B IP core in the Knowledge Base**
- **JESD204B RX Address Map and Register Definitions**
- **JESD204B TX Address Map and Register Definitions**

JESD204B IP Core v16.0

Table 7: v16.0 May 2016

Description	Impact
Support automatic generation of basic SignalTap® II Logic Analyzer files.	Simplifies generation of files for debugging.
Uncharacterized support for data rate of up to 15 Gbps.	—

Related Information

- **JESD204B IP Core User Guide**
- **Errata for JESD204B IP core in the Knowledge Base**

JESD204B IP Core v15.1

Table 8: v15.1 November 2015

Description	Impact
Added data rate support of up to 13.5 Gbps for Arria 10 and 7.5 Gbps for Arria V GT/ST devices.	—
Added a new selection for PCS Option parameter—Enabled PMA Direct.	—

Description	Impact
Changed the default value for *RX Phase Compensation FIFO empty error enable* (`csr_pcfifo_empty_err_en`) CSR to 0 (refer to the **RX register map**).	Disables the interrupt when PC FIFO empty condition occurs.
Added **Example Designs** tab in the parameter editor that automatically generates both simulation and hardware example designs with the parameters you specify.	—
Added a new design example—Nios II Control. The Altera JESD204B IP core now includes two design examples: • RTL State Machine Control (supports Arria V, Cyclone V, Stratix V, and Arria 10 devices only) • Nios II Control (supports Arria 10 devices only)	The RTL State Machine Control is a legacy design example and is renamed in this release.

Related Information

- **JESD204B IP Core User Guide**
- **Errata for JESD204B IP core in the Knowledge Base**

JESD204B IP Core v15.0

Table 9: v15.0 May 2015

Description	Impact
Added support for Cyclone V FPGA device family (up to 5 Gbps).	–
Added new parameters: • **Enable Capability Registers** • **Set user-defined IP identifier** • **Enable Control and Status Registers** • **Enable Prbs Soft Accumulators** • **Enable manual F configuration**	–
Added new register bits to support error detection (refer to **New Register Bits**).	These new register bits are available when you upgrade the IP core to v15.0.

Table 10: New Register Bits

Register	Bit	Description
tx_err (0x60)	csr_pll_locked_err	Detects and flags an error when one or more lanes of PLL locked loses lock while the JESD204B link is running.
	csr_pcfifo_full_err	Detects and flags an error when one or more lanes of the Phase Compensation FIFO is unexpectedly full while the JESD204B link is running.
	csr_pcfifo_empty_err	Detects and flags an error when one or more lanes of the Phase Compensation FIFO is unexpectedly empty while the JESD204B link is running.
tx_err_enable (0x64)	csr_pll_locked_err_en	Enable interrupt for PLL lose lock error.
	csr_pcfifo_full_err_en	Enable interrupt for Phase Compensation FIFO full error.
	csr_pcfifo_empty_err_en	Enable interrupt for Phase Compensation FIFO empty error.
rx_err0 (0x60)	csr_rx_locked_to_data_err	Detects and flags an error when one or more lanes is not locked to data while the JESD204B link is running.
	csr_pcfifo_full_err	Detects and flags an error when one or more lanes of the Phase Compensation FIFO is unexpectedly full while the JESD204B link is running.
	csr_pcfifo_empty_err	Detects and flags an error when when one or more lanes of the Phase Compensation FIFO is unexpectedly empty while the JESD204B link is running.
rx_err_enable (0x74)	csr_rx_locked_to_data_err_en	Enable interrupt for RX not locked to data error.
	csr_pcfifo_full_err_en	Enable interrupt for Phase Compensation FIFO full error.
	csr_pcfifo_empty_err_en	Enable interrupt for Phase Compensation FIFO empty error.
rx_err_link_ reinit (0x78)	csr_rx_locked_to_data_err_ link_reinit	Enable link reinitialization for RX not locked to data error.
	csr_pcfifo_full_err_link_ reinit	Enable link reinitialization for Phase Compensation FIFO full error.
	csr_pcfifo_empty_err_link_ reinit	Enable link reinitialization for Phase Compensation FIFO empty error.

Related Information

- JESD204B IP Core User Guide

- Errata for JESD204B IP core in the Knowledge Base

JESD204B IP Core v14.1

Table 11: 14.1 December 2014

Description	Impact
Revised the parameter name of **Enable PLL/CDR Dynamic Reconfiguration** to **Enable Transceiver Dynamic Reconfiguration**.	–
Added a new parameter—**Altera Debug Master Endpoint**. Enable this feature to access the reconfiguration space of the Transceiver Native PHY IP Core.	This feature is available only for Arria 10 device family.

Added new register bits:
• TX core:
  • Bit: `csr_reinit_w_rxsyncn_rise` in the `dll_ctrl` register (offset 0x50).
  • Description: This bit controls the Code Group Synchronization (CGS) state exit behavior during link re-initialization.
• RX core:
  • Bit: `csr_syncn_delay` in the `syncn_sysref_ctrl` register (offset 0x54).
  • Description: This bit extends the *SYNC_N* assertion (low state) by delaying the deassertion.
	The new register bits are available when you upgrade the IP core in your design to v14.1.

Updated the test_ilas_loop bit behavior in the `dll_ctrl` register (offset 0x50).	Upgrade the IP core in your design to v14.1 to implement this new behavior.
Changed the JESD204B Avalon-MM slave interface *readLatency* value from 0 to 1.	Upgrade the IP core in your design to v14.1 to implement this new behavior. If you upgrade your IP core in your design, you have to reconnect the IP core in your design due to port change.
Changed the interface type of the `jesd204_rx_int` and `jesd204_tx_int` signals from conduit to interrupt.	–
Changed signal type of `pll_locked`, `tx_cal_busy`, `rx_cal_busy`, and `rx_is_lockedtodata`.	–

Description	Impact
New simulation flow for the IP core design example testbench. Changed the link bring up sequence by powering up the JESD204B TX link and JESD204B RX link independently.	Regenerate the design example from the IP Parameter Editor to obtain this change.
Changed the default value of the 8B/10B encoder to /K28.5/ control word during reset assertion to resolve the CDR lock issue in the receiver. This change only affects design that select **Enabled Soft PCS** for the **PCS Option** parameter.	If you use **Enabled Soft PCS** for the **PCS Option** parameter, you must upgrade the IP core in your design to v14.1.

Related Information

- **JESD204B IP Core User Guide**
- **Errata for JESD204B IP core in the Knowledge Base**