# Contents

1 Interlaken PHY IP Core Release Notes.................................................................................. 3  
   1.1 Interlaken PHY IP Core v14.1 Revision History.............................................................. 3 
   1.2 Interlaken PHY IP Core v14.0 Revision History.............................................................. 3 
   1.3 Interlaken PHY IP Core v13.1 Revision History.............................................................. 3
1 Interlaken PHY IP Core Release Notes

If a release note is not available for a specific IP core version, the IP core has no changes in that version. Information on the latest update releases is in the Quartus Prime Design Suite Update Release Notes.

Related Links
Quartus Prime Design Suite Update Release Notes

1.1 Interlaken PHY IP Core v14.1 Revision History

Table 1. v14.1 December 2014

<table>
<thead>
<tr>
<th>Description</th>
<th>Impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>Verified in Quartus II software v14.1</td>
<td>-</td>
</tr>
</tbody>
</table>

Related Links
- Altera Transceiver PHY IP Core User Guide
- Errata for Interlaken PHY IP Core in the Knowledge Base
- Introduction to Altera IP Cores

1.2 Interlaken PHY IP Core v14.0 Revision History

Table 2. v14.0 July 2014

<table>
<thead>
<tr>
<th>Description</th>
<th>Impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to IP Catalog and Parameter Editor in Introduction to Altera IP Cores.</td>
<td>-</td>
</tr>
</tbody>
</table>

Related Links
- Altera Transceiver PHY IP Core User Guide
- Errata for Interlaken PHY IP Core in the Knowledge Base
- Introduction to Altera IP Cores

1.3 Interlaken PHY IP Core v13.1 Revision History

Table 3. v13.1 November 2013

<table>
<thead>
<tr>
<th>Description</th>
<th>Impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>Verified in the Quartus II software v13.1</td>
<td>-</td>
</tr>
</tbody>
</table>

© 2016 Intel Corporation. All rights reserved. Intel, the Intel logo, Altera, Arria, Cyclone, Enpirion, MAX, Megacore, NIOS, Quartus and Stratix words and logos are trademarks of Intel Corporation in the US and/or other countries. Other marks and brands may be claimed as the property of others. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.
Related Links

- Altera Transceiver PHY IP Core User Guide
- Errata for Interlaken PHY IP Core in the Knowledge Base
- Introduction to Altera IP Cores