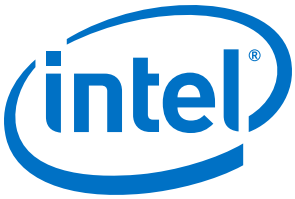

IOPLL Intel FPGA IP Core Release Notes

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If a release note is not available for a specific IP core version, the IP core has no changes in that version. Information on the latest update releases is in the *Intel Quartus Prime Design Suite Update Release Notes*.

Related Information

Intel Quartus Prime Design Suite Update Release Notes

IOPLL Intel FPGA IP v18.0

Table 1. v18.0 May 2018

Description	Impact
Renamed Intel FPGA IOPLL IP core to IOPLL Intel FPGA IP core as per Intel rebranding.	—
Added new settings to reduce jitter peaking: charge pump current, loop resistance, and ripplecap settings.	—
Added a new GUI parameter: **Create a permit_cal signal to connect with an upstream PLL** to export the `permit_cal` input.	—
Added a new input signal: `permit_cal`. Connecting this `permit_cal` port to the locked output port of the upstream I/O PLL ensures that the cascaded I/O PLLs are calibrated in the correct order.	—
Improved compensation accuracy.	—
Decreased IP simulation time.	—

Related Information

- Introduction to Intel FPGA IP Cores
- Intel® Stratix® 10 Clocking and PLL User Guide
- Altera I/O Phase-Locked Loop (Altera IOPLL) IP Core User Guide
- Errata for other IP cores in the Knowledge Base

Intel FPGA IOPLL v17.1

Table 2. v17.1 November 2017

Description	Impact
Added support for Intel Stratix 10 and Intel Cyclone® 10 GX devices.	—

Related Information

- Introduction to Intel FPGA IP Cores
- Intel Stratix 10 Clocking and PLL User Guide

- Altera I/O Phase-Locked Loop (Altera IOPLL) IP Core User Guide
- Errata for other IP cores in the Knowledge Base