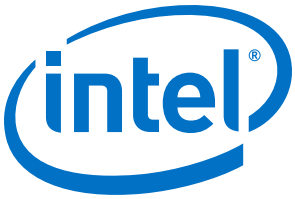

IOPLL Intel FPGA IP Core Release Notes

Subscribe
Send Feedback

RN-1160 | 2019.09.30
Latest document on the web: PDF | HTML

Contents

IOPLL Intel FPGA IP Core Release Notes

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the *Intel® Quartus® Prime Design Suite Update Release Notes*.

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

The IP versioning scheme (X.Y.Z) number changes from one software version to another. A change in:

- X indicates a major revision of the IP. If you update your Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Related Information

- Intel Quartus Prime Design Suite Update Release Notes
- Intel Agilex™ Clocking and PLL User Guide
- Intel Stratix® 10 Clocking and PLL User Guide
- Altera I/O Phase-Locked Loop (Altera IOPLL) IP Core User Guide
- Errata for other IP cores in the Knowledge Base

IOPLL Intel FPGA IP v19.3.0

Table 1. v19.3.0 2019.09.30

Intel Quartus Prime Version	Description	Impact
19.3	Added support for Intel Agilex™ devices.	—

IOPLL Intel FPGA IP v18.0

Table 2. v18.0 May 2018

Description	Impact
Renamed Intel FPGA IOPLL IP core to IOPLL Intel FPGA IP core as per Intel rebranding.	—
Added new settings to reduce jitter peaking: charge pump current, loop resistance, and ripplecap settings.	—
Added a new GUI parameter: **Create a permit_cal signal to connect with an upstream PLL** to export the `permit_cal` input.	—
Added a new input signal: `permit_cal`. Connecting this `permit_cal` port to the locked output port of the upstream I/O PLL ensures that the cascaded I/O PLLs are calibrated in the correct order.	—
Improved compensation accuracy.	—
Decreased IP simulation time.	—

Related Information

- Introduction to Intel FPGA IP Cores
- Intel Stratix® 10 Clocking and PLL User Guide
- Altera I/O Phase-Locked Loop (Altera IOPLL) IP Core User Guide
- Errata for other IP cores in the Knowledge Base

Intel FPGA IOPLL v17.1

Table 3. v17.1 November 2017

Description	Impact
Added support for Intel Stratix® 10 and Intel Cyclone® 10 GX devices.	—

Related Information

- Introduction to Intel FPGA IP Cores
- Intel Stratix 10 Clocking and PLL User Guide
- Altera I/O Phase-Locked Loop (Altera IOPLL) IP Core User Guide
- Errata for other IP cores in the Knowledge Base

Intel Stratix 10 Clocking and PLL User Guide Archives

If the table does not list a software version, the user guide for the previous software version applies.

Intel Quartus Prime Version	User Guide
19.2	Intel Stratix 10 Clocking and PLL User Guide
18.1	Intel Stratix 10 Clocking and PLL User Guide
18.0	Intel Stratix 10 Clocking and PLL User Guide
17.1	Intel Stratix 10 Clocking and PLL User Guide

IOPLL Intel FPGA IP Core User Guide Archives

If an IP core version is not listed, the user guide for the previous IP core version applies.

IP Core Version	User Guide
17.0	Altera I/O Phase-Locked Loop (Altera IOPLL) IP Core User Guide
16.1	Altera I/O Phase-Locked Loop (Altera IOPLL) IP Core User Guide
16.0	Altera I/O Phase-Locked Loop (Altera IOPLL) IP Core User Guide
15.0	Altera I/O Phase-Locked Loop (Altera IOPLL) IP Core User Guide