



IOPLL Intel FPGA IP Core Release Notes



Contents

IOPLL Intel FPGA IP Core Release Notes.....	3
IOPLL Intel FPGA IP v18.0.....	3
Intel FPGA IOPLL v17.1.....	3



IOPLL Intel FPGA IP Core Release Notes

If a release note is not available for a specific IP core version, the IP core has no changes in that version. Information on the latest update releases is in the *Intel Quartus Prime Design Suite Update Release Notes*.

Related Information

[Intel Quartus Prime Design Suite Update Release Notes](#)

IOPLL Intel FPGA IP v18.0

Table 1. v18.0 May 2018

Description	Impact
Renamed Intel FPGA IOPLL IP core to IOPLL Intel FPGA IP core as per Intel rebranding.	—
Added new settings to reduce jitter peaking: charge pump current, loop resistance, and ripplecap settings.	—
Added a new GUI parameter: Create a permit_cal signal to connect with an upstream PLL to export the permit_cal input.	—
Added a new input signal: permit_cal. Connecting this permit_cal port to the locked output port of the upstream I/O PLL ensures that the cascaded I/O PLLs are calibrated in the correct order.	—
Improved compensation accuracy.	—
Decreased IP simulation time.	—

Related Information

- [Introduction to Intel FPGA IP Cores](#)
- [Intel® Stratix® 10 Clocking and PLL User Guide](#)
- [Altera I/O Phase-Locked Loop \(Altera IOPLL\) IP Core User Guide](#)
- [Errata for other IP cores in the Knowledge Base](#)

Intel FPGA IOPLL v17.1

Table 2. v17.1 November 2017

Description	Impact
Added support for Intel Stratix 10 and Intel Cyclone® 10 GX devices.	—

Related Information

- [Introduction to Intel FPGA IP Cores](#)
- [Intel Stratix 10 Clocking and PLL User Guide](#)

Intel Corporation. All rights reserved. Intel, the Intel logo, Altera, Arria, Cyclone, Enpirion, MAX, Nios, Quartus and Stratix words and logos are trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.

*Other names and brands may be claimed as the property of others.

ISO
9001:2008
Registered



- [Altera I/O Phase-Locked Loop \(Altera IOPLL\) IP Core User Guide](#)
- [Errata for other IP cores in the Knowledge Base](#)