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IOPLL Reconfig Intel FPGA IP Core Release Notes

If a release note is not available for a specific IP core version, the IP core has no changes in that version. Information on the latest update releases is in the Intel Quartus Prime Design Suite Update Release Notes.

Related Information
Intel Quartus Prime Design Suite Update Release Notes

IOPLL Reconfig Intel FPGA IP v18.0

Table 1. v18.0 May 2018

<table>
<thead>
<tr>
<th>Description</th>
<th>Impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>Renamed Intel FPGA IOPLL Reconfig IP core to IOPLL Reconfig Intel FPGA IP core as per Intel rebranding.</td>
<td>—</td>
</tr>
<tr>
<td>Added advanced reconfiguration mode to dynamically reconfigure specific I/O PLL addresses.</td>
<td>Any incorrect settings may cause damage to the device.</td>
</tr>
</tbody>
</table>

Related Information
- Introduction to Intel FPGA IP Cores
- Intel® Stratix® 10 Clocking and PLL User Guide
- Errata for other IP cores in the Knowledge Base

Intel FPGA IOPLL Reconfig v17.1

Table 2. v17.1 November 2017

<table>
<thead>
<tr>
<th>Description</th>
<th>Impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>Initial release. This IP is available only in Intel Stratix 10 devices.</td>
<td>—</td>
</tr>
</tbody>
</table>

Related Information
- Introduction to Intel FPGA IP Cores
- Intel Stratix 10 Clocking and PLL User Guide
- Errata for other IP cores in the Knowledge Base

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