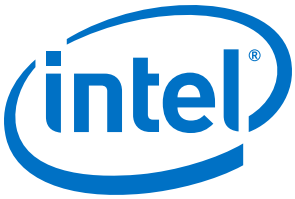

Interlaken (2nd Generation) Intel® FPGA IP Release Notes

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1. Interlaken (2nd Generation) Intel® FPGA IP FPGA IP Release Notes

If a release note is not available for a specific IP core version, the IP core has no changes in that version. For information on IP update releases up to v18.1, refer to the *Intel Quartus Prime Design Suite Update Release Notes*.

Intel® FPGA IP versions match the Intel Quartus® Prime Design Suite software versions until v19.1. Starting in Intel Quartus Prime Design Suite software version 19.2, Intel FPGA IP has a new versioning scheme.

The Intel FPGA IP version (X.Y.Z) number can change with each Intel Quartus Prime software version. A change in:

- X indicates a major revision of the IP. If you update the Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Related Information

- Intel Quartus Prime Design Suite Update Release Notes
- Interlaken (2nd Generation) Intel FPGA IP User Guide
- Errata for Interlaken (2nd Generation) Intel FPGA IP in the Knowledge Base
- Interlaken (2nd Generation) Intel Stratix 10 FPGA IP Design Example User Guide
- Interlaken (2nd Generation) Intel Agilex FPGA IP Design Example User Guide
- Introduction to Intel FPGA IP Cores

1.1. Interlaken (2nd Generation) Intel FPGA IP v20.0.0

Table 1. v20.0.0 2020.10.05

Intel Quartus Prime Version	Description	Impact
20.3	Added support for 25.78125 Gbps data rate.	—
	Modified the data rates support from 25.3 Gbps to 25.28 Gbps and 25.8 Gbps to 25.78125 Gbps.	—

1.2. Interlaken (2nd Generation) Intel FPGA IP v19.3.0

Table 2. v19.3.0 2020.06.22

Intel Quartus Prime Version	Description	Impact
19.3.0	The IP now supports Interlaken Look-aside feature.	—
	Added new **Enable Interlaken Look-aside mode** parameter in the IP parameter editor.	You can configure the IP in Interlaken Look-aside mode.
	Transfer mode selection parameter is removed from the current version of the Intel Quartus Prime software.	—
	Added 12.5 Gbps data rate support for number of lanes 10 in H-tile and E-tile (NRZ mode) IP core variations.	—
	Removed the following signals from the IP: • `rx_pma_data` • `tx_pma_data` • `itx_hungry` • `itx_hungry`	—
	Added following new signals: • `sop_cntr_inc1` • `eop_cntr_inc1` • `rx_xcoder_uncor_feccw` • `itx_ch0_xon` • `irx_ch0_xon` • `itx_ch1_xon` • `irx_ch1_xon` • `itx_valid` • `irx_valid` • `itx_idle` • `irx_idle` • `itx_ctrl` • `itx_credit` • `irx_credit`	—
	Removed following two offsets from register map: • 16'h40- TX_READY_XCVR • 16'h41- RX_READY_XCVR	—
	Hardware testing of the design example is now available for Intel Agilex™ devices.	You can test the design example on Intel Agilex F-series Transceiver-SoC Development Kit.
	You can change the data rate and transceiver reference clock frequency to slightly different values for your Interlaken (2nd Generation) IP instance that targets Intel Stratix® 10 H-tile or E-tile device. Refer to this KDB for information on how to change the data rate.	You can customize the data rates depending on the tiles.

1.3. Interlaken (2nd Generation) Intel FPGA IP v19.2.1

Table 3. v19.2.1 2019.09.27

Intel Quartus Prime Version	Description	Impact
19.3	Public release for Intel Agilex devices with E-tile transceivers.	—
	Renamed the Interlaken (2nd Generation) Intel Stratix 10 FPGA IP to Interlaken (2nd Generation) Intel FPGA IP	—

1.4. Interlaken (2nd Generation) Intel Stratix 10 FPGA IP v18.1 Update 1

Table 4. Version 18.1 Update 1 2019.03.15

Description	Impact
Added multi-segment mode support.	—
Added **Number of Segments** parameter.	—
• Added support for lane and data rate combinations as follows: — For Intel Stratix 10 L-tile devices: • 4 lanes with 12.5/25.3/25.8 Gbps lane rates • 8 lanes with 12.5 Gbps lane rates — For Intel Stratix 10 H-tile devices: • 4 lanes with 12.5/25.3/25.8 Gbps lane rates • 8 lanes with 12.5/25.3/25.8 Gbps lane rates • 10 lanes with 25.3/25.8 Gbps lane rates — For Intel Stratix 10 E-tile (NRZ) devices: • 4 lanes with 6.25/12.5/25.3/25.8 Gbps lane rates • 8 lanes with 12.5/25.3/25.8 Gbps lane rates • 10 lanes with 25.3/25.8 Gbps lane rates • 12 lanes with 10.3125 Gbps lane rate	—
• Added the following new transmit user interface signals: — itx_eob1 — itx_eopbits1 — itx_chan1	—
• Added the following new receiver user interface signals: — irx_eob1 — irx_eopbits1 — irx_chan1 — irx_err1 — irx_err	—

1.5. Interlaken (2nd Generation) Intel Stratix 10 FPGA IP v18.1

Table 5. Version 18.1 2018.09.10

Description	Impact	Notes
Renamed the document tile as *Interlaken (2nd Generation) Intel Stratix 10 FPGA IP User Guide*	—	—
Added VHDL simulation model and testbench support for Interlaken (2nd Generation) IP core.	—	—
Added the following new registers to the IP core: • TX_READY_XCVR • RX_READY_XCVR • ILKN_FEC_XCODER_TX_ILLEGAL_STATE • ILKN_FEC_XCODER_RX_ILLEGAL_STATE	—	These registers are only available in Intel Stratix 10 E-Tile device variations.

1.6. Interlaken (2nd Generation) Intel FPGA IP v18.0.1

Table 6. Version 18.0.1 July 2018

Description	Impact	Notes
Added support for Intel Stratix 10 devices with E-Tile transceivers.	—	—
Added 53.125 Gbps data rate support for Intel Stratix 10 E-Tile devices in PAM4 mode.	—	—
Added clock signal `mac_clkin` for Intel Stratix 10 E-Tile devices in PAM4 mode	—	—

1.7. Interlaken (2nd Generation) Intel FPGA IP v18.0

Table 7. Version 18.0 May 2018

Description	Impact	Notes
Renamed the Interlaken IP core (2nd Generation) to Interlaken (2nd Generation) Intel FPGA IP as per Intel rebranding.	—	—
Added 25.8 Gbps data rate support for number of lanes 6 and 12.	—	—
Added support for Cadence Xcelium* Parallel simulator.	—	—

1.8. Interlaken IP Core (2nd Generation) v17.1

Table 8. Version 17.1 November 2017

Description	Impact	Notes
Initial release in the Intel FPGA IP Library.	—	—

Related Information

Interlaken IP Core (2nd Generation) User Guide

1.9. Interlaken (2nd Generation) Intel FPGA IP User Guide Archives

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

If an IP core version is not listed, the user guide for the previous IP core version applies.

Quartus Version	IP Core Version	User Guide
20.2	19.3.0	Interlaken (2nd Generation) FPGA IP User Guide
19.3	19.2.1	Interlaken (2nd Generation) FPGA IP User Guide
19.2	19.2	Interlaken (2nd Generation) FPGA IP User Guide
18.1.1	18.1.1	Interlaken (2nd Generation) Intel Stratix 10 FPGA IP User Guide
18.1	18.1	Interlaken (2nd Generation) Intel Stratix 10 FPGA IP User Guide
18.0.1	18.0.1	Interlaken (2nd Generation) FPGA IP User Guide
18.0	18.0	Interlaken (2nd Generation) Intel FPGA IP User Guide
17.1	17.1	Interlaken IP Core (2nd Generation) User Guide