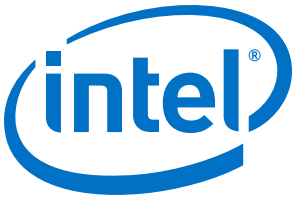

# Intel® Acceleration Stack for Intel® Xeon® CPU with FPGAs Version 1.2 Release Notes

Updated for Intel® Acceleration Stack for Intel® Xeon® CPU with FPGAs: **1.2**



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Latest document on the web: PDF | HTML

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# Notice

Please note that the Intel® Acceleration Stack for Intel Xeon® CPU with FPGAs DOES NOT include mitigations for the exploits known as Spectre (CVE-2017-5753, CVE-2017-5715) and Meltdown (CVE-2017-5754). These exploits require that malware runs locally on the system, which is not normally possible in a closed environment where the system's software is centrally controlled. Intel does not recommend that an un-mitigated version of the Intel Acceleration Stack for Intel Xeon CPU with FPGAs be used in an environment that is not a closed system environment.

# Intel Acceleration Stack for Intel Xeon CPU with FPGAs Version 1.2 Release Notes

This document provides up-to-date information about the Intel Acceleration Stack for Intel Xeon CPU with FPGAs version 1.2 release.

## Acceleration Acronym List

Use the following table as a reference when reviewing the release notes.

**Table 1. Acronyms**

| Acronyms | Expansion | Description |
|---|---|---|
| AFU | Accelerator Functional Unit | Hardware Accelerator implemented in FPGA logic which offloads a computational operation for an application from the CPU to improve performance. |
| AF | Accelerator Function | Compiled Hardware Accelerator image implemented in FPGA logic that accelerates an application. An AFU and associated AFs may also be referred to as GBS (Green-Bits, Green BitStream) in the Acceleration Stack installation directory tree and in source code comments. |
| ASE | AFU Simulation Environment | Co-simulation environment that allows you to use the same host application and AF in a simulation environment. ASE is part of the Intel Acceleration Stack for FPGAs. |
| FIM | FPGA Interface Manager | The FPGA hardware containing the FPGA Interface Unit (FIU) and external interfaces for memory, networking, etc.<br>The FIM may also be referred to as BBS (Blue-Bits, Blue BitStream) in the Acceleration Stack installation directory tree and in source code comments.<br>The Accelerator Function (AF) interfaces with the FIM at run time. |
| HSSI | High-speed Serial Interface | Reference to the multi-gigabit serial transceiver I/O in the FIM and the corresponding interface to the Accelerator Functional Unit (AFU). |

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| Acronyms | Expansion | Description |
|---|---|---|
| OPAE | Open Programmable Acceleration Engine | The OPAE is a software framework for managing and accessing AFs. |
| PIM | Platform Interface Manager | An abstraction layer for managing top-level device ports and system-provided clock crossing. |
| PR | Partial Reconfiguration | The ability to dynamically reconfigure a portion of an FPGA while the remaining FPGA design continues to function. |

## Minimum Requirements

The minimum requirements for the Intel Programmable Acceleration Card with Intel Arria® 10 GX FPGA must include:

- Intel Xeon Scalable processor
- A PCI Express* x16 Slot
- 48 GB of free memory is a requirement only if you are compiling a hardware design
- Operating System:
  - Red Hat* Enterprise Linux* (RHEL) version 7.4
  - CentOS version 7.4
  - Ubuntu* version 16.04
- Board management controller (BMC) firmware version 26889 and bootloader version 26879.

### Related Information

Intel Acceleration Stack Quick Start Guide for Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA
For more information on how to flash the firmware image.

# Intel Acceleration Stack Reference Table

## Table 2. Intel Acceleration Stack Reference Table

*Note:* Intel recommends porting AFUs and workloads to the Intel Acceleration Stack v1.2. You must recompile and validate when upgrading to the new release. The Intel Acceleration Stack v1.2 cannot be downgraded to previous versions.

*Note:* When the image in the user partition cannot be loaded, a flash failover occurs and the factory image is loaded instead. After a flash failover occurs, the PR ID reads as d4a76277-07da-528d-b623-8b9301feaffe.

| Intel Acceleration Stack Version | Platform | FPGA Interface Manager (FIM) Version: Partial Reconfiguration (PR) Interface ID | Open Programmable Acceleration Engine (OPAE) Version | Intel Quartus® Prime Pro Edition |
|---|---|---|---|---|
| 1.2 | Intel PAC with Intel Arria 10 GX FPGA | 69528db6-eb31-577a-8c36-68f9faa081f6 | 1.1.2 | 17.1.1 |
| 1.1 | Intel PAC with Intel Arria 10 GX FPGA | 9926ab6d-6c92-5a68-aabc-a7d84c545738 | 1.0.2 | 17.1.1 |
| 1.0 | Intel PAC with Intel Arria 10 GX FPGA | ce489693-98f0-5f33-946d-560708be108a | 0.13.1 | 17.0.0 |

# Intel Acceleration Stack v1.2 Enhancements

## Table 3. Enhancements in the Intel Acceleration Stack v1.2

| Area | Enhancement |
|---|---|
| Operating System Support | Support for Ubuntu version 16.04. |
| Telemetry Support over PCIe | • The `fpgaflash` command in OPAE supports remote system updates to board management controller firmware over PCIe*. For steps on how to flash the firmware, please refer to the *Intel Acceleration Stack Quick Start Guide for Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA*.<br>• The `fpgainfo` command allows you to retrieve FPGA sensor information.<br>*Note:* Telemetry over PCIe is only supported in the BMC firmware version 26889 and BMC bootloader version 26879 or higher. |
| pacd daemon Service | This system service runs in the background and offers:<br>• Monitoring of board management sensor values.<br>• Triggering of events to prevent card from exceeding thresholds.<br>• Ability to specify poll and cool down intervals.<br>For information on `pacd`, please refer to the *Intel Acceleration Stack Quick Start Guide for Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA*.<br>*Note:* The pacd deamon service is only supported in the BMC firmware version 26889 and BMC bootloader version 26879 or higher. |
| QSFP | Default physical medium attachment (PMA) settings for Intel supported cables are now part of the Intel Acceleration Stack installer. Refer to the QSFP+ section in the *Intel Programmable Acceleration Card (PAC) with Intel Arria 10 GX Datasheet* for a list of cables and switches used in the validation configuration. |
| HSSI | New flag -m to set destination MAC address. |
| Streaming DMA | Improvement in streaming DMA bandwidth with the addition of non-uniform memory access (NUMA) affinity. |

# Intel Acceleration Stack v1.2 Known Issues

## Table 4. Known Issues for the Intel Acceleration Stack v1.2

| Known Issue | Details |
|---|---|
| PCIe directed speed changes are not supported. | Only automatic down-training at boot time is supported. |
| Invalid memory read fault may cause FIM to lock. | • The FIM locks after the AFU sends a memory read to invalid address.<br>• Workaround: Power cycle the system to reinitialize the Intel PAC with Intel Arria 10 GX FPGA and recover from this issue. Refer to the Knowledge Base entry for more information.<br>• Status: Fix targeted for a future version of the Intel Acceleration Stack. |
| Possible corruption of board management controller firmware during an in-band update. | • The board management controller firmware may be corrupted when performing an in-band update using fpgaflash. This event prevents the Intel PAC with Intel Arria 10 GX FPGA from booting after the update.<br>• Workaround: The current installer implements a workaround that checks for data corruption and retries an update up to three times. If the update continues to fail after the three attempts you must relaunch the fpgaflash command without rebooting your host.<br>• Status: Fix targeted for a future version of firmware. |
| When an AFU workload exceeds board management controller sensor thresholds, the server may reboot. | • An AFU workload may exceed the board management controller threshold before pacd can identify and act on the threshold violation. If this situation occurs, the board management controller removes the card from the PCIe bus and the server reboots before the pacd can perform a graceful shutdown.<br>• Workaround: No workaround available.<br>• Status: Fix targeted for a future version of the Intel Acceleration Stack. |
| Streaming DMA only supports access to host memory. | • The streaming DMA basic building blocks (BBBs) can access host or FPGA memory, but the driver does not provide any means for accessing FPGA memory.<br>• Status: This limitation will be fixed in a future version of the driver. |
| Inconsistency in `green_bs` input port naming. | The names of the clock port inputs to the `green_bs` block do not correspond to resulting frequency provided from the `dcp_io_pll` block.<br>**Table 5. Clock Port Input Inconsistency**<br>**`dcp_io_pll` port frequency provided to `green_bs` block clock input** / **`green_bs` clock input port name**<br>50 MHz / `clk_100`<br>100 MHz / `clk_200`<br>200 MHz / `clk_400`<br>The file can be found at `a10_gx_pac_ias_1_2_alpha/hw/lib/build/platform/green_bs.sv`.<br>Status: Fix targeted for a future version of the Intel Acceleration Stack. |

*continued...*

| Known Issue | Details |
|---|---|
| `setup_permissions.sh` in OpenCL* prints error when using virtual machine. | • When you run the `setup_permissions.sh` script in a virtual machine to set permissions and system parameters for OpenCL, the following error displays:<br>`chmod: cannot access '/dev/intel-fpga-fme.*': No such file or directory.`<br>• Workaround: No workaround available.<br>• Status: Fix targeted for a future version of the Intel Acceleration Stack. |
| Graceful shutdown is not supported when using a virtual machine. | • When a hypervisor is connected to a virtual function on a card, Intel PAC daemon (pacd) cannot perform graceful shutdown when the sensor thresholds are exceeded. In this case, the hypervisor and server reboot.<br>• Workaround: No workaround available.<br>• Status: Fix targeted for a future version of the Intel Acceleration Stack. |
| The BMC may return incorrect sensor data. | • The BMC may return incorrect sensor data to the `pacd` and `fpgainfo` tool. This incorrect data may cause `pacd` to interrupt the execution of applications using the Intel Programmable Acceleration Card (PAC) resulting in a system reboot.<br>• Workaround: No workaround available.<br>• Status: Fix targeted for a future version of the Intel Acceleration Stack. |
| The fpgainfo error `First Malformed Req` returns 0xFFFFFFFFFFFFFFFF for `streaming_dma_afu.gbs` or `dma_afu.gbs`. | • If you configure the `streaming_dma_afu.gbs` or `dma_afu.gbs` using `fpgaconfig` and then run `fpgainfo errors`, the command returns a `First Malformed Req` error of 0xFFFFFFFFFFFFFFFF. This error is not valid and does not affect the functioning of the `dma_afu` or `streaming_dma_afu` block.<br>• Workaround: No workaround available.<br>• Status: Fix targeted for a future version of the Intel Acceleration Stack. |
| Virtual Function (VF) may fail to attach or detach when using the Linux Red Hat* 3.10 kernel. | The VF failure to attach or detach is a known issue with `qemu/kvm` and `libvirt`. Refer to the Red Hat website for more information about this issue. |

# Intel Acceleration Stack v1.2 Resolved Issues

## Table 6. Issues Resolved from v1.1 to v1.2 in the Intel Acceleration Stack Software

| Area | Description |
|---|---|
| AFU | Designs now function properly when a customer loads an AFU for a second time using `fpgaconf`. Please contact Intel Support for further questions. |
| Streaming DMA AFU | Corrected packet transfers. Intel Acceleration Stack version 1.1 Production only supported end-of-packet (EOP) assertion for packet transfers. Intel Acceleration Stack version 1.2 Alpha asserts start-of-packet (SOP) to indicate the beginning of a transfer. |
| Streaming DMA AFU | Corrected non-deterministic length transfers. Non-deterministic length stream-to-memory transfers end when the byte length of data is received or EOP is found in the received stream, whichever happens earlier. Intel Acceleration Stack version 1.1 Production ignored transfer length. |

# Intel Acceleration Stack for Intel Xeon CPU with FPGAs Release Notes Archives

| Intel Acceleration Stack Version | User Guide |
|---|---|
| 1.1 | Intel Accleration Stack for Intel Xeon CPU with FPGAs Version 1.1 Release Notes |
| 1.0 | Intel Accleration Stack for Intel Xeon CPU with FPGAs Version 1.0 Release Notes |

# Intel Acceleration Stack for Intel Xeon CPU with FPGAs v1.2 Release Notes Revision History

| Date | Acceleration Stack Version | Changes |
|---|---|---|
| 2019.03.08 | 1.2 (compatible with Intel Quartus Prime Pro Edition 17.1.1) | Added known issue "Using `pacd` may result in false failures." |
| 2019.02.23 | 1.2 (compatible with Intel Quartus Prime Pro Edition 17.1.1) | Added note about upgrading to the Intel Acceleration Stack v1.2 in the *Intel Acceleration Stack Reference Table* section. |
| 2018.12.04 | 1.2 (compatible with Intel Quartus Prime Pro Edition 17.1.1) | Initial release. |