Intel® Acceleration Stack for Intel® Xeon® CPU with FPGAs Version 2.0.1
Release Notes

For the Intel FPGA Programmable Acceleration Card D5005

Updated for Intel® Acceleration Stack for Intel® Xeon® CPU with FPGAs: 2.0.1
Notice........................................................................................................................................... 3

Intel Acceleration Stack for Intel Xeon CPU with FPGAs Version 2.0.1 Release Notes
for the Intel FPGA PAC D5005.................................................................................................. 4
  Acceleration Acronym List........................................................................................................ 4
  Minimum Requirements............................................................................................................ 5
  Intel Acceleration Stack v2.0.1 Reference Table.................................................................. 5
  Intel Acceleration Stack v2.0.1 Features............................................................................... 6
  Known Issues for the Intel Acceleration Stack v2.0.1......................................................... 7
  Resolved Issues from Intel Acceleration Stack v2.0 to v2.0.1............................................. 9
  Resolved Issues from Intel Acceleration Stack v2.0.1 Beta to v2.0.1 Production............... 9
  Known Issues for the Intel Acceleration Stack v2.0.1 AFU Design Examples.................. 11
  Resolved Issues from Intel Acceleration Stack v2.0 to v2.0.1 AFU Design Examples........ 11
  Revision History for the Intel Acceleration Stack for Intel Xeon CPU with FPGAs v2.0.1
    Release Notes.................................................................................................................. 12
Notice

Please note that the Intel® Acceleration Stack for Intel Xeon® CPU with FPGAs DOES NOT include mitigations for the exploits known as Spectre (CVE-2017-5753, CVE-2017-5715) and Meltdown (CVE-2017-5754). These exploits require that malware runs locally on the system, which is not normally possible in a closed environment where the system’s software is centrally controlled. Intel does not recommend that an un-mitigated version of the Intel Acceleration Stack for Intel Xeon CPU with FPGAs be used in an environment that is not a closed system environment.
# Intel Acceleration Stack for Intel Xeon CPU with FPGAs
## Version 2.0.1 Release Notes for the Intel FPGA PAC D5005

This document provides up-to-date information about the Intel Acceleration Stack for Intel Xeon CPU with FPGAs version 2.0.1 release for the Intel FPGA PAC D5005.

## Acceleration Acronym List

Use the following table as a reference when reviewing the release notes.

### Table 1. Acronyms

<table>
<thead>
<tr>
<th>Acronyms</th>
<th>Expansion</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AFU</td>
<td>Accelerator Functional Unit</td>
<td>Hardware Accelerator implemented in FPGA logic which offloads a computational operation for an application from the CPU to improve performance.</td>
</tr>
<tr>
<td>AF</td>
<td>Accelerator Function</td>
<td>Compiled Hardware Accelerator image implemented in FPGA logic that accelerates an application. An AFU and associated AFs may also be referred to as GBS (Green-Bits, Green BitStream) in the Acceleration Stack installation directory tree and in source code comments.</td>
</tr>
<tr>
<td>ASE</td>
<td>AFU Simulation Environment</td>
<td>Co-simulation environment that allows you to use the same host application and AF in a simulation environment. ASE is part of the Intel Acceleration Stack for FPGAs.</td>
</tr>
<tr>
<td>FIM</td>
<td>FPGA Interface Manager</td>
<td>The FPGA component containing the FPGA Interface Unit (FIU) and external interfaces for memory, networking, etc. The FIM may also be referred to as BBS (Blue-Bits, Blue BitStream) in the Acceleration Stack installation directory tree and in source code comments. The Accelerator Function (AF) interfaces with the FIM at run time.</td>
</tr>
<tr>
<td>HSSI</td>
<td>High-speed Serial Interface</td>
<td>Reference to the multi-gigabit serial transceiver I/O in the FIM and the corresponding interface to the Accelerator Functional Unit (AFU).</td>
</tr>
</tbody>
</table>

*continued...*
### Acronyms

<table>
<thead>
<tr>
<th>Acronyms</th>
<th>Expansion</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPAE</td>
<td>Open Programmable Acceleration Engine</td>
<td>The OPAE is a software framework for managing and accessing AFs.</td>
</tr>
<tr>
<td>PIM</td>
<td>Platform Interface Manager</td>
<td>An abstraction layer for managing top-level device ports and system-provided clock crossing.</td>
</tr>
<tr>
<td>PR</td>
<td>Partial Reconfiguration</td>
<td>The ability to dynamically reconfigure a portion of an FPGA while the remaining FPGA design continues to function.</td>
</tr>
</tbody>
</table>

### Minimum Requirements

The minimum requirements for the Intel FPGA Programmable Acceleration Card D5005 are:

- Intel Xeon Scalable processor
- A PCI Express* x16 Slot
- 128 GB of free memory is a requirement only if you are compiling a hardware design
- Operating System:
  - Red Hat* Enterprise Linux* (RHEL) version 7.6 Kernel 3.10.0-957
- PACTool tool requires Python 3.0
- OPAE tools require Python 2.7
- OpenCL* RTE version 19.2.0.57

### Intel Acceleration Stack v2.0.1 Reference Table

Table 2. Intel Acceleration Stack Best Known Configuration

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>2.0.1</td>
<td>Intel FPGA PAC D5005</td>
<td>9346116d-a52d-5ca8-b06a-a9a389ef7c8d</td>
<td>1.1.4-8</td>
<td>19.2</td>
<td>2.0.6</td>
<td>2.0.12</td>
</tr>
<tr>
<td>2.0</td>
<td>Intel FPGA PAC D5005</td>
<td>bfac4d85-1ee8-56fe-8c95-865ce1bbaa2d</td>
<td>1.1.4-3</td>
<td>18.1.2</td>
<td>1.0.15</td>
<td>1.0.12</td>
</tr>
</tbody>
</table>

When the image in the user partition cannot be loaded, a flash failover occurs and the factory image is loaded instead. After a flash failover occurs, the PR ID reads as 9346116d-a52d-5ca8-b06a-a9a389ef7c8d.
Table 3. Features of the Intel Acceleration Stack v2.0.1

<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
</tr>
</thead>
</table>
| **Security Enhancements** | • Intel MAX® 10 Root-of-Trust Implementation  
  • Support for BMC firmware, BMC RTL, FIM, and AFU signing  
  • New OPAE security tools:  
    1. FPGA one-time secure update (fpgaotsu): Upgrades from v2.0 to v2.0.1  
    2. FPGA secure update (fpgasupdate): Remotely updates bitstreams securely. fpgasupdate replaces fpgaflash.  
    4. PACSign: Enables signing of bitstreams. To use this tool, you must have the capability to generate a public/private key pair and your hardware security module (HSM) must support a Public-Key Cryptography Standards (PKCS)#11 compatible application programming interface (API) to the PACSign tool. |
| **CCI-P Byte Enable** | Supports programmable byte writes less than 1 cache line in length. Refer to the Intel Acceleration Stack for Intel Xeon CPU with FPGAs Core Cache Interface (CCI-P) Reference Manual for more details. |
| **Networking Interface** | • Interface supports 32-bit PCS direct mode (PMA only).  
  • 10 GbE MAC AFU is not provided.  
  • Pseudo-random bit stream generator (PRBS) AFU provided to test interface. |
| **Sample AFUs Supported** | The following unsigned AFU examples are provided with the Intel Acceleration Stack for Intel Xeon CPU with FPGAs:  
  • dma_afu_unsigned.gbs  
  • streaming_dma_afu_unsigned.gbs  
  • hello_afu_unsigned.gbs  
  • hello_mem_afu_unsigned.gbs  
  • hello_intr_afu_unsigned.gbs  
  • nlb_mode_0_unsigned.gbs  
  • nlb_mode_0_stp_unsigned.gbs  
  • nlb_mode_3_unsigned.gbs  
  • byte_enable_afu_unsigned.gbs  
  • hssi_prbs_unsigned.gbs  
  **Note:** Each *.* unsigned.gbs above is prepended with the necessary block0 and block1 headers but there are no hashes in these headers that have been signed with the root and code signing keys. To learn how to securely sign a provided *.* unsigned.gbs refer to the Intel Acceleration Stack Quick Start Guide: Intel FPGA Programmable Acceleration Card D5005. |

**Related Information**

- Intel Acceleration Stack for Intel Xeon CPU with FPGAs Core Cache Interface (CCI-P) Reference Manual  
- Intel Acceleration Stack Quick Start Guide: Intel FPGA Programmable Acceleration Card D5005
### Known Issues for the Intel Acceleration Stack v2.0.1

<table>
<thead>
<tr>
<th>Known Issue</th>
<th>Details</th>
</tr>
</thead>
</table>
| The Intel FPGA PAC D5005 may be unable to recover after an AFU fails to load onto the card. This issue can occur if a \*.gbs file is not signed with the correct key or if a \*.gbs file is corrupted. | • When the AFU fails to load on the card, you see this error message:  
  ```plaintext
  WARNING | Update starting. Please do not interrupt.  
  libopae-reconf.c:427:fpgaReconfigureSlot() **ERROR** : Failed to reconfigure bitstream: Input/output error  
  libopae-reconf.c:455:fpgaReconfigureSlot() **ERROR** : PRIP protocol error detected  
  Error writing bitstream to FPGA: reconfiguration error  
  ```  
  • Workaround: To recover after loading a corrupted or incorrectly signed AFU onto the Intel FPGA PAC D5005, power cycle the card.  
  • Status: This limitation will be fixed in a future version of the Intel Acceleration Stack. |
| `fpgabist -i` does not check device ID or report errors on incorrect device ID. | • Workaround: None available.  
  • Status: Fix targeted for a future version of the Intel Acceleration Stack. |
| Invalid memory read fault may cause FIM to lock.                          | • The FIM locks after the AFU sends a memory read to invalid address.  
  — When using `fpgainfo`, this error displays as `compStatErr`.  
  — When using `sudo lspci -vvs B:D.F` this error displays as `TransPend+entry under DevSta`.  
  • Workaround: Power cycle the card to reinitialize the Intel FPGA PAC and recover from this issue. Refer to the Knowledge Base entry for more information.  
  • Status: Fix targeted for a future version of the Intel Acceleration Stack. |
| The Intel FPGA PAC D5005 may report that a non-fatal error has occurred during boot. | • This error is not seen if you are using OPAE drivers. If you do not have the OPAE drivers installed, the Intel FPGA PAC D5005 responds to configuration read requests to functions that do not exist by returning `NonFatalErr+` error responses. You can clear and ignore these errors after boot.  
  • Workaround: If you are not using the OPAE driver to handle this error, you can clear the relevant errors at boot:  
    ```bash
    sudo setpci -s BDF ECAP_AER+0x10.L=0xFFFFFFFF  
    ```  
  • Status: Fix targeted for a future version of the Intel Acceleration Stack. |
| QSFP link and activity LEDs do not reflect Ethernet link status.       | • Workaround: None available.  
  • Status: Fix targeted for a future version of the board management controller firmware. |

---

Send Feedback
<table>
<thead>
<tr>
<th>Known Issue</th>
<th>Details</th>
</tr>
</thead>
</table>
| PACSign tool requires Python* version 3.x software to be in /usr/bin.     | • Although the PACSign tool requires Python version 3.x software to be in /usr/bin, installation from a local zip file typically results in the software being installed to /usr/local/bin.  
  • Workaround: When installing from source, complete the following commands:  
    ```bash  
    tar zxvf Python-3...tgz  
    cd Python-3...  
    ./configure --prefix=/usr  
    make  
    sudo make install  
    ```
  to install the tool in the correct directory. If you have already installed in /usr/local/bin, you can invoke the PACSign command using python3 /usr/local/bin/PACSign.  
  • Status: Fix targeted for a future version of the Intel Acceleration Stack. |
| When virtual functions (VF) or physical functions (PF) send multiple unaligned read or write requests to the Intel FPGA PAC D5005 registers, the host reboots. | • This issue only exists when using Red Hat* Enterprise Linux (RHEL) version 7.6 Kernel 3.10.0-957.  
  • Workaround: None available.  
  • Status: This limitation is addressed in newer Linux kernels. Intel recommends upgrading from the Red Hat* Enterprise Linux (RHEL) version 7.6 Kernel 3.10.0-957 kernel. No fixes are planned for this version of the kernel. |
| The Intel FPGA PAC D5005 does not support optical module cables that require the ResetL pin to be driven high for link up to complete. | • Workaround: None available.  
  • Status: Fix targeted for a future version of the Intel Acceleration Stack. |
| The Intel FPGA PAC D5005 reports a preset QSFP temperature threshold value irrespective of what is specified in the QSFP module data sheet. | • The Intel FPGA PAC D5005 reports a QSFP module temperature of 70C for upper-non critical threshold and 90C for upper non-recoverable threshold regardless of what the specified value is for that QSFP module.  
  • Workaround: Monitor the QSFP temperature reported by the sensors to ensure the module is not exceeding operating conditions defined in the QSFP module's data sheet.  
  • Status: Fix targeted for a future version of the Intel Acceleration Stack. |
| fpgainfo bmc may not return QSFP Supply Voltage if your QSFP module does not support supply voltage registers. | • The Intel MAX 10 BMC obtains the QSFP voltage sensor value from the Supply Voltage registers beginning at offset 26, as listed in the Free Side Monitoring Values Table 6-7, of the SFF8636 Specification for Management Interface for 4-Lane Modules and Cables, rev2.10a.  
  • Workaround: If your QSFP module does not support this register please disregard the value returned by the Intel MAX 10 BMC when using the fpgainfo bmc command.  
  • Status: No fix. |
| If pacd is killed before it recovers from a sensor trip, fpgasupdate or other accesses to the FPGA may fail. | • Workaround: Resetting the FPGA is the only way to recover from the failure.  
  • Status: Fix targeted for a future version of the Intel Acceleration Stack. |
| Running the OpenCL example may give a segmentation fault. | • Including the parameter default_hugepagesz=1G creates the error.  
  • Workaround: Remove the parameter default_hugepagesz=1G.  
  • Status: Fix targeted for a future version of the Intel Acceleration Stack. |

continued...
A partial reconfiguration (PR) compile using OpenCL may produce hold time violations in the static regions.

- **Workaround:** Recompile using a different seed with the command:
  ```bash
  aoc <kernel_name.cl> -seed=<integer>
  ```
  For example:
  ```bash
  aoc hello_world.cl -seed=5
  ```
- **Status:** Fix targeted for a future version of the Intel Acceleration Stack.

PCIe* bandwidth limitation with OpenCL designs.

- PCIe Gen3x16 operates at a lower throughput than expected only with OpenCL designs.
- **Workaround:** None available.
- **Status:** Fix targeted for a future version of the Intel Acceleration Stack.

PACSign tool requires installation of Python* version 3.x through the rpm process.

- Installation of Python* version 3.x from source is not accepted by PACSign. PACSign looks for python 3.x in rpm repository.
- **Workaround:** You must install Python3 using the following command before installing the Acceleration Stack for Runtime or the Acceleration Stack for Development.
  ```bash
  sudo yum install python3
  ```
- **Status:** Fix targeted for a future version of the Intel Acceleration Stack.

---

**Resolved Issues from Intel Acceleration Stack v2.0 to v2.0.1**

*Table 5. Resolved Issues from Intel Acceleration Stack v2.0 to v2.0.1*

<table>
<thead>
<tr>
<th>Known Issue</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPAE does not verify the signatures it loads onto the Intel FPGA PAC D5005.</td>
<td>Fixed.</td>
</tr>
<tr>
<td>The <code>fpgaflash</code> BDF value is case sensitive.</td>
<td>Fixed.</td>
</tr>
<tr>
<td>The <code>/var/log/message</code> file includes error messages on invalid rules that are not active.</td>
<td>Fixed.</td>
</tr>
<tr>
<td>After a cold boot, SPI reads from the host to the BMC using the OPAE <code>fpgainfo bmc</code> command may not complete.</td>
<td>Not reproducible, closed.</td>
</tr>
</tbody>
</table>

**Resolved Issues from Intel Acceleration Stack v2.0.1 Beta to v2.0.1 Production**

*Table 6. Resolved Issues from Intel Acceleration Stack v2.0.1 Beta to v2.0.1 Production*

<table>
<thead>
<tr>
<th>Known Issue</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>fpgainfo bmc</code> output reports intermittent incorrect values if any of the the <code>nlb_mode_*</code>.gbs AFUs and <code>fpgainfo</code> are run simultaneously.</td>
<td>Fixed.</td>
</tr>
<tr>
<td>The Intel MAX 10 BMC does not allow failover to the FPGA factory image if the FPGA user image is corrupt.</td>
<td>Fixed.</td>
</tr>
</tbody>
</table>

*continued...*
<table>
<thead>
<tr>
<th>Known Issue</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>The same encoding response is returned for an invalid or retry response when writing to the SMBus parameter mailbox.</td>
<td>Fixed.</td>
</tr>
<tr>
<td>Intel Quartus Prime Pro Edition v19.2 Timing Analyzer may report two setup timing violations in the transceiver, in the fast 900 mV, 100 C corner.</td>
<td>Fixed.</td>
</tr>
<tr>
<td>PACSign tool requires Python version 3.x software to be in /usr/bin.</td>
<td>Fixed. When installing the PACSign *.rpm, the component installs in /usr/bin. &lt;br&gt;Note: PACSign still requires Python version 3.x.</td>
</tr>
</tbody>
</table>
Known Issues for the Intel Acceleration Stack v2.0.1 AFU Design Examples

Table 7. Known Issues for the Intel Acceleration Stack v2.0.1 AFU Design Examples

<table>
<thead>
<tr>
<th>Known Issue</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>The streaming_dma_afu_unsigned.gbs, dma_afu_unsigned.gbs show timing violations that may limit their operation.</td>
<td>• Workaround: No workaround available. • Status: This limitation will be fixed in a future patch of the Intel Acceleration Stack.</td>
</tr>
<tr>
<td>The Intel Quartus Prime Pro Edition compilation report for hello_mem__afu_unsigned.gbs displays Fmax and slack times incorrectly.</td>
<td>• Workaround: To view the correct timing, open the results in the Timing Analyzer tool or in the timing reports found in output_files/timing_reports for the final timing reports of the design. • Status: This limitation will be fixed in a future version of the Intel Acceleration Stack.</td>
</tr>
<tr>
<td>After a partial reconfiguration of a dma_afu_unsigned.gbs or a streaming dma_afu_unsigned.gbs, First Malformed Req is set in the PORT errors output.</td>
<td>• Workaround: To clear the errors, you must power cycle the Intel FPGA PAC. • Status: This limitation will be fixed in a future version of the Intel Acceleration Stack.</td>
</tr>
</tbody>
</table>
| Running the fpgabist command on nlb_mode_3_unsigned.gbs reports incorrect output. | • Instead of reporting the output of a throughput test, a default BIST test runs. • Workaround: Load the nlb_mode_3_unsigned.gbs bitstream. Complete the steps below to get read, write and read-write combined bandwidth:  

```
$ fpgadiag -B -D -F --mode=read --read-vc=vh0 --write-vc=vh0 --multi-cl=4 --begin=1024 --end=1024 --timeout-sec=5 --cont
$ fpgadiag -B -D -F --mode=write --read-vc=vh0 --write-vc=vh0 --multi-cl=4 --begin=1024 --end=1024 --timeout-sec=5 --cont
$ fpgadiag -B -D -F --mode=trput --read-vc=vh0 --write-vc=vh0 --multi-cl=4 --begin=1024 --end=1024 --timeout-sec=5 --cont
```
• Status: This limitation will be fixed in a future version of the Intel Acceleration Stack. |

Resolved Issues from Intel Acceleration Stack v2.0 to v2.0.1 AFU Design Examples

Table 8. Resolved Issues for the Intel Acceleration Stack v2.0.1 AFU Design Examples

<table>
<thead>
<tr>
<th>Known Issue</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Compilation of nlb_mode_3 AFU from source produces incorrect nlb_400.gbs output.</td>
<td>Fixed.</td>
</tr>
<tr>
<td>The dma_afu may access an invalid host memory address causing a Translation Layer Packet Completion Status error (TLP CPL status error).</td>
<td>Fixed.</td>
</tr>
<tr>
<td>After initial programming of the dma_afu subsequent partial reconfigurations may cause the kernel message to report errors.</td>
<td>Fixed.</td>
</tr>
</tbody>
</table>
### Revision History for the Intel Acceleration Stack for Intel Xeon CPU with FPGAs v2.0.1 Release Notes

<table>
<thead>
<tr>
<th>Date</th>
<th>Acceleration Stack Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>2019.12.26</td>
<td>2.0.1 (compatible with Intel Quartus Prime Pro Edition v19.2)</td>
<td>Added a new known issue: <em><em>PACSRun tool requires installation of Python</em> version 3.x through the rpm process.</em>*</td>
</tr>
</tbody>
</table>